Texas Instruments

Analog Engineer's Circuit Cookbook: Amplifiers

Introduction

The *Analog Engineer's Circuit Cookbook*: *Amplifiers* provides amplifier subcircuit ideas that you can quickly adapt to meet your specific system needs. Each circuit is presented as a "definition by example." It includes step-by-step instructions, like a recipe, with formulas enabling you to adapt the circuit to meet your design goals. Additionally, all circuits are verified with SPICE simulations.

We've provided at least one recommended amplifier for each circuit, but you can swap it with another amplifier if you've found one that's a better fit for your design. You can search our portfolio at ti.com/amplifiers.

Our circuits require a basic understanding of amplifier concepts. If you're new to amplifier design, we highly recommend completing our **TI Precision Labs (TIPL) training series**. TIPL includes courses on introductory topics, such as device architectures, as well as advanced, application-specific problem-solving, using both theory and practical knowledge. Check out our curriculum for operational amplifiers (op amps), analog-to-digital converters (ADCs) and more at **ti.com/precisionlabs**.

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Integrator Circuit

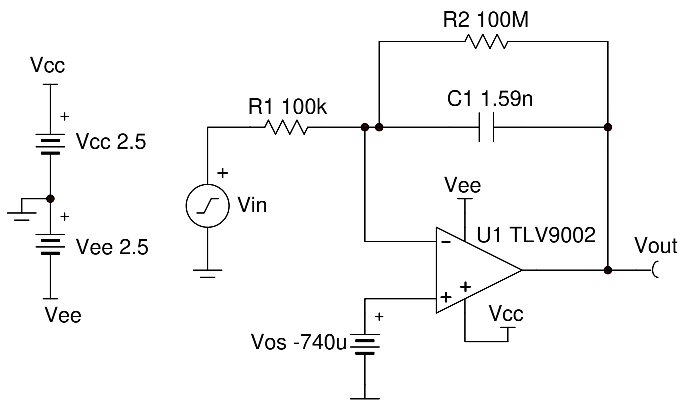
TEXAS INSTRUMENTS

Design Goals

Input			Output		Supply	
f_{Min}	f_{0dB}	f_{Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
100 Hz	1 kHz	100 kHz	–2.45 V	2.45 V	2.5 V	–2.5 V

Design Description

The integrator circuit outputs the integral of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal integrator circuit will saturate to the supply rails depending on the polarity of the input offset voltage and requires the addition of a feedback resistor, R_2, to provide a stable DC operating point. The feedback resistor limits the lower frequency range over which the integration function is performed. This circuit is most commonly used as part of a larger feedback/servo loop which provides the DC feedback path, thus removing the requirement for a feedback resistor.



Design Notes

1. Use as large of a value as practical for the feedback resistor.
2. Select a CMOS op amp to minimize the errors from the input bias current.
3. The gain bandwidth product (GBP) of the amplifier will set the upper frequency range of the integrator function. The effectiveness of the integration function is usually reduced starting about one decade away from the amplifier bandwidth.
4. An adjustable reference needs to be connected to the non-inverting input of the op amp to cancel the input offset voltage or the large DC noise gain will cause the circuit to saturate. Op amps with very low offset voltage may not require this.

Design Steps

The ideal circuit transfer function is given below.

$$V_{out} = -\frac{1}{R_1 \times C_1}\int_0^t V_{in}(t)\, d\, t$$

1. Set R_1 to a standard value.

   $$R_1 = 100k\Omega$$

2. Calculate C_1 to set the unity-gain integration frequency.

   $$C_1 = \frac{1}{2 \times \pi \times R_1 \times f_{0dB}} = \frac{1}{2 \times \pi \times 100k\Omega \times 1\ \ kHz} = 1.59nF$$

3. Calculate R_2 to set the lower cutoff frequency a decade less than the minimum operating frequency.

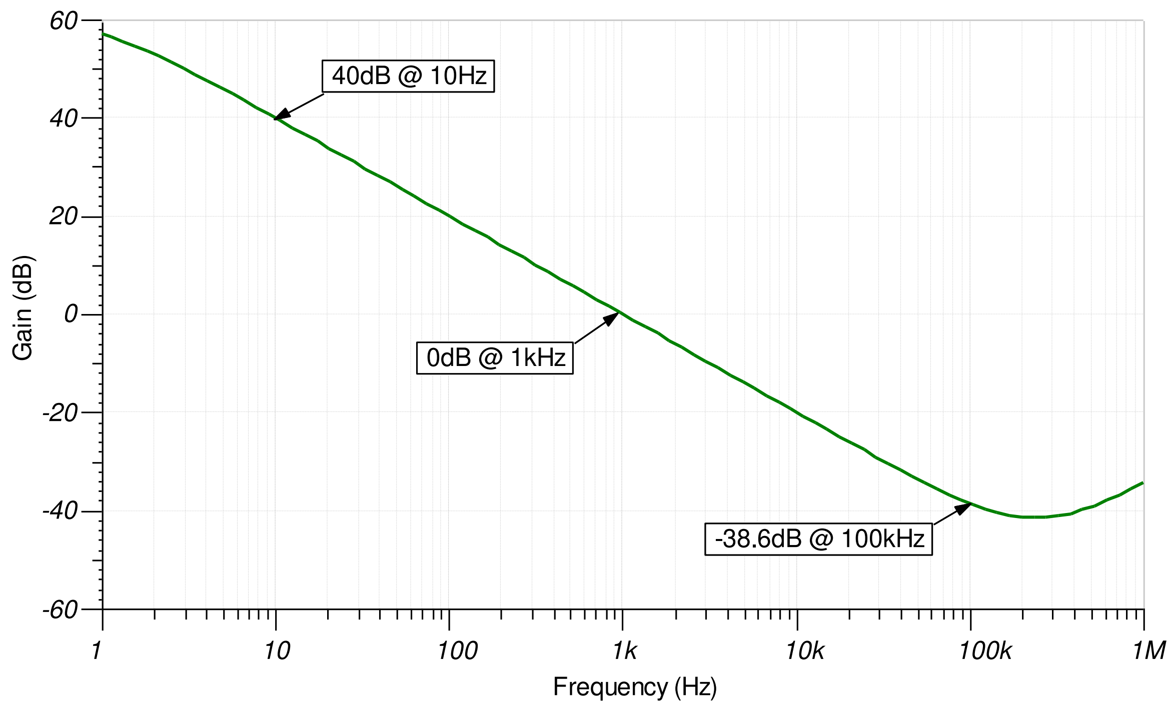
   $$R_2 \geq \frac{10}{2 \times \pi \times C_1 \times f_{Min}} \geq \frac{10}{2 \times \pi \times 1.59nF \times 10Hz} \geq 100M\Omega$$

4. Select an amplifier with a gain bandwidth at least 10 times the desired maximum operating frequency.

   $$GBP \geq 10 \times f_{Max} \geq 10 \times 100kHz \geq 1\ \ MHz$$

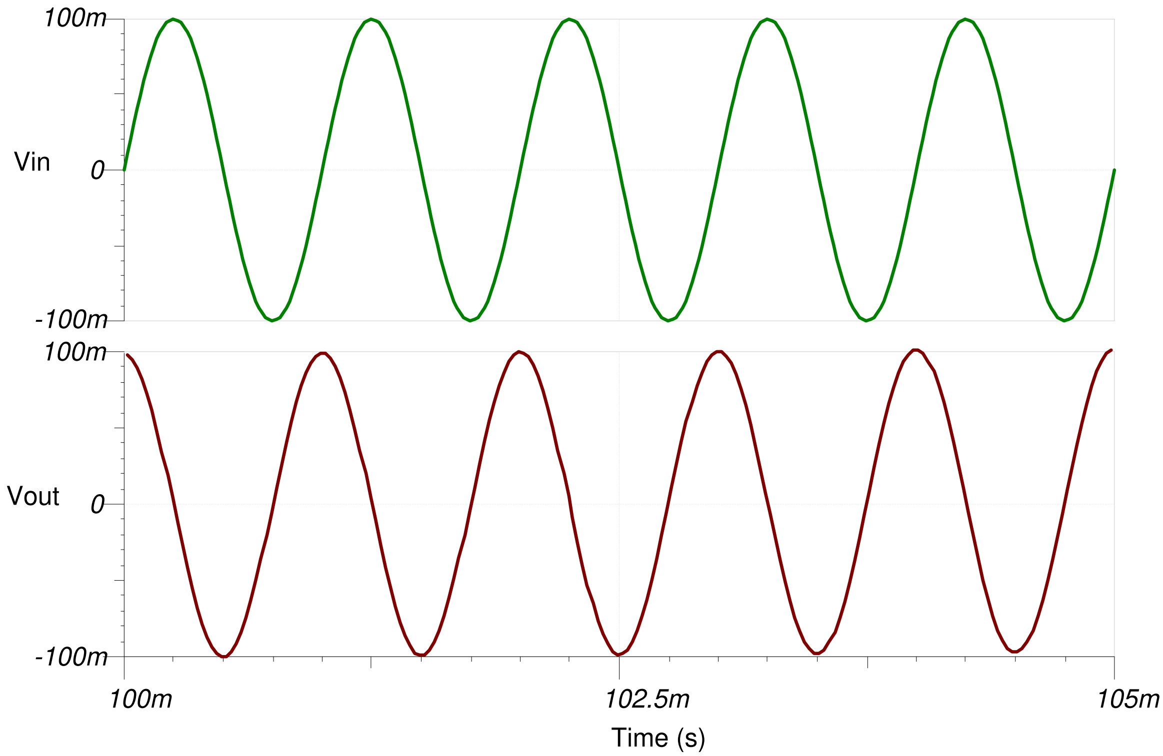
Design Simulations

AC Simulation Results

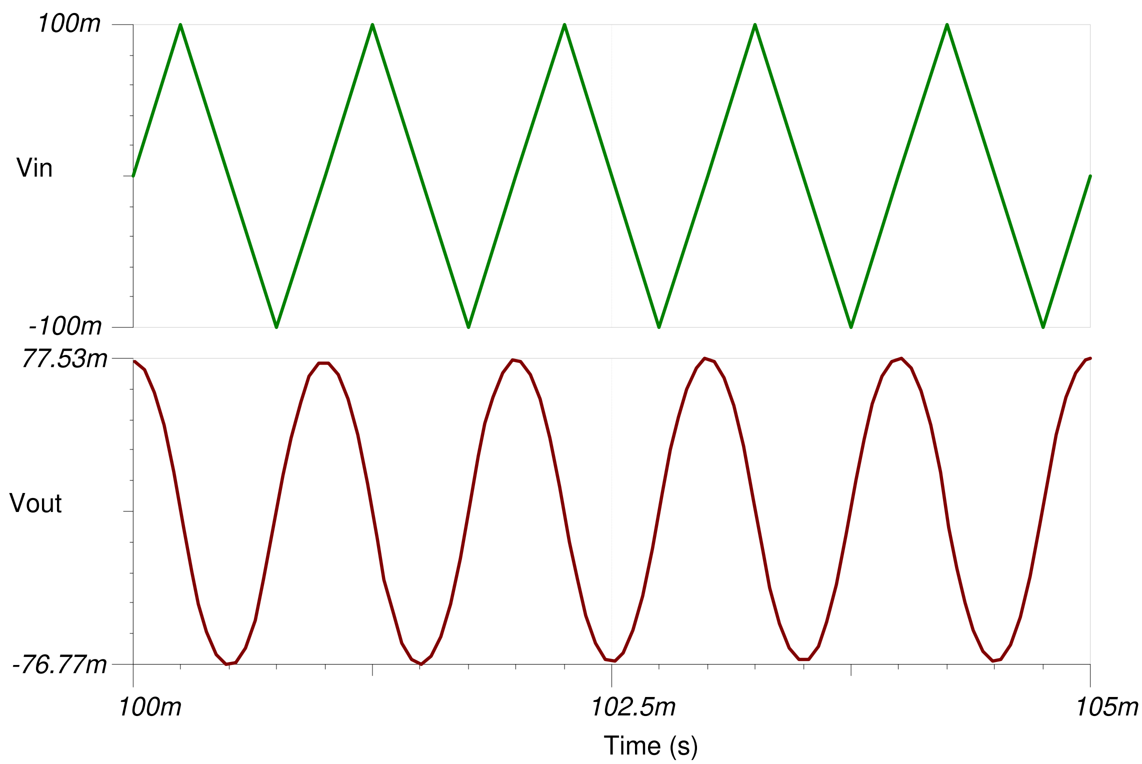


Transient Simulation Results

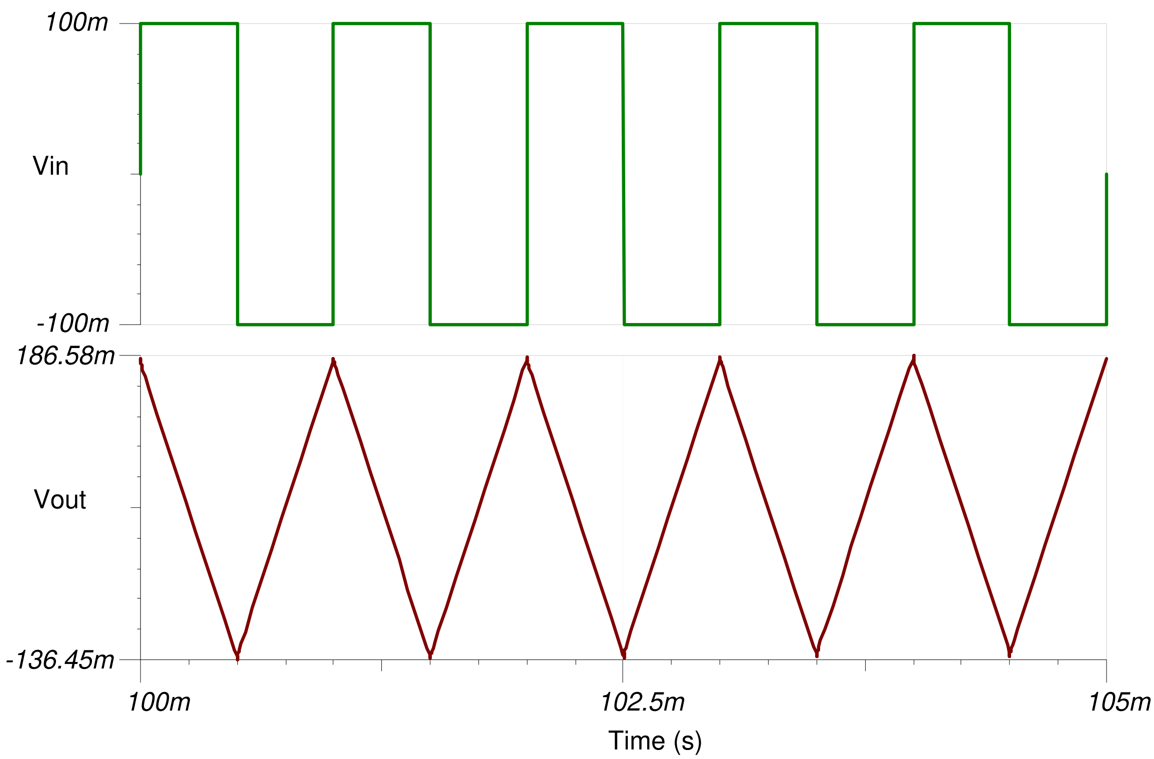
A 1 kHz sine wave input yields a 1 kHz cosine output.



A 1 kHz triangle wave input yields a 1 kHz sine wave output.



A 1 kHz square wave input yields a 1 kHz triangle wave output.



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC496.

See TIPD191.

Design Featured Op Amp

TLV9002	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4 mV
I_q	0.06 mA
I_b	5 pA
UGBW	1 MHz
SR	2 V/µs
#Channels	1, 2, and 4
TLV9002	

Design Alternate Op Amp

OPA376	
V_{cc}	2.2 V to 5.5 V
V_{inCM}	(V_{ee}-0.1 V) to (V_{cc}-1.3 V)
V_{out}	Rail-to-rail
V_{os}	0.005 mV
I_q	0.76 mA
I_b	0.2 pA
UGBW	5.5 MHz
SR	2 V/µs
#Channels	1, 2, and 4
OPA376	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 31, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page	1

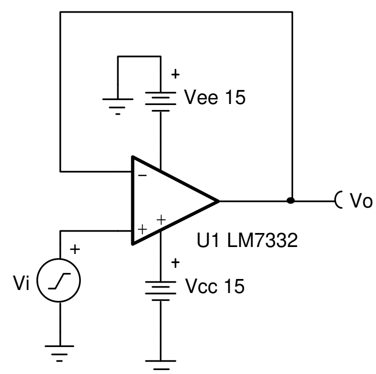
Buffer (Follower) Circuit

Design Goals

Input		Output		Freq.	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
–10 V	10 V	–10 V	10 V	100 kHz	15 V	–15 V

Design Description

This design is used to buffer signals by presenting a high input impedance and a low output impedance. This circuit is commonly used to drive low-impedance loads, analog-to-digital converters (ADC) and buffer reference voltages. The output voltage of this circuit is equal to the input voltage.



Design Notes

1. Use the op-amp linear output operating range, which is usually specified under the A_{OL} test conditions.
2. The small-signal bandwidth is determined by the unity-gain bandwidth of the amplifier.
3. Check the maximum output voltage swing versus frequency graph in the data sheet to minimize slew-induced distortion.
4. The common mode voltage is equal to the input signal.
5. Do not place capacitive loads directly on the output that are greater than the values recommended in the data sheet.
6. High output current amplifiers may be required if driving low impedance loads.
7. For more information on op-amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the *Design References* section.

Design Steps

The transfer function for this circuit follows:

$$V_o = V_i$$

1. Verify that the amplifier can achieve the desired output swing using the supply voltages provided. Use the output swing stated in the A_{OL} test conditions. The output swing range of the amplifier must be greater than the output swing required for the design.

   $$-14V \le V_o \le 14V$$

   - The output swing of the LM7332 using ±15 V supplies is greater than the required output swing of the design. Therefore, this requirement is met.
   - Review the Output Voltage versus Output Current curves in the product data sheet to verify the desired output voltage can be achieved for the desired output current.
2. Verify the input common mode voltage of the amplifier will not be violated using the supply voltage provided. The input common mode voltage range of the amplifier must be greater than the input signal voltage range.

   $$-15.1\ \ V \le V_{icm} \le 15.1\ \ V$$

   - The input common-mode range of the LM7332 using ±15 V supplies is greater than the required input common-mode range of the design. Therefore, this requirement is met.
3. Calculate the minimum slew rate required to minimize slew-induced distortion.

   $$SR > 2 \times \pi \times Vp \times f = 2 \times \pi \times 10V \times 100kHz = 6.28V/\mu s$$

   - The slew rate of the LM7332 is 15.2 V/µs. Therefore, this requirement is met.
4. Verify the device will have sufficient bandwidth for the desired output signal frequency.

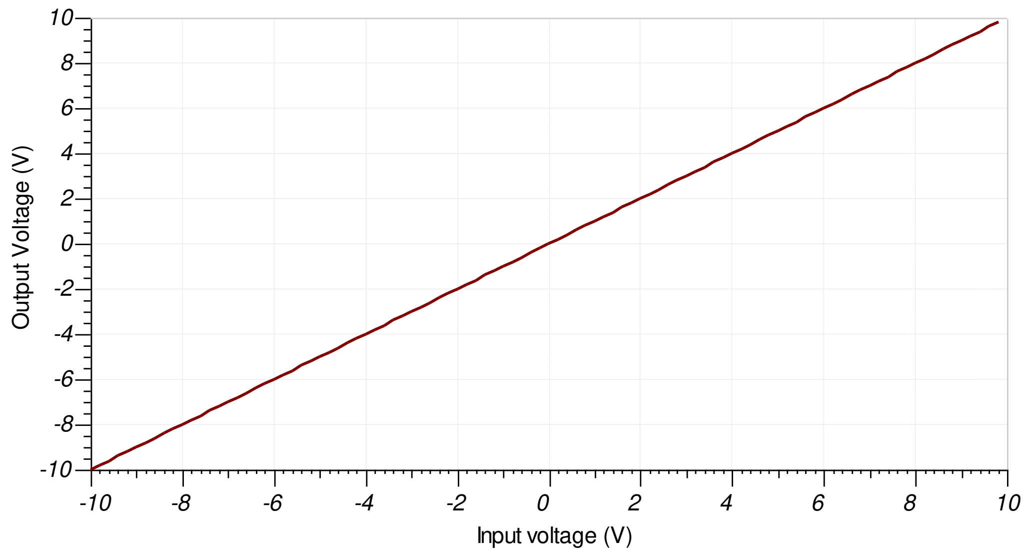
   $$f_{signal} < f_{unity}$$

   $$100kHz \quad < 7.5MHz$$

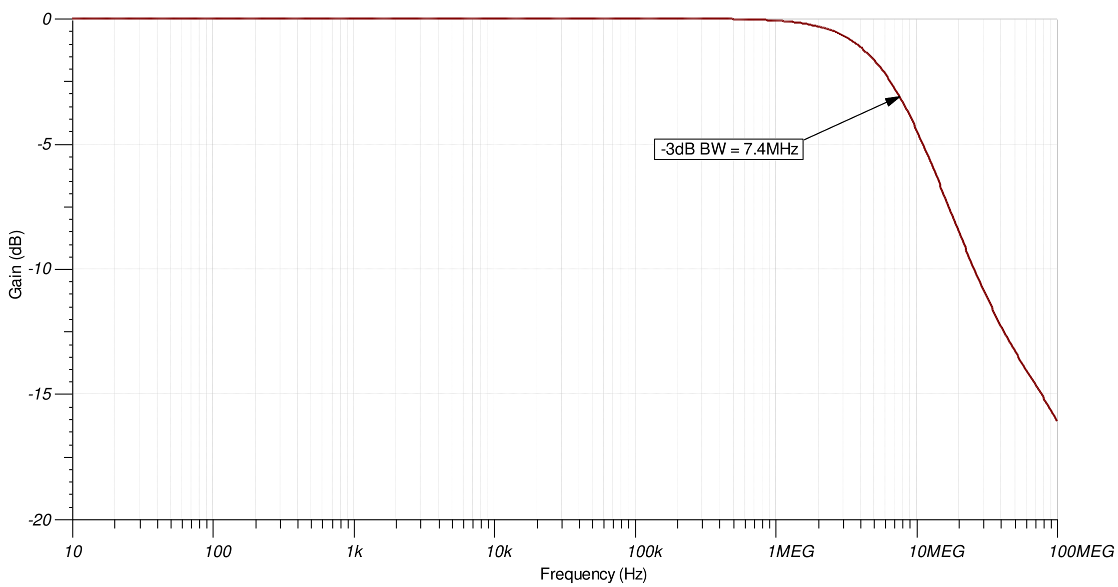
   - The desired output signal frequency is less than the unity-gain bandwidth of the LM7332. Therefore, this requirement is met.

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See the *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

For more information, see the *Capacitive Load Drive Verified Reference Design Using an Isolation Resistor* TI Design.

See the circuit SPICE simulation file SBOC491.

For more information on many op amp topics including common-mode range, output swing, bandwidth, slew rate, and how to drive an ADC, see *TI Precision Labs*.

Design Featured Op Amp

LM7332	
V_{ss}	2.5 V to 32 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1.6 mV
I_q	2 mA
I_b	1 µA
UGBW	7.5 MHz (±5 V supply)
SR	15.2 V/µs
#Channels	2
LM7332	

Design Alternate Op Amp

OPA192	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	1 mA
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA192	

The following device is for battery-operated or power-conscious designs outside of the original design goals described earlier, where lowering the total system power is desired.

LPV511	
V_{ss}	2.7 V to 12 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.2 mV
I_q	1.2 µA
I_b	0.8 nA
UGBW	27 KHz
SR	7.5 V/ms
#Channels	1
LPV511	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 14, 2019 **Page**

- Downscale title. Added LPV511 table in the *Design Alternate Op Amp* section..1

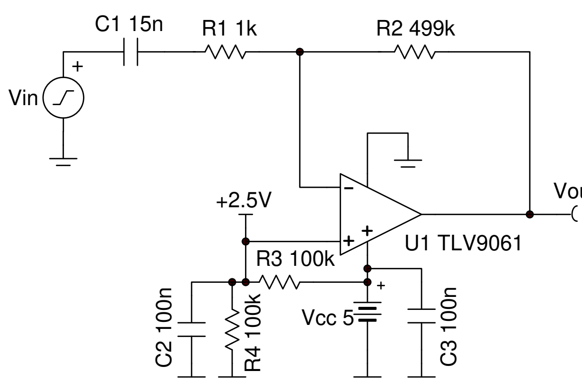
Differentiator Circuit

Design Goals

Input		Output		Supply		
f_{Min}	f_{Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
100Hz	2.5kHz	0.1V	4.9V	5V	0V	2.5V

Design Description

The differentiator circuit outputs the derivative of the input signal over a frequency range based on the circuit time constant and the bandwidth of the amplifier. The input signal is applied to the inverting input so the output is inverted relative to the polarity of the input signal. The ideal differentiator circuit is fundamentally unstable and requires the addition of an input resistor, a feedback capacitor, or both, to be stable. The components required for stability limit the bandwidth over which the differentiator function is performed.



Design Notes

1. Select a large resistance for R_2 to keep the value of C_1 reasonable.
2. A capacitor can be added in parallel with R_2 to filter the high-frequency noise of the circuit. The capacitor will limit the effectiveness of the differentiator function starting about half a decade (approximately 3.5 times) away from the filter cutoff frequency.
3. A reference voltage can be applied to the non-inverting input to set the DC output voltage which allows the circuit to work single-supply. The reference voltage can be derived from a voltage divider.
4. Operate within the linear output voltage swing (see Aol specification) to minimize non-linearity errors.

Design Steps

The ideal circuit transfer function is given below.

$$\text{Vout} \;=\; -R_2 \times C_1 \times \frac{d\,V_{in}(t)}{d\,t}$$

1. Set R_2 to a large standard value.

   $$R_2 = 499\text{k}\Omega$$

2. Set the minimum differentiation frequency at least half a decade below the minimum operating frequency.

   $$C_1 \geq \frac{3.5}{2 \times \pi \times R_2 \times f_{min}} \geq \frac{3.5}{2 \times \pi \times 499\text{k}\Omega \times 100\text{Hz}} \geq 11.1\ \text{nF} \approx 15\text{nF}\ \left(\text{Standard Value}\right)$$

3. Set the upper cutoff frequency at least half a decade above the maximum operating frequency.

   $$R_1 \leq \frac{1}{3.5 \times 2 \times \pi \times C_1 \times f_{Max}} \leq \frac{1}{7 \times \pi \times 15\text{nF} \times 2.5\text{kHz}} \leq 1.2\text{k}\Omega \approx 1\ \text{k}\Omega\ \left(\text{Standard Value}\right)$$

4. Calculate the necessary op amp gain bandwidth product (GBP) for the circuit to be stable.

   $$\text{GBP} > \frac{R_1 + R_2}{2 \times \pi \times {R_1}^2 \times C_1} > \frac{499\text{k}\Omega + 1\ \text{k}\Omega}{2 \times \pi \times 1\ \text{k}\Omega^2 \times 15\text{nF}} > 5.3\text{MHz}$$

   - The bandwidth of the TLV9061 is 10MHz, therefore this requirement is met.

5. If a feedback capacitor, C_F , is added in parallel with R_2, the equation to calculate the cutoff frequency follows.

   $$f_c = \frac{1}{2 \times \pi \times R_2 \times C_F}$$

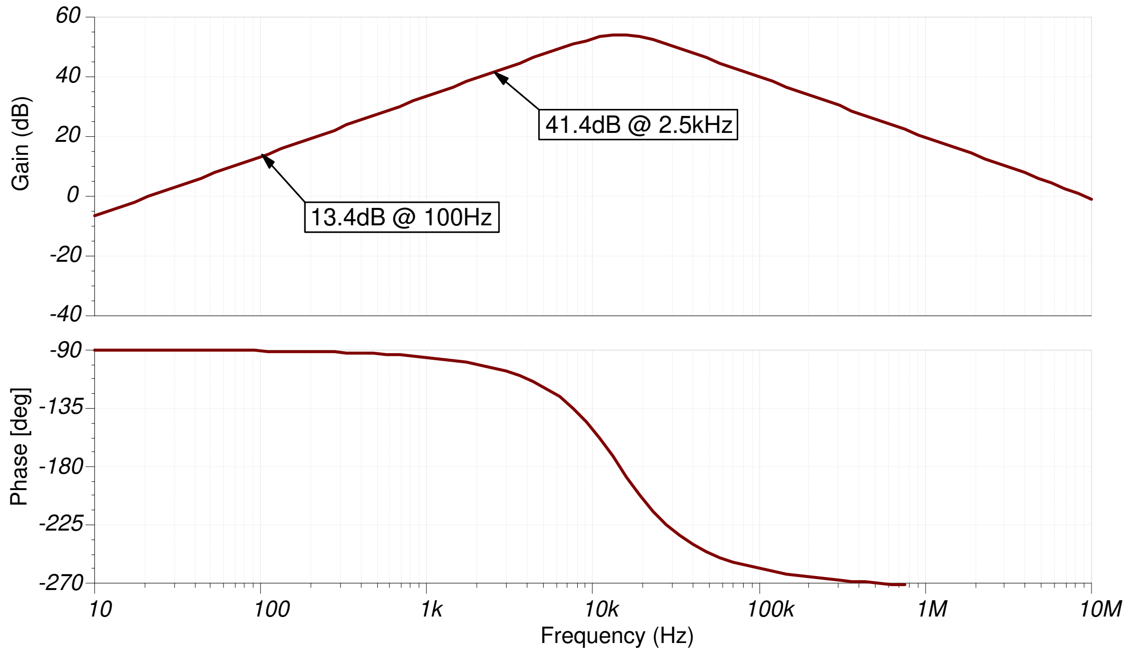
6. Calculate the resistor divider values for a 2.5-V reference voltage.

   $$R_3 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_4 = \frac{5\text{V} - 2.5\text{V}}{2.5\text{V}} \times R_4 = R_4$$

   $$R_3 = R_4 = 100\text{k}\Omega\ \left(\text{Standard Values}\right)$$

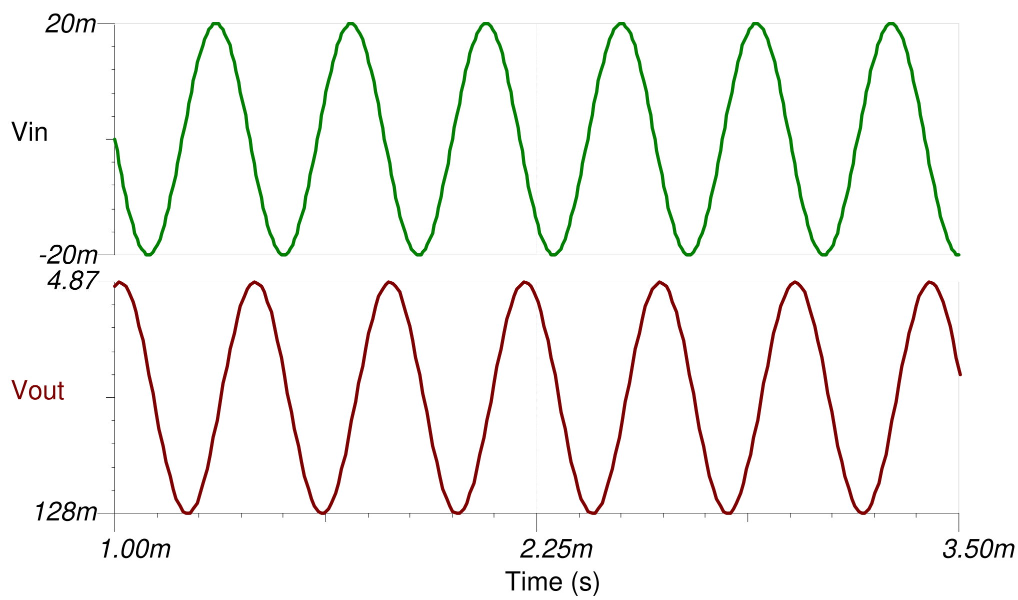
Design Simulations

AC Simulation Results

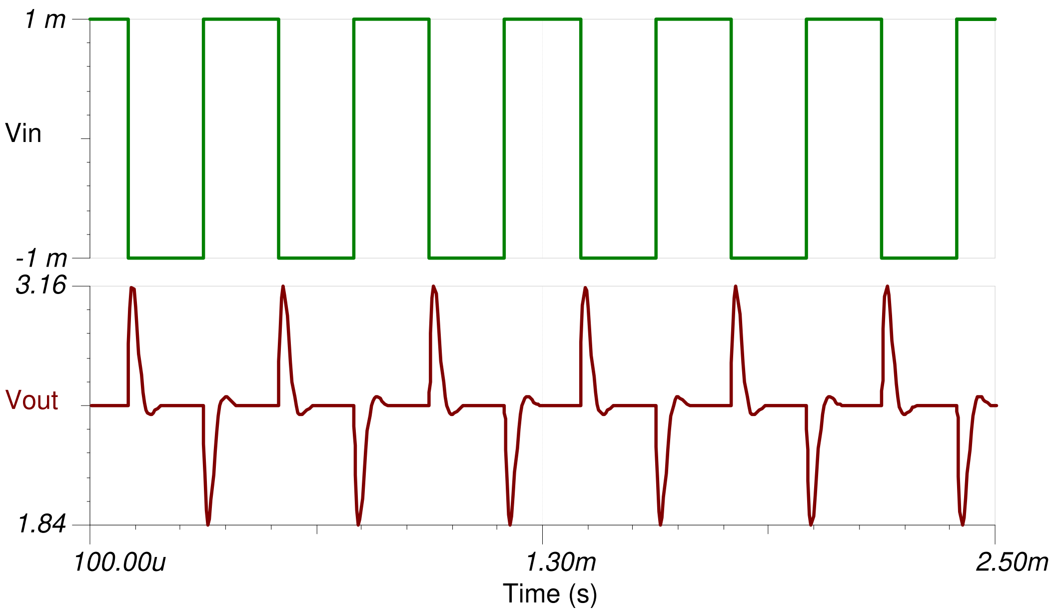


Transient Simulation Results

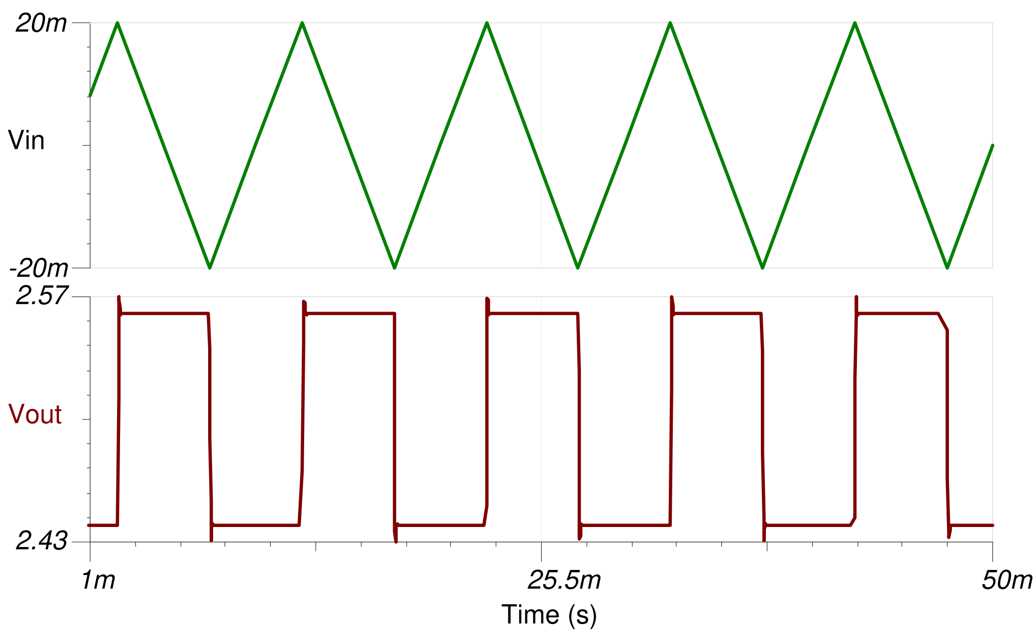
A 2.5-kHz sine wave input yields a 2.5-kHz cosine output.



A 2.5-kHz square wave input produces an impulse output.



A 100-Hz triangle wave input yields a square wave output.



Design Featured Op Amp

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC497.

TLV9061	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	0.538mA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv9061	

Design Alternate Op Amp

OPA374	
V_{cc}	2.3V to 5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1mV
I_q	0.585mA
I_b	0.5pA
UGBW	6.5MHz
SR	0.4V/µs
#Channels	1, 2, 4
www.ti.com/product/opa374	

Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.
B	April 2020	Changed f_{MAX} in the Design Goals from 5kHz to 2.5kHz.
C	August 2021	Updated the numbering format for tables, figures and cross-references throughout the document.

Three Op Amp Instrumentation Amplifier Circuit

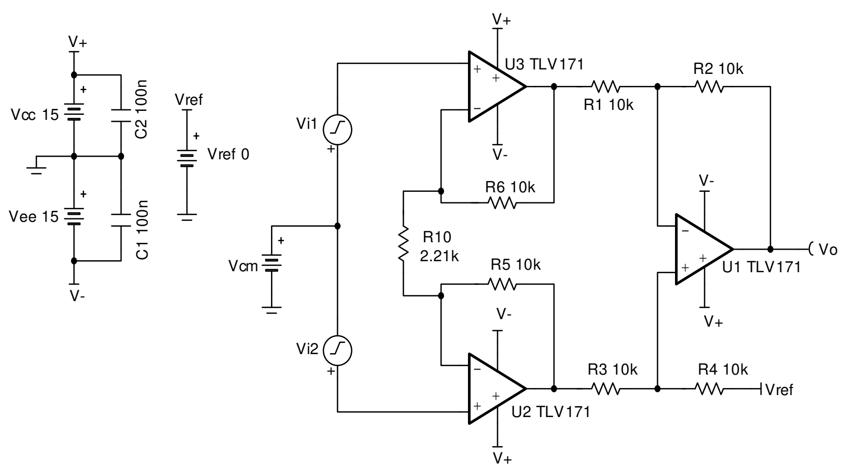
Amplifiers

Design Goals

Input V_{idiff} ($V_{i2} – V_{i1}$)		Common-Mode Voltage	Output		Supply		
$V_{i\ diff\ Min}$	$V_{i\ diff\ Max}$	V_{cm}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
-0.5 V	+0.5 V	±7 V	–5 V	+5 V	+15 V	–15 V	0 V

Design Description

This design uses 3 op amps to build a discrete instrumentation amplifier. The circuit converts a differential signal to a single-ended output signal. Linear operation of an instrumentation amplifier depends upon linear operation of its building block: op amps. An op amp operates linearly when the input and output signals are within the device's input common-mode and output swing ranges, respectively. The supply voltages used to power the op amps define these ranges.



Design Notes

1. Use precision resistors to achieve high DC CMRR performance
2. R_{10} sets the gain of the circuit.
3. Add an isolation resistor to the output stage to drive large capacitive loads.
4. High-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
5. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the A_{ol} test conditions in the op amps data sheets.

Design Steps

1. Transfer function of this circuit:

$$V_O = (V_{i2} - V_{i1}) \times G + V_{ref}$$

When V_{ref} = 0, the transfer function simplifies to the following equation:

$$V_O = (V_{i2} - V_{i1}) \times G$$

where

$$G = \frac{R_4}{R_3} \times \left(1 + \frac{2 \times R_5}{R_{10}}\right)$$

2. Select the feedback loop resistors R_5 and R_6:

$$\text{Choose } R_5 = R_6 = 10\,k\Omega \text{ (Standard Value)}$$

3. Select R_1, R_2, R_3, R_4. To set the Vref gain at 1 V/V and avoid degrading the instrumentation amplifier's CMRR, ratios of R_4/R_3 and R_2/R_1 must be equal.

$$\text{Choose } R_1 = R_2 = R_3 = R_4 = 10\,k\Omega \text{ (Standard Value)}$$

4. Calculate R_{10} to meet the desired gain:

$$G = \frac{R_4}{R_3} \times \left(1 + \frac{2 \times R_5}{R_{10}}\right) = 10\ \frac{V}{V}$$

$$R_4 = R_3 = 10\,k\Omega$$

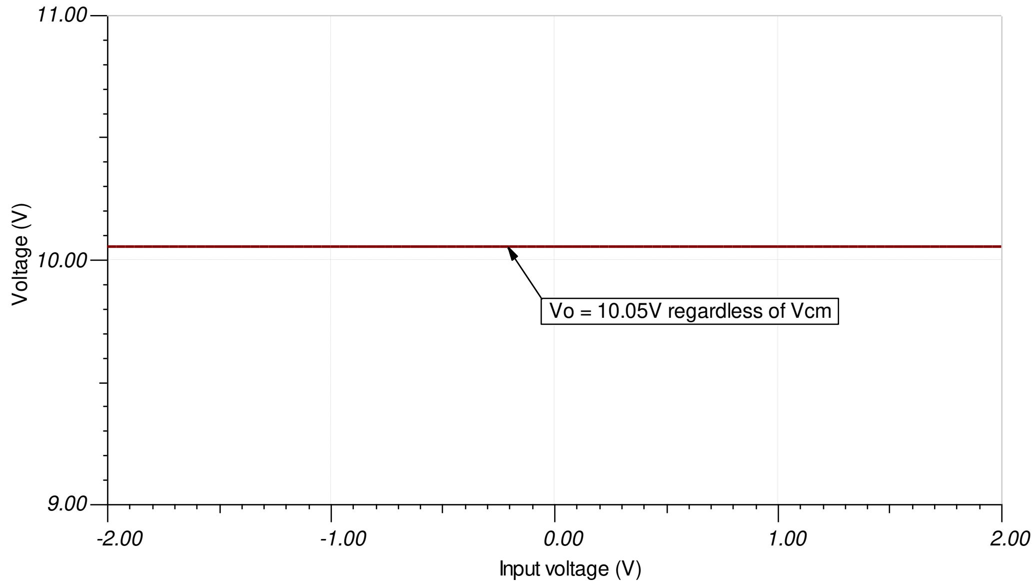
$$\rightarrow G = \left(1 + \frac{2 \times 10\,k\Omega}{R_{10}}\right) = 10\ \frac{V}{V} \rightarrow \left(1 + \frac{20\,k\Omega}{R_{10}}\right) = 10\ \frac{V}{V}$$

$$\frac{20\,k\Omega}{R_{10}} = 9\ \frac{V}{V} \rightarrow R_{10} = \frac{20\,k\Omega}{9} = 2222.2\Omega \rightarrow R_{10} = 2.21k\Omega\ \text{(Standard Value)}$$

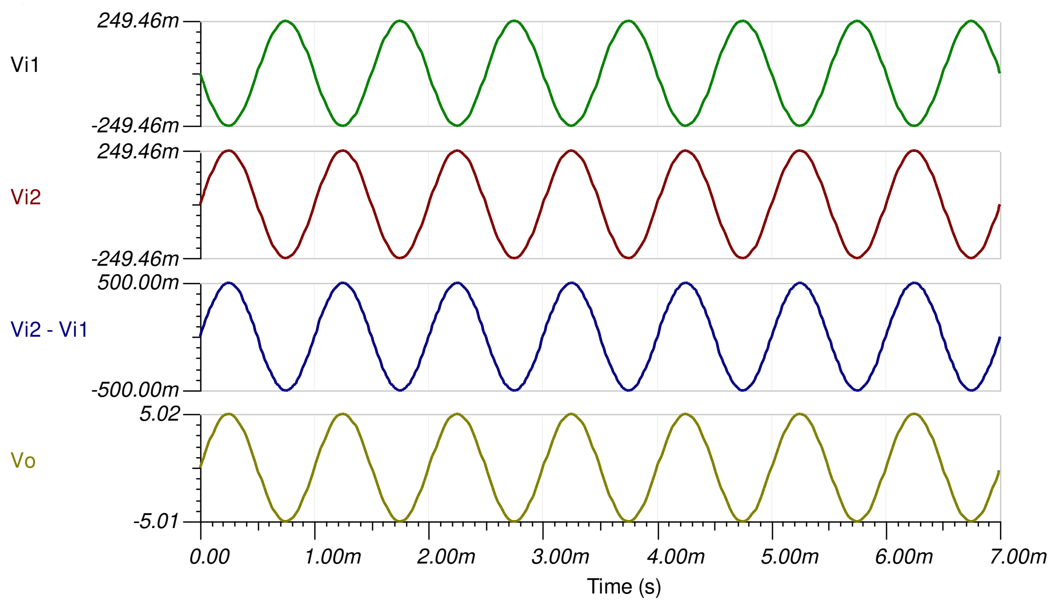
5. To check the common-mode voltage range, download and install the program from reference [5]. Edit the INA_Data.txt file in the installation directory by adding the code for a 3 op amp INA whose internal amplifiers have the common-mode range, output swing, and supply voltage range as defined by the amplifier of choice (TLV172, in this case). There is no V_{be} shift in this design and the gain of the output stage difference amplifeir is 1 V/V. The default supply voltage and reference voltages are ±15 V and 0 V, respectively. Run the program and set the gain and reference voltage accordingly. The resulting V_{CM} vs. V_{OUT} plot approximates the linear operating region of the discrete INA.

Design Simulations

DC Simulation Results



Transient Simulation Results



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOMAU8
3. TI Precision Labs
4. Instrumentation Amplifier V_{CM} vs. V_{OUT} Plots
5. Common-mode Range Calculator for Instrumentation Amplifiers

Design Featured Op Amp

TLV171	
V_{ss}	4.5 V to 36 V
V_{inCM}	(V–) – 0.1 V < Vin < (V+) – 2 V
V_{out}	Rail–to–rail
V_{os}	0.25 mV
I_q	475 µA
I_b	8 pA
UGBW	3 MHz
SR	1.5 V/µs
#Channels	1,2, and4
TLV171	

Design Alternate Op Amp

	OPA172	OPA192
V_{ss}	4.5 V to 36 V	4.5 V to 36 V
V_{inCM}	(V–) – 0.1 V < Vin < (V+) – 2 V	V_{ee}–0.1 V to V_{cc}+0.1 V
V_{out}	Rail–to–rail	Rail–to–rail
V_{os}	0.2 mV	±5 µV
I_q	1.6 mA	1 mA/Ch
I_b	8 pA	5 pA
UGBW	10 MHz	10 MHz
SR	10 V/µs	20 V/µs
#Channels	1, 2, and 4	1, 2, and 4
	OPA172	OPA192

Analog Engineer's Circuit

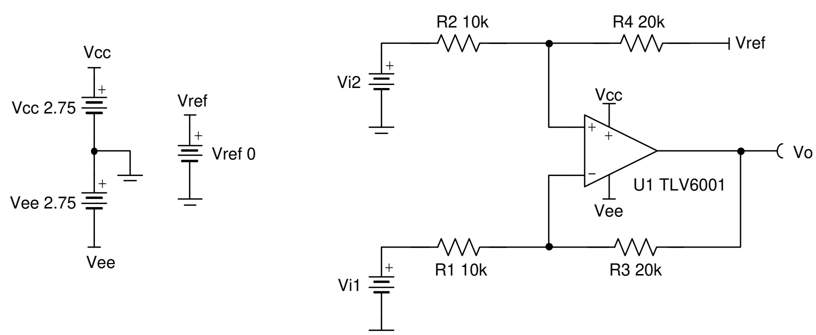
Difference Amplifier (Subtractor) Circuit

Design Goals

Input (V_{i2}-V_{i1})		Output		CMRR (min)	Supply		
$V_{idiffMin}$	$V_{idiffMax}$	V_{oMin}	V_{oMax}	dB	V_{cc}	V_{ee}	V_{ref}
–1.25 V	1.25 V	–2.5 V	2.5 V	50	2.75 V	–2.75 V	0 V

Design Description

This design inputs two signals, V_{i1} and V_{i2}, and outputs their difference (subtracts). The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the resistive network. Difference amplifiers are typically used to amplify differential input signals and reject common-mode voltages. A common-mode voltage is the voltage common to both inputs. The effectiveness of the ability of a difference amplifier to reject a common-mode signal is known as common-mode rejection ratio (CMRR). The CMRR of a difference amplifier is dominated by the tolerance of the resistors.



Design Notes

1. Use the op amp in a linear operating region. Ensure that the inputs of the op amp do not exceed the common-mode range of the device. Linear output swing is usually specified under the A_{OL} test conditions.
2. The input impedance is determined by the input resistive network. Make sure these values are large when compared to the output impedance of the sources.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitors in parallel to R_3 and R_4. Adding capacitors in parallel with R_3 and R_4 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The complete transfer function for this circuit is shown below.

$$V_o = V_{i\,1} \times \left(-\frac{R_3}{R_1}\right) + V_{i\,2} \times \left(\frac{R_4}{R_2 + R_4}\right) \times \left(1 + \frac{R_3}{R_1}\right) + Vref \times \left(\frac{R_2}{R_2 + R_4}\right) \times \left(1 + \frac{R_3}{R_1}\right)$$

If $R_1 = R_2$ and $R_3 = R_4$ the transfer function for this circuit simplifies to the following equation.

$$V_o = (V_{i\,2} - V_{i\,1}) \times \frac{R_3}{R_1} + Vref$$

- Where the gain, G, is R_3/R_1.

1. Determine the starting value of R_1 and R_2. The relative size of R_1 and R_2 to the signal impedance of the source affects the gain error.

$$R_1 = R_2 = 10k\Omega$$

2. Calculate the gain required for the circuit.

$$G = \frac{V_{oMax} - V_{oMin}}{V_{idiffMax} - V_{idiffMin}} = \frac{2.5V - (-2.5V)}{1.25V - (-1.25V)} = 2\frac{V}{V} = 6.02dB$$

3. Calculate the values for R_3 and R_4.

$$G = 2\frac{V}{V} = \frac{R_3}{R_1} \rightarrow 2 \times R_1 = R_3 = R_4 = 20k\Omega$$

4. Calculate resistor tolerance to meet the minimum common-mode rejection ratio (CMRR). For minimum (worst-case) CMRR, α = 4. For a more probable, or typical value of CMRR, α = 0.33.

$$CMRR_{dB} \cong 20\log 10\left(\frac{1 + G}{\alpha \times \varepsilon}\right)$$

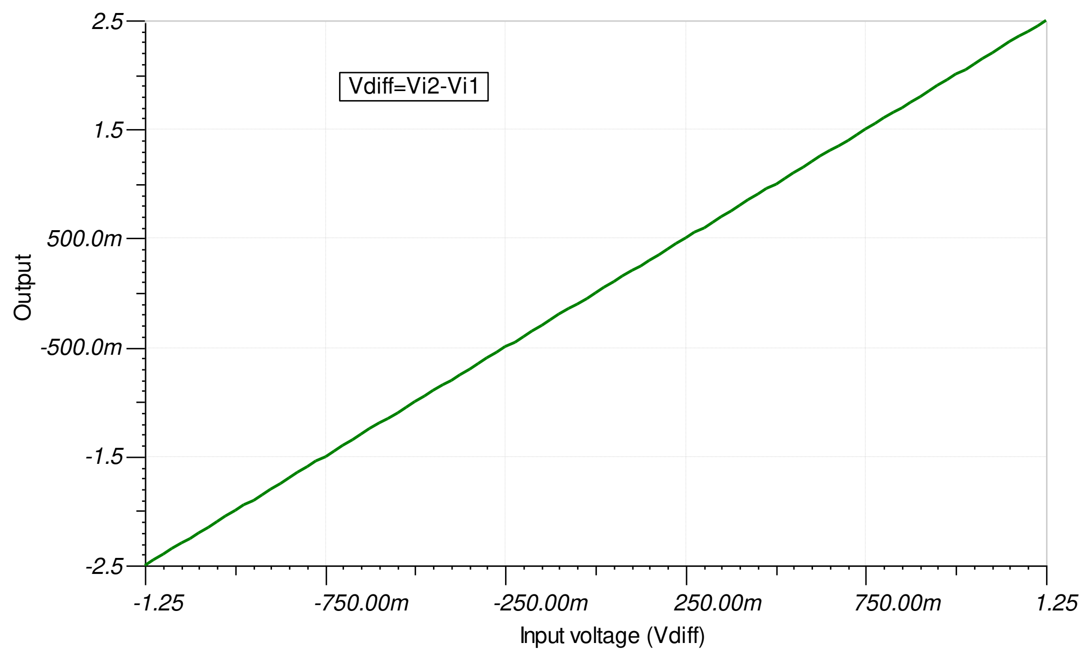
$$\varepsilon = \frac{1 + G}{\alpha \times 10^{\left(\frac{CMRR_{dB}}{20}\right)}} = \frac{3}{4 \times 10^{\left(\frac{50}{20}\right)}} = 0.024 = 0.24\% \rightarrow \text{Use } 0.1\% \text{ resistors}$$

5. For quick reference, the following table compares resistor tolerance to minimum and typical CMRR values assuming G = 1 or G = 2. As shown above, as gain increases so does CMRR.

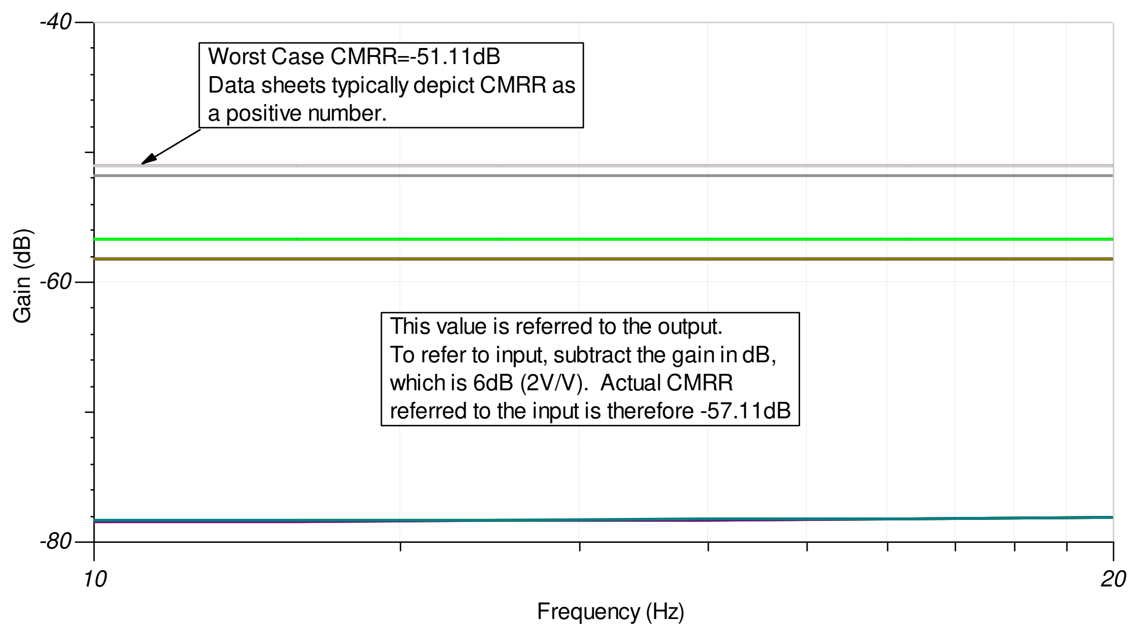
Tolerance	G=1 Minimum (dB)	G=1 Typical (dB)	G=2 Minimum (dB)	G=2 Typical (dB)
0.01%=0.0001	74	95.6	77.5	99.2
0.1%=0.001	54	75.6	57.5	79.2
0.5%=0.005	40	61.6	43.5	65.2
1%=0.01	34	55.6	37.5	59.2
5%=0.05	20	41.6	23.5	45.2

Design Simulations

DC Simulation Results



CMRR Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC495.

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs. For more information on difference amplifier CMRR, please read *Overlooking the obvious: the input impedance of a difference amplifier*.

Design Featured Op Amp

TLV6001	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	750 µV
I_q	75 µA
I_b	1 pA
UGBW	1 MHz
SR	0.5 V/µs
#Channels	1, 2, and 4
TLV6001	

Design Alternate Op Amp

OPA320	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40 µV
I_q	1.5 mA
I_b	0.2 pA
UGBW	20 MHz
SR	10 V/µs
#Channels	1 and 2
OPA320	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 31, 2019 **Page**

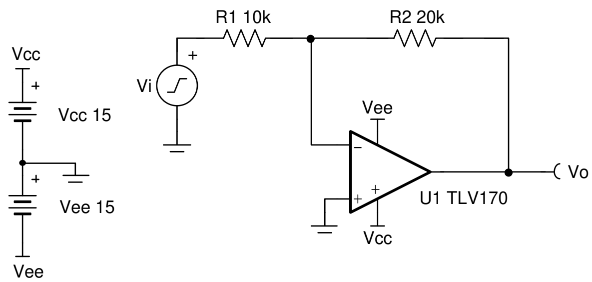
Inverting Amplifier Circuit

Design Goals

Input		Output		Freq.	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
–7V	7V	–14V	14V	3kHz	15V	–15V

Design Description

This design inverts the input signal, V_i, and applies a signal gain of –2V/V. The input signal typically comes from a low-impedance source because the input impedance of this circuit is determined by the input resistor, R_1. The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistor. Make sure this value is large when compared to the source output impedance.
3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_2. Adding a capacitor in parallel with R_2 improves stability of the circuit if high value resistors are used.
6. Large signal performance can be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the Design References section.

Design Steps

The transfer function of this circuit follows:

$$V_o = V_i \times \left(-\frac{R_2}{R_1}\right)$$

1. Determine the starting value of R_1. The relative size of R_1 to the signal source impedance affects the gain error. Assuming the impedance from the signal source is low (for example, 100Ω), set R_1 = 10kΩ for 1% gain error.

   $$R_1 = 10\ k\Omega$$

2. Calculate the gain required for the circuit. Since this is an inverting amplifier, use V_{iMin} and V_{oMax} for the calculation.

   $$G = \frac{V_{oMax}}{V_{iMin}} = \frac{14\ V}{-7\ V} = -2\frac{V}{V}$$

3. Calculate R_2 for a desired signal gain of –2 V/V.

   $$G = -\frac{R_2}{R_1} \rightarrow R_2 = -G \times R_1 = -\left(-2\frac{V}{V}\right) \times 10\ k\Omega = 20\ k\Omega$$

4. Calculate the small signal circuit bandwidth to ensure it meets the 3-kHz requirement. Be sure to use the noise gain, or non-inverting gain, of the circuit.

   $$GBP_{TLV\ 170} = 1.2\ MHz$$

   $$NG = \left(1 + \frac{R_2}{R_1}\right) = 3\frac{V}{V}$$

   $$BW = \frac{GBP}{NG} = \frac{1.2\ MHz}{3\ V/V} = 400\ kHz$$

5. Calculate the minimum slew rate required to minimize slew-induced distortion.

   $$V_p = \frac{SR}{2 \times \pi \times f} \rightarrow SR > 2 \times \pi \times f \times V_p$$

   $$SR > 2 \times \pi \times 3\ kHz \times 14\ V = 263.89\frac{kV}{s} = 0.26\frac{V}{\mu s}$$

   - SR_{TLV170} = 0.4V/µs, therefore, it meets this requirement.
6. To avoid stability issues, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

   $$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_2 \parallel R_1)} > \frac{GBP}{NG}$$

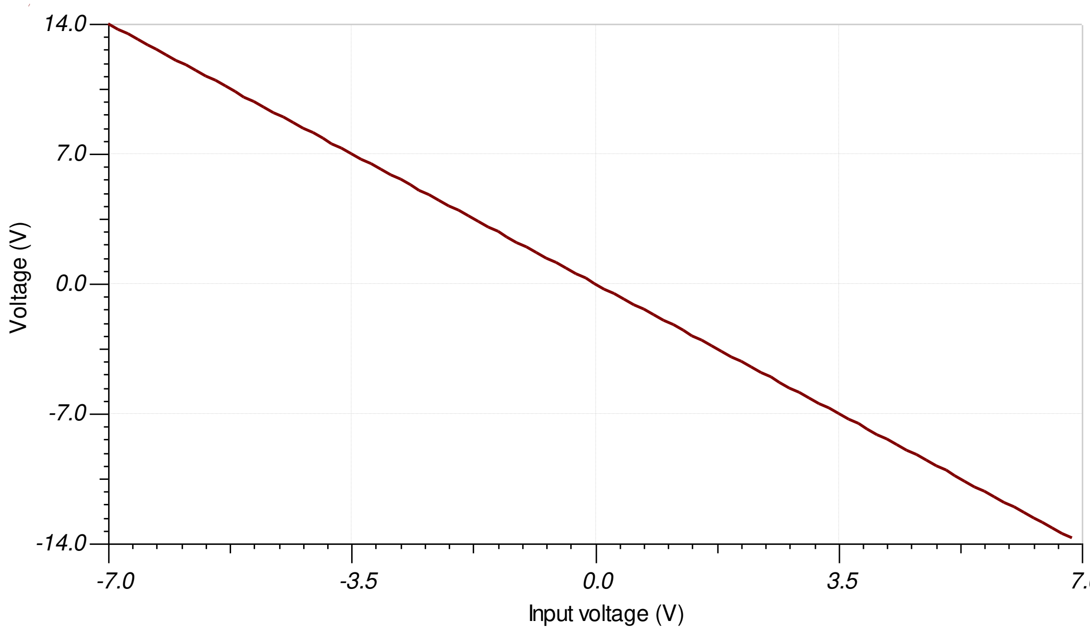
   $$\frac{1}{2 \times \pi \times (3\ pF + 3\ pF) \times \frac{20\ k\Omega \times 10\ k\Omega}{20\ k\Omega + 10\ k\Omega}} > \frac{1.2\ MHz}{3\ V/V}$$

   $$3.97\ MHz > 400\ kHz$$

- C_{cm} and C_{diff} are the common-mode and differential input capacitance of the TLV170, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

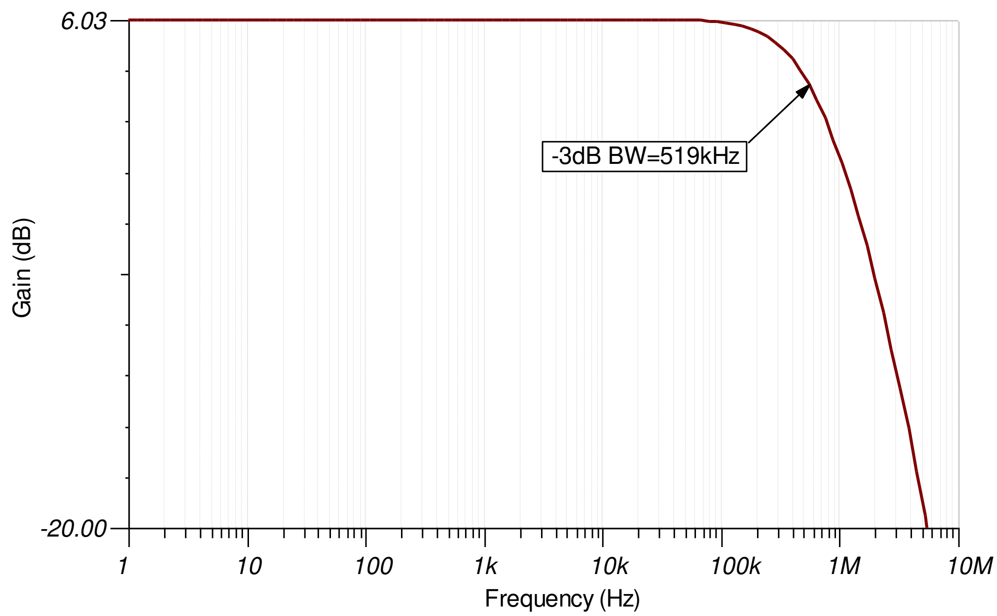
Design Simulations

DC Simulation Results



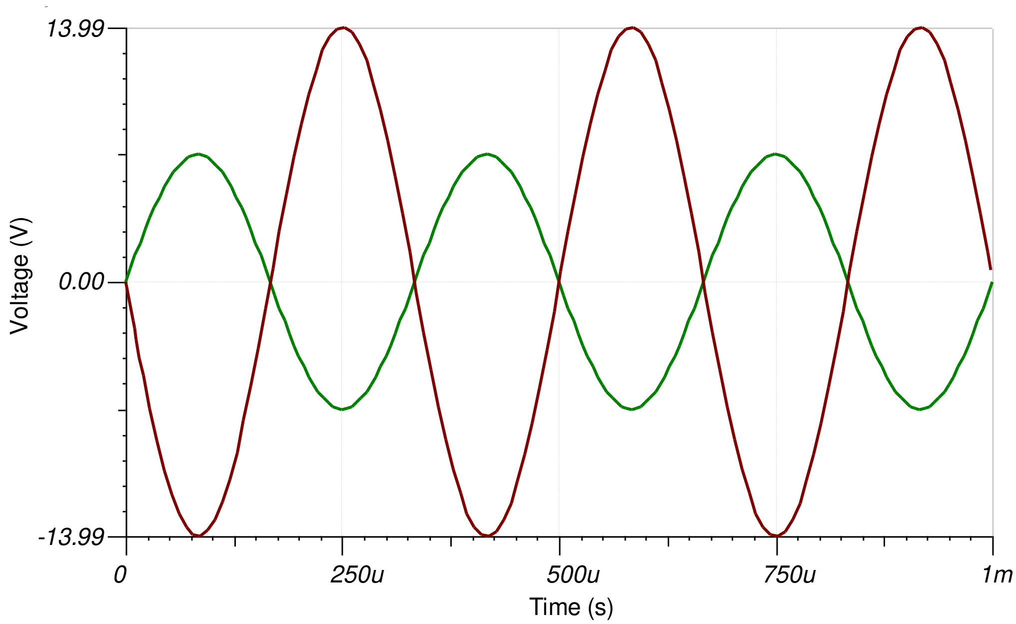
AC Simulation Results

The bandwidth of the circuit depends on the noise gain, which is 3V/V. The bandwidth is determined by looking at the –3-dB point, which is located at 3dB given a signal gain of 6dB. The simulation sufficiently correlates with the calculated value of 400kHz.



Transient Simulation Results

The output is double the magnitude of the input and inverted.



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOC492
3. TI Precision Labs

Design Featured Op Amp

TLV170	
V_{ss}	±18 V (36 V)
V_{inCM}	(Vee-0.1 V) to (Vcc-2 V)
V_{out}	Rail-to-rail
V_{os}	0.5 mV
I_q	125 µA
I_b	10 pA
UGBW	1.2 MHz
SR	0.4 V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv170	

Design Alternate Op Amp

LMV358A	
V_{ss}	2.5 V to 5.5 V
V_{inCM}	(V_{ee}–0.1 V) to (V_{cc}–1 V)
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	70 µA
I_b	10 pA
UGBW	1 MHz
SR	1.7 V/µs
#Channels	1 (LMV321A), 2 (LMV358A), 4 (LMV324A)
www.ti.com/product/lmv358A	

Revision History

Revision	Date	Change
C	December 2020	Updated result for Design Step 6.
B	March 2019	Changed LMV358 to LMV358A in the Design Alternate Op Amp section.
A	January 2019	Downstyle title. Added link to circuit cookbook landing page.

Application Note

Two op amp instrumentation amplifier circuit

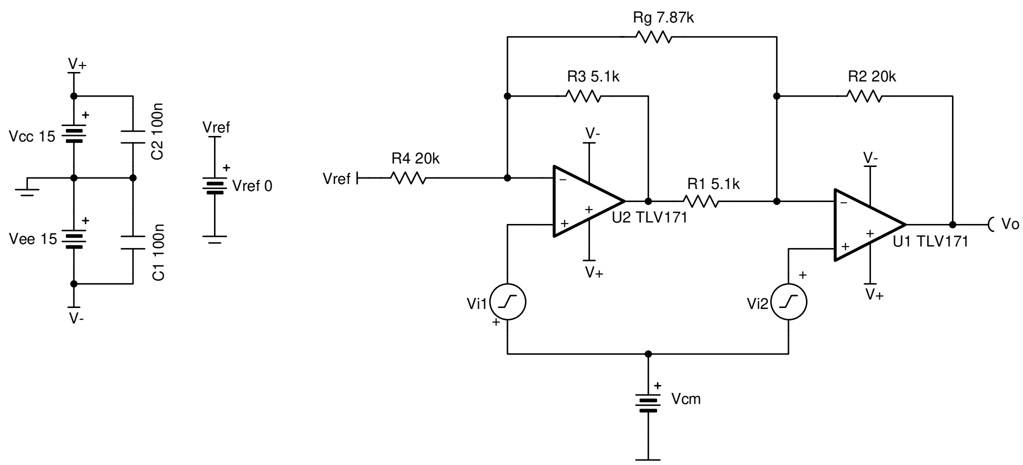
Design Goals

Input $V_{iDiff}(V_{i2} - V_{i1})$		Output		Supply		
V_{iDiff_Min}	V_{iDiff_Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
+/–1V	+/–2V	–10V	+10V	15V	–15V	0V

V_{cm}	Gain Range
+/-10V	5V/V to 10V/V

Design Description

This design amplifiers the difference between V_{i1} and V_{i2} and outputs a single ended signal while rejecting the common–mode voltage. Linear operation of an instrumentation amplifier depends upon the linear operation of its primary building block: op amps. An op amp operates linearly when the input and output signals are within the device's input common–mode and output–swing ranges, respectively. The supply voltages used to power the op amps define these ranges.



Design Notes

1. R_g sets the gain of the circuit.
2. High–value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
3. The ratio of R_4 and R_3 set the minimum gain when R_g is removed.
4. Ratios of R_2/R_1 and R_4/R_3 must be matched to avoid degrading the instrumentation amplifier's DC CMRR and ensuring the V_{ref} gain is 1V/V.
5. Linear operation is contingent upon the input common–mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the A_{ol} test conditions in the op amps data sheets.

Design Steps

1. Transfer function of this circuit.

$$V_o = V_{iDiff} \times G + V_{ref} = \left(V_{i2} - V_{i1}\right) \times G + V_{ref}$$

when $V_{ref} = 0$, the transfer function simplifies to the following equation:

$$V_o = \left(V_{i2} - V_{i1}\right) \times G$$

where G is the gain of the instrumentation amplifier and $G = 1 + \frac{R_4}{R_3} + \frac{2R_2}{R_g}$

2. Select R_4 and R_3 to set the minimum gain.

$$G_{min} = 1 + \frac{R_4}{R_3} = 5\frac{V}{V}$$

Choose $R_4 = 20k\Omega$

$$G_{min} = 1 + \frac{20k\Omega}{R_3} = 5\frac{V}{V}$$

$$R_3 = \frac{R_4}{5-1} = \frac{20k\Omega}{4} = 5k\Omega \rightarrow R_3 = 5.1k\Omega \ \left(\text{Standard Value}\right)$$

3. Select R_1 and R_2. Ensure that R_1/R_2 and R_3/R_4 ratios are matched to set the gain applied to the reference voltage at 1V/V.

$$\frac{V_{o\_ref}}{Vref} = \left(-\frac{R_3}{R_4}\right) \times \left(-\frac{R_2}{R_1}\right) = \frac{R_3 \times R_2}{R_4 \times R_1} = 1\frac{V}{V}$$

$$\frac{R_2}{R_1} = \frac{R_4}{R_3} \rightarrow R_1 = R_3 = 5.1k\Omega \text{ and } R_2 = R_4 = 20k\Omega \ \left(\text{Standad Value}\right)$$

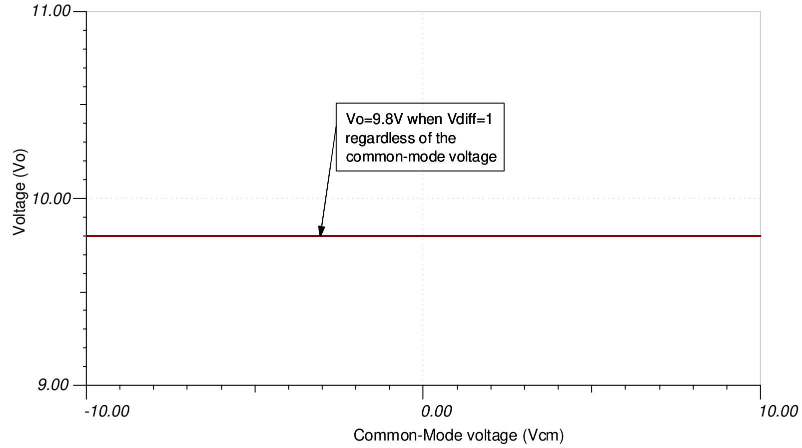
4. Select R_g to meet the desired maximum gain G = 10V/V.

$$G = 1 + \frac{R_4}{R_3} + \frac{2R_2}{R_g} = 1 + \frac{20\ k\Omega}{5.1\ k\Omega} + \frac{2 \times 20\ k\Omega}{R_g} = 10\ V/V$$

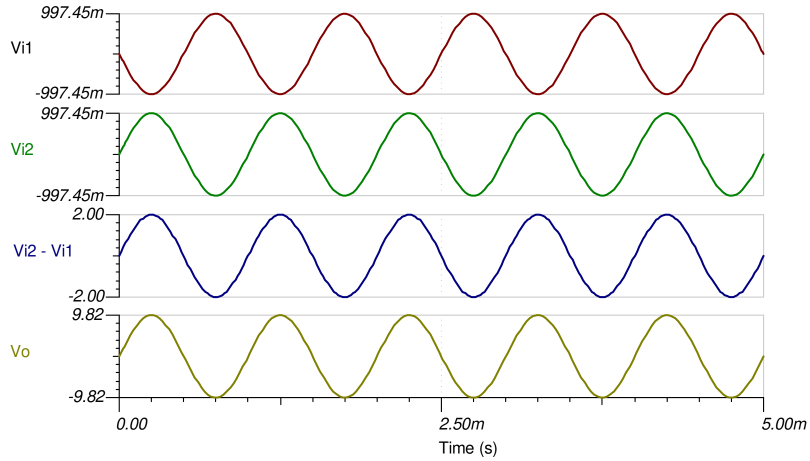
$$R_g = 8\ k\Omega \rightarrow R_g = 7.87\ k\Omega \ \left(\text{Standard Value}\right)$$

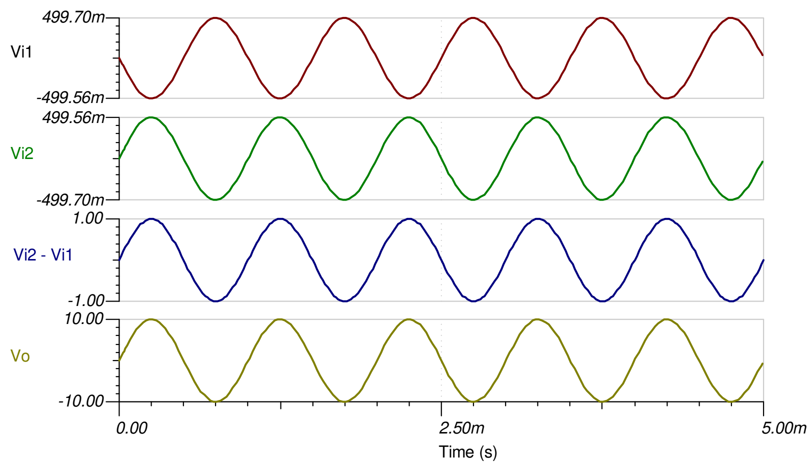
Design Simulations

DC Simulation Results



Transient Simulation Results





References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOMAU7
3. TI Precision Labs
4. *V_{CM} vs. V_{OUT} plots for instrumentation amplifiers with two op amps*
5. Common-mode Range Calculator for Instrumentation Amplifiers

Design Featured Op Amp

TLV171	
V_{ss}	4.5V to 36V
V_{inCM}	(V_{ee}–0.1V) to (V_{cc}–2V)
V_{out}	Rail–to–rail
V_{os}	0.25mV
I_q	475µA
I_b	8pA
UGBW	3MHz
SR	1.5V/µs
#Channels	1,2,4
www.ti.com/product/tlv171	

Design Alternate Op Amp

OPA172	
V_{ss}	4.5V to 36V
V_{inCM}	(V_{ee}–0.1V) to (V_{cc}–2V)
V_{out}	Rail–to–rail
V_{os}	0.2mV
I_q	1.6mA
I_b	8pA
UGBW	10MHz
SR	10V/µs
#Channels	1,2,4
www.ti.com/product/opa172	

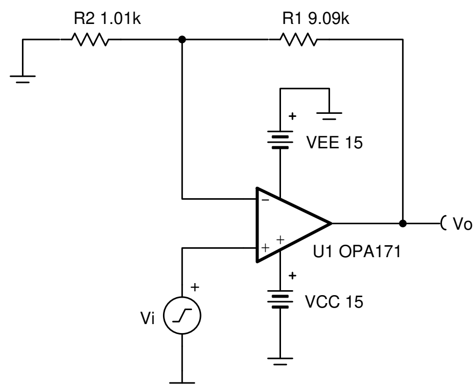
Non-Inverting Amplifier Circuit

Design Goals

Input		Output		Supply	
ViMin	ViMax	VoMin	VoMax	Vcc	Vee
–1 V	1 V	–10 V	10 V	15 V	–15 V

Design Description

This design amplifies the input signal, V_i, with a signal gain of 10 V/V. The input signal may come from a high-impedance source (for example, MΩ) because the input impedance of this circuit is determined by the extremely high input impedance of the op amp (for example, GΩ). The common-mode voltage of a non-inverting amplifier is equal to the input signal.



Design Notes

1. Use the op amp linear output operating range, which is usually specified under the A_{OL} test conditions. The common-mode voltage is equal to the input signal.
2. The input impedance of this circuit is equal to the input impedance of the amplifier.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. The small-signal bandwidth of a non-inverting amplifier depends on the gain of the circuit and the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1. Adding a capacitor in parallel with R_1 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = V_i \times \left(1 + \frac{R_1}{R_2}\right)$$

1. Calculate the gain.

$$G = \frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}}$$
$$G = \frac{10V - (-10V)}{1\ \ V - (-1\ \ V)} = 10V/V$$

2. Calculate values for R_1 and R_2.

$$G = 1 + \frac{R_1}{R_2}$$
$$\text{Choose} \quad R_1 = 9.09k\Omega$$
$$R_2 = \frac{R_1}{G-1} = \frac{9.09k\Omega}{(10V/V) - 1} = 1.01k\Omega$$

3. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$SR > 2 \times \pi \times V_p \times f = 2 \times \pi \times 10V \times 20kHz = 1.257V/\mu s$$

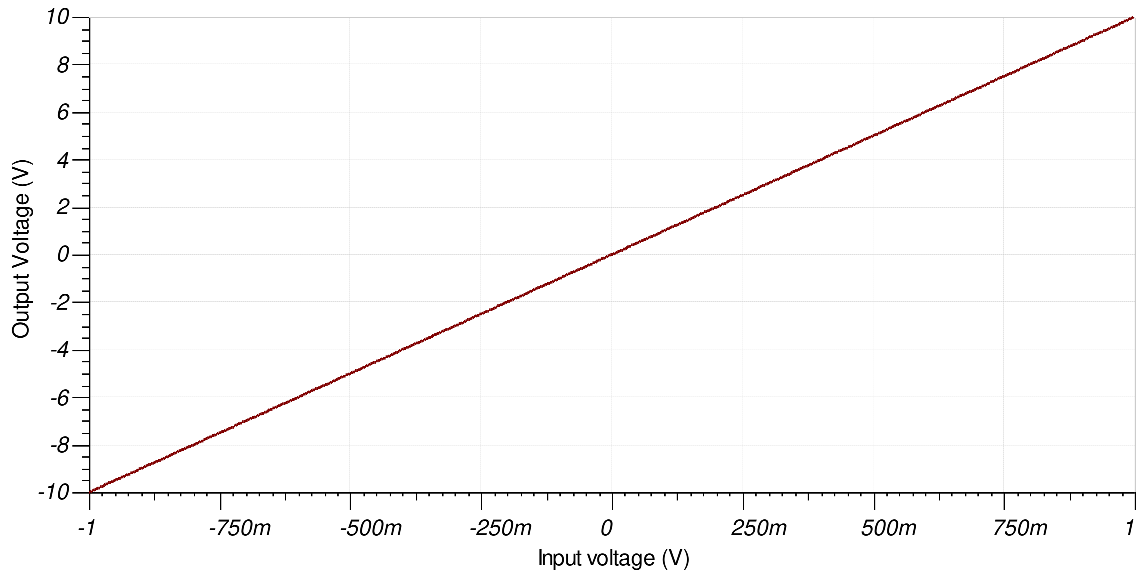
   - The slew rate of the OPA171 is 1.5 V/µs, therefore it meets this requirement.
4. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1 \parallel R_2)} > \frac{GBP}{G}$$
$$\frac{1}{2 \times \pi \times (3pF + 3pF) \times \frac{1.01k\Omega \times 9.09k\Omega}{1.01k\Omega + 9.09k\Omega}} > \frac{3MHz}{10V/V}$$
$$29.18MHz > 300kHz$$

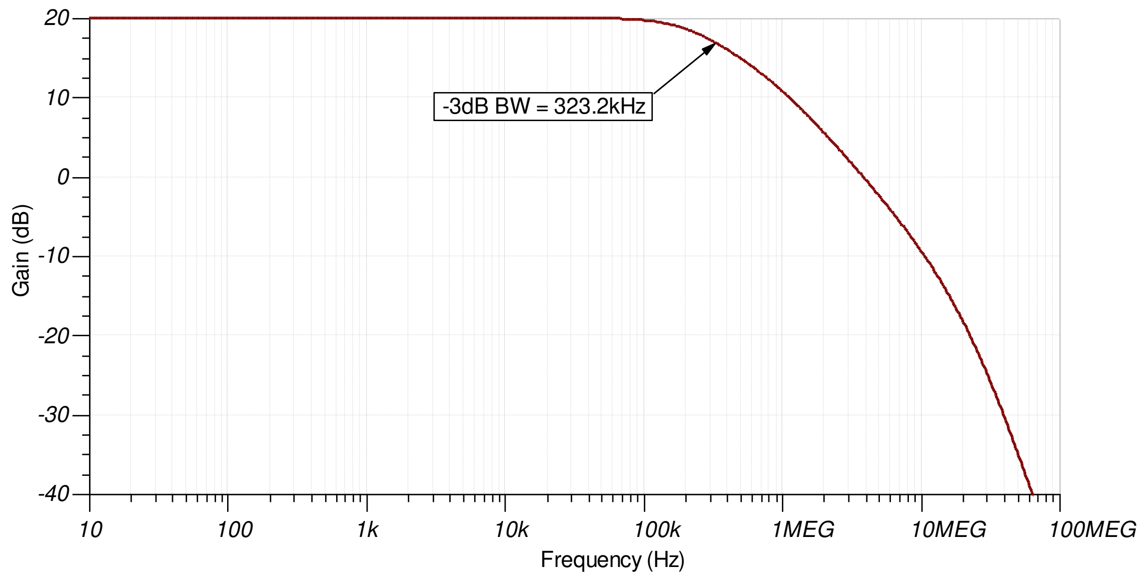
- C_{cm} and C_{diff} are the common-mode and differential input capacitances of the OPA171, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC493.

For more information on many op amp topics including common-mode range, output swing, and bandwidth please visit TI Precision Labs.

Design Featured Op Amp

OPA171	
V_{ss}	2.7 V to 36 V
V_{inCM}	(V_{ee}–0.1 V) to (V_{cc}–2 V)
V_{out}	Rail-to-rail
V_{os}	250 µV
I_q	475 µA
I_b	8 pA
UGBW	3 MHz
SR	1.5 V/µs
#Channels	1, 2, and 4
OPA171	

Design Alternate Op Amp

OPA191	
V_{ss}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	140 µA
I_b	5 pA
UGBW	2.5 MHz
SR	7.5 V/µs
#Channels	1, 2, and 4
OPA191	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 22, 2018 to January 31, 2019 **Page**

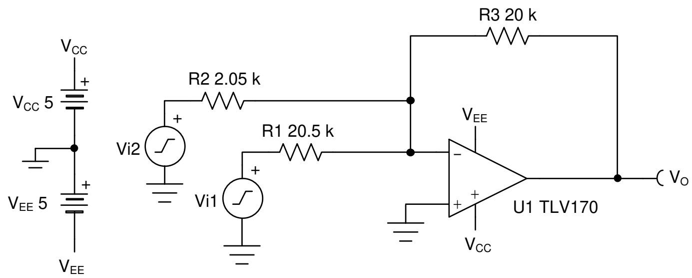
Inverting Summer Circuit

Design Goals

Input 1		Input 2		Output		Freq.	Supply	
V_{i1Min}	V_{i1Max}	V_{i2Min}	V_{i2Max}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
–2.5V	2.5V	–250mV	250mV	–4.9V	4.9V	10kHz	5V	–5V

Design Description

This design sums (adds) and inverts two input signals, V_{i1} and V_{i2}. The input signals typically come from low-impedance sources because the input impedance of this circuit is determined by the input resistors, R_1 and R_2. The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistors. Make sure these values are large when compared to the output impedance of the source.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_3. Adding a capacitor in parallel with R_3 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = V_{i1} \times \left(-\frac{R_3}{R_1}\right) + V_{i2} \times \left(-\frac{R_3}{R_2}\right)$$

1. Select a reasonable resistance value for R_3.

   $$R_3 = 20\ k\Omega$$

2. Calculate gain required for V_{i1}. For this design, half of the output swing is devoted to each input.

   $$|G_{Vi1}| = \left|\frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i1Max} - V_{i1Min}}\right| = \left|\frac{\frac{4.9\ V - (-4.9\ V)}{2}}{2.5\ V - (-2.5\ V)}\right| = 0.98\frac{V}{V} = -0.175\ dB$$

3. Calculate the value of R_1.

   $$|G_{Vi1}| = \frac{R_3}{R_1} \to R_1 = \frac{R_3}{|G_{Vi1}|} = \frac{20\ k\Omega}{0.98\ \frac{V}{V}} = 20.4\ k\Omega \approx 20.5\ k\Omega\ (Standard\,Value)$$

4. Calculate gain required for V_{i2}. For this design, half of the output swing is devoted to each input.

   $$|G_{Vi2}| = \left|\frac{\frac{V_{oMax} - V_{oMin}}{2}}{V_{i2Max} - V_{i2Min}}\right| = \left|\frac{\frac{4.9\ V - (-4.9\ V)}{2}}{250\,mV - (-250\ mV)}\right| = 9.8\ \frac{V}{V} = 19.82\ dB$$

5. Calculate the value of R_2.

   $$|G_{Vi2}| = \frac{R_3}{R_2} \to R_2 = \frac{R_3}{|G_{Vi2}|} = \frac{20\ k\Omega}{9.8\ \frac{V}{V}} = 2.04\ k\Omega \approx 2.05\ k\Omega\ (Standard\,Value)$$

6. Calculate the small signal circuit bandwidth to ensure it meets the 10-kHz requirement. Be sure to use the noise gain (NG), or non-inverting gain, of the circuit. When calculating the noise gain note that R_1 and R_2 are in parallel.

   $$GBP_{OPA170} = 1.2\ MHz$$

   $$NG = 1 + \frac{R_3}{R_1||R_2} = 1 + \frac{20\ k\Omega}{1.86\ k\Omega} = 11.75\frac{V}{V} = 21.4\ dB \quad (8)$$

   $$BW = \frac{GBP}{NG} = \frac{1.2\ MHz}{11.75\ \frac{V}{V}} = 102\ kHz \quad (9)$$

   - This requirement is met because the closed-loop bandwidth is 102kHz and the design goal is 10kHz.

7. Calculate the minimum slew rate to minimize slew-induced distortion.

   $$V_p = \frac{SR}{2 \times \pi \times f} \to SR > 2 \times \pi \times f \times V_p$$

   $$SR > 2 \times \pi \times 10\ kHz \times 4.9\ V = 307.87\ \frac{kV}{s} = 0.31\ \frac{V}{\mu s} \quad (11)$$

   - SR_{OPA170}=0.4V/µs, therefore it meets this requirement.

8. To avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

   $$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1||R_2||R_3)} > \frac{GBP}{NG}$$

   $$\frac{1}{2 \times \pi \times 3\ pF \times 3\ pF \times 1.7\ k\Omega} > \frac{1.2\ MHz}{11.75\ \frac{V}{V}} \quad (13)$$

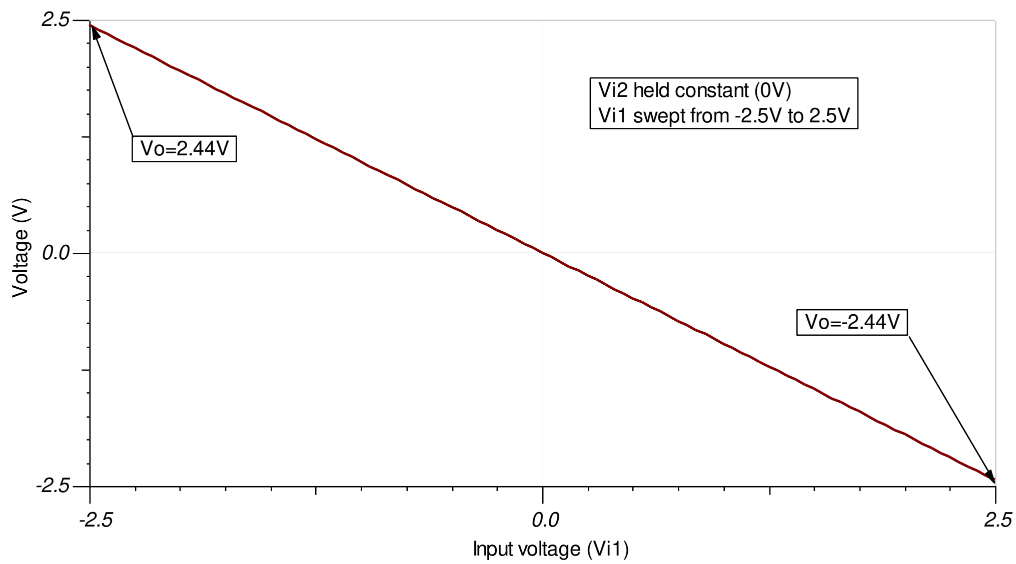
   $$15.6\ MHz > 102\ kHz \quad (14)$$

   - C_{cm} and C_{diff} are the common-mode and differential input capacitances.
   - Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

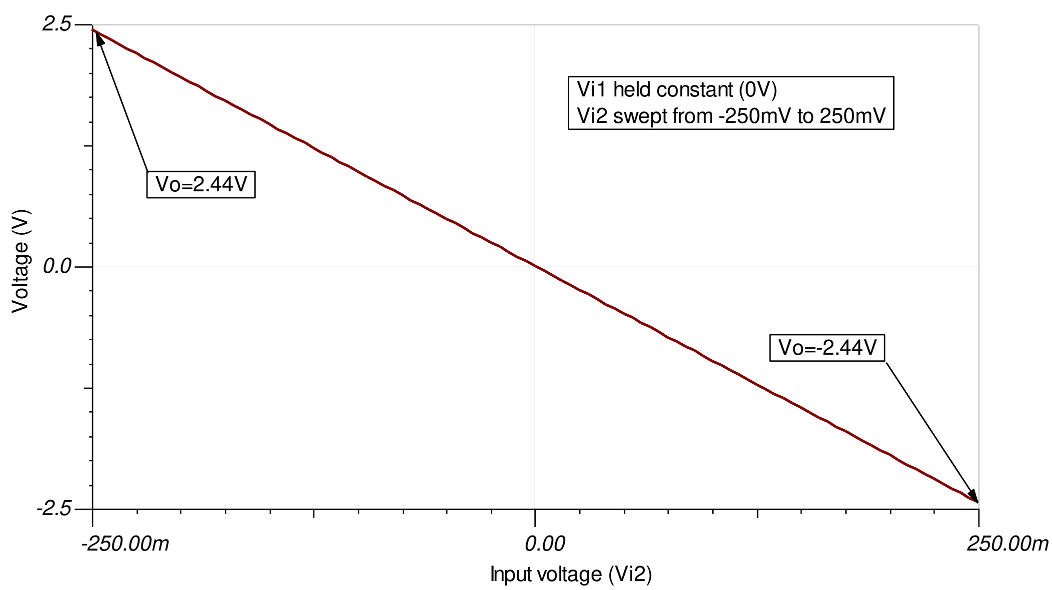
Design Simulations

DC Simulation Results

This simulation sweeps V_{i1} from –2.5V to 2.5V while V_{i2} is held constant at 0V. The output is inverted and ranges from –2.44V to 2.44V.

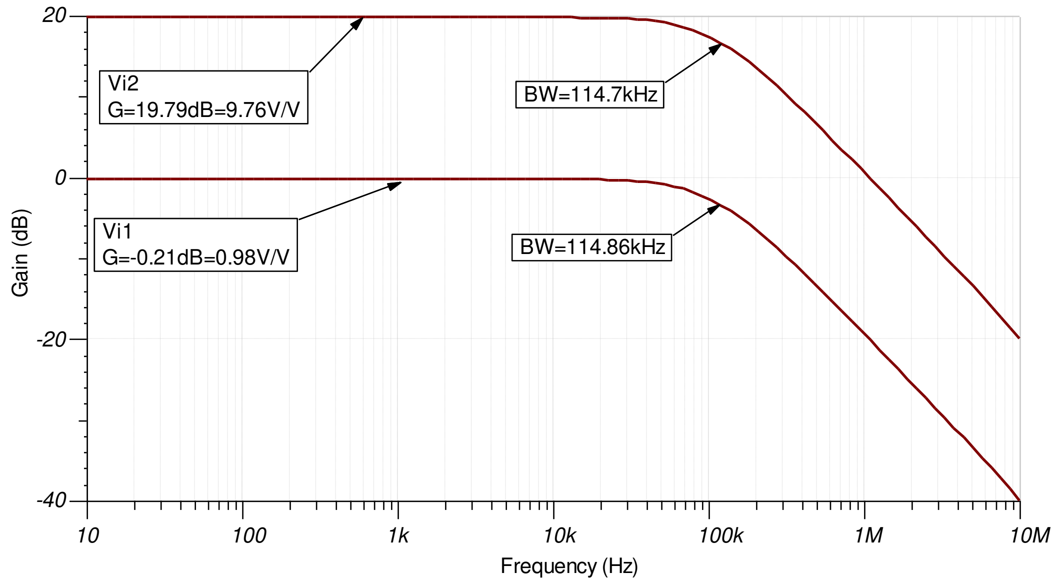


This simulation sweeps V_{i2} from –250mV to 250mV while V_{i1} is held constant at 0V. The output is inverted and ranges from –2.44V to 2.44V.



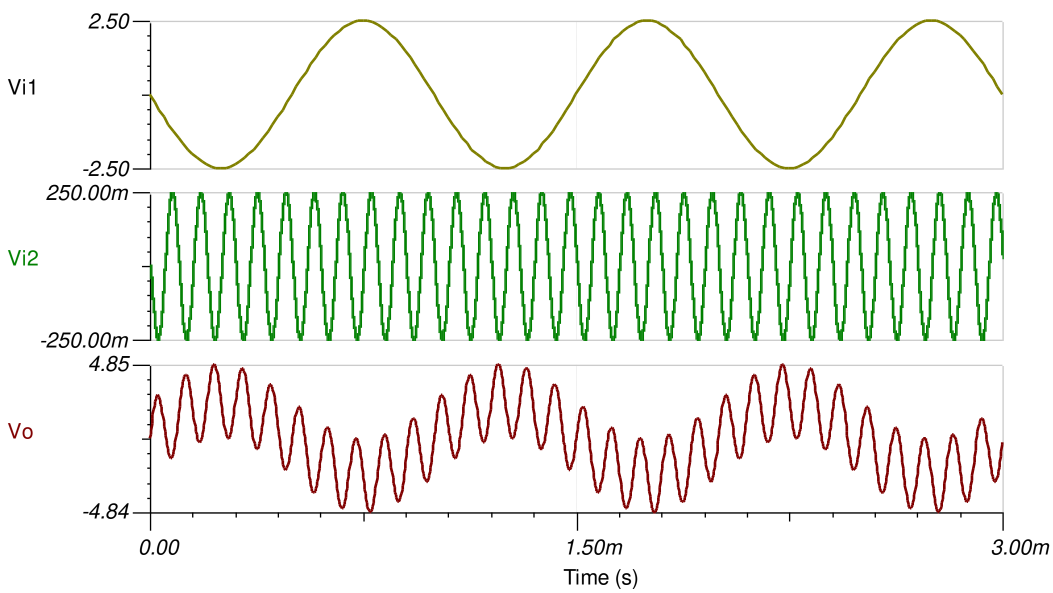
AC Simulation Results

This simulation shows the bandwidth of the circuit. Note that the bandwidth is the same for either input. This is because the bandwidth depends on the noise gain of the circuit, not the signal gain of each input. These results correlate well with the calculations.



Transient Simulation Results

This simulation shows the inversion and summing of the two input signals. V_{i1} is a 1-kHz, 5-V_{pp} sine wave and V_{i2} is a 10-kHz, 500-mV_{pp} sine wave. Since both inputs are properly amplified or attenuated, the output is within specification.



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC494.

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs.

Design Featured Op Amp

OPA170	
V_{ss}	2.7V to 36V
V_{inCM}	(Vee-0.1V) to (Vcc-2V)
V_{out}	Rail-to-rail
V_{os}	0.25mV
I_q	110µA
I_b	8pA
UGBW	1.2MHz
SR	0.4V/µs
#Channels	1, 2, 4
www.ti.com/product/opa170	

Design Alternate Op Amp

LMC7101	
V_{ss}	2.7V to 15.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	110µV
I_q	0.8mA
I_b	1pA
UGBW	1.1MHz
SR	1.1V/µs
#Channels	1
www.ti.com/product/lmc7101	

Revision History

Revision	Date	Change
C	January 2021	Updated Formula format
B	December 2020	Updated Design Goals Table
A	January 2019	Down-style title. Updated title role to *Amplifiers*. Added link to circuit cookbook landing page.

Transimpedance Amplifier Circuit

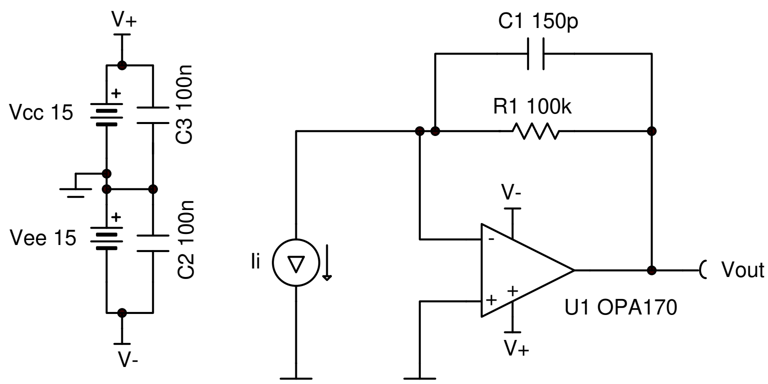
TEXAS INSTRUMENTS

Design Goals

Input		Output		BW	Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}
0 A	50 µA	0 V	5 V	10 kHz	15 V	–15 V

Design Description

The transimpedance op amp circuit configuration converts an input current source into an output voltage. The current to voltage gain is based on the feedback resistance. The circuit is able to maintain a constant voltage bias across the input source as the input current changes which benefits many sensors.



Design Notes

1. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
2. A bias voltage can be added to the non-inverting input to set the output voltage for 0 A input currents.
3. Operate within the linear output voltage swing (see A_{ol} specification) to minimize non-linearity errors.

Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{5V - 0V}{50\mu A} = 100k\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \le \frac{1}{2 \times \pi \times R_1 \times f_p}$$

$$C_1 \le \frac{1}{2 \times \pi \times 100k\Omega \times 10kHz} \le 159pF \approx 150pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

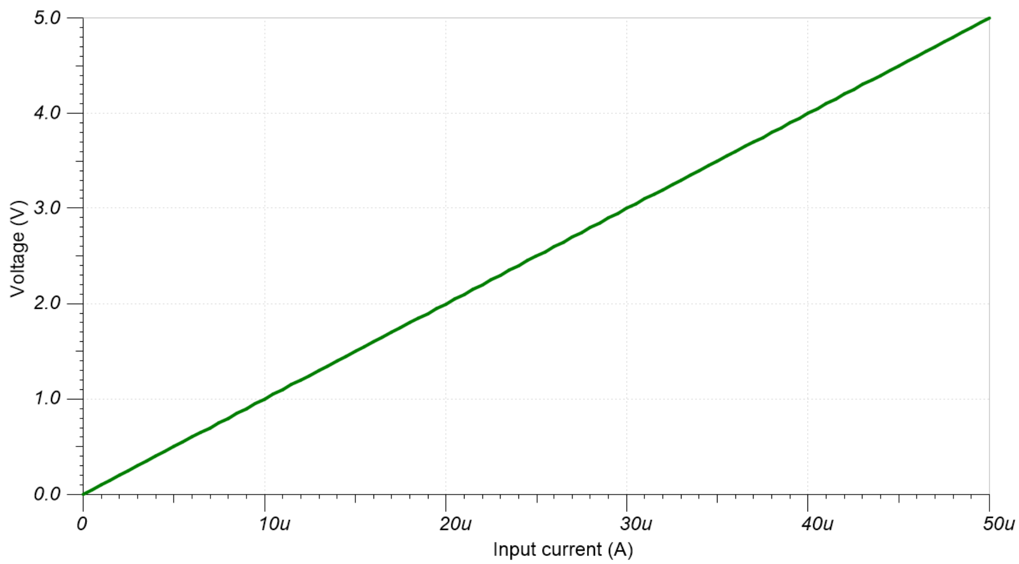
$$GBW > \frac{C_i + C_1}{2 \times \pi \times R_1 \times {C_1}^2} > \frac{6pF + 150pF}{2 \times \pi \times 100k\Omega \times (150pF)^2} > 11.03kHz$$

$$\text{where } C_i = C_s + C_d + C_{cm} = 0pF + 3pF + 3pF = 6pF \text{ given}$$

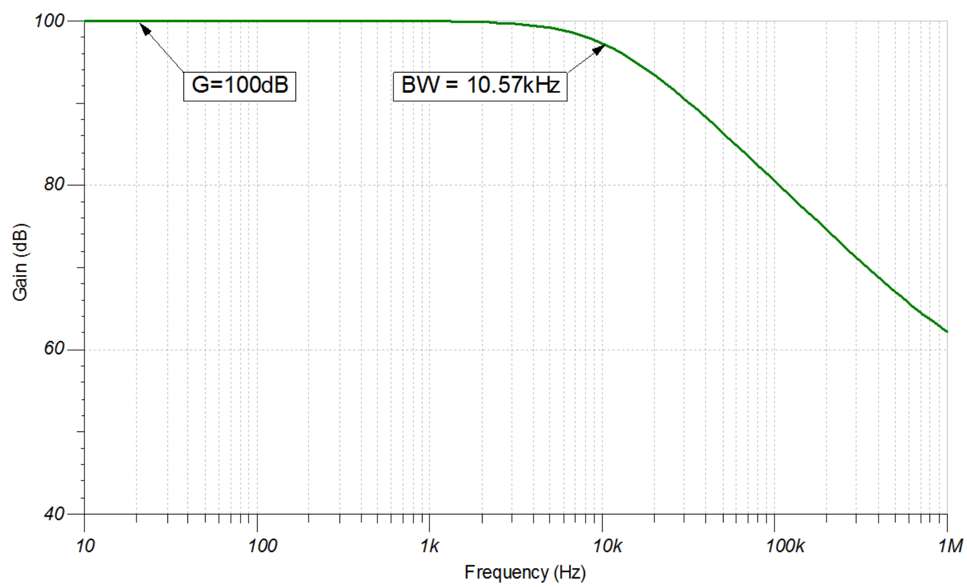
- C_s: Input source capacitance
- C_d: Differential input capacitance of the amplifier
- C_{cm}: Common-mode input capacitance of the inverting input

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC501.

See TIPD176.

Design Featured Op Amp

OPA170	
V_{cc}	2.7 V to 36 V
V_{inCM}	(V_{ee}–0.1 V) to (V_{cc} –2 V)
V_{out}	Rail–to–rail
V_{os}	0.25 mV
I_q	0.11 mA
I_b	8 pA
UGBW	1.2 MHz
SR	0.4 V/µs
#Channels	1, 2, and 4
OPA170	

Design Alternate Op Amp

OPA1671	
V_{cc}	1.7 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	(V_{ee}+10 mV) to (V_{cc}-10 mV) at 275 µA
V_{os}	250 µV
I_q	940 µA
I_b	1 pA
UGBW	12 MHz
SR	5 V/µs
#Channels	1
OPA1671	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Updated *Design Alternate Op Amp* table with OPA1671. Added link to circuit cookbook landing page.	1

Analog Engineer's Circuit

High-Side Current-Sensing Circuit Design

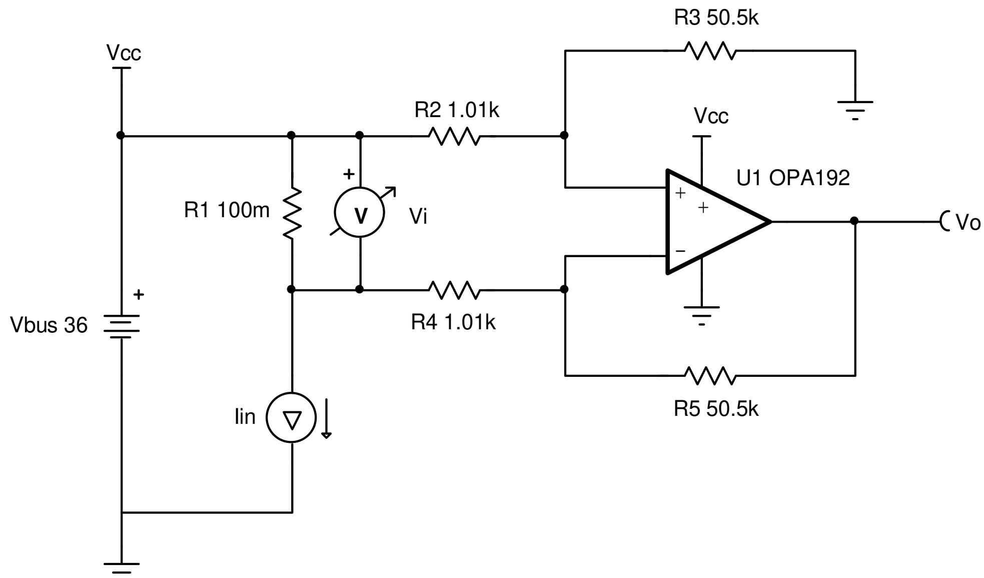
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
50 mA	1 A	0.25 V	5 V	36 V	0 V

Design Description

This single–supply, high–side, low–cost current sensing solution detects load current between 50 mA and 1 A and converters it to an output voltage from 0.25 V to 5 V. High–side sensing allows for the system to identify ground shorts and does not create a ground disturbance on the load.



Design Notes

1. DC common mode rejection ratio (CMRR) performance is dependent on the matching of the gain setting resistors, R_2-R_5.
2. Increasing the shunt resistor increases power dissipation.
3. Ensure that the common–mode voltage is within the linear input operating region of the amplifier. The common mode voltage is set by the resistor divider formed by R_2, R_3, and the bus voltage. Depending on the common–mode voltage determined by the resistor divider a rail–to–rail input (RRI) amplifier may not be required for this application.
4. An op amp that does not have a common-mode voltage range that extends to V_{cc} may be used in low–gain or an attenuating configuration.
5. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability, and help reduce noise.
6. Use the op amp in a linear output operating region. Linear output swing is usually specified under the A_{OL} test conditions.

Design Steps

1. The full transfer function of the circuit is provided below.

$$V_o = I_{in} \times R_1 \times \frac{R_5}{R_4}$$
$$\text{Given} \quad R_2 = R_4 \quad \text{and} \quad R_3 = R_5$$

2. Calculate the maximum shunt resistance. Set the maximum voltage across the shunt to 100 mV.

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{100mV}{1A} = 100m\Omega$$

3. Calculate the gain to set the maximum output swing range.

$$\text{Gain} = \frac{V_{oMax} - V_{oMin}}{(I_{iMax} - I_{iMin}) \times R_1} = \frac{5V - 0.25V}{(1A - 0.05A) \times 100m\Omega} = 50\frac{V}{V}$$

4. Calculate the gain setting resistors to set the gain calculated in step 3.

$$\text{Choose} \quad R_2 = R_4 = 1.01k\,\Omega \quad (\text{Standard} \quad \text{value})$$
$$R_3 = R_5 = R_2 \times \text{Gain} = 1.01k\,\Omega \times 50\frac{V}{V} = 50.5k\,\Omega \,(\text{Standard} \quad \text{value})$$

5. Calculate the common–mode voltage of the amplifier to ensure linear operation.

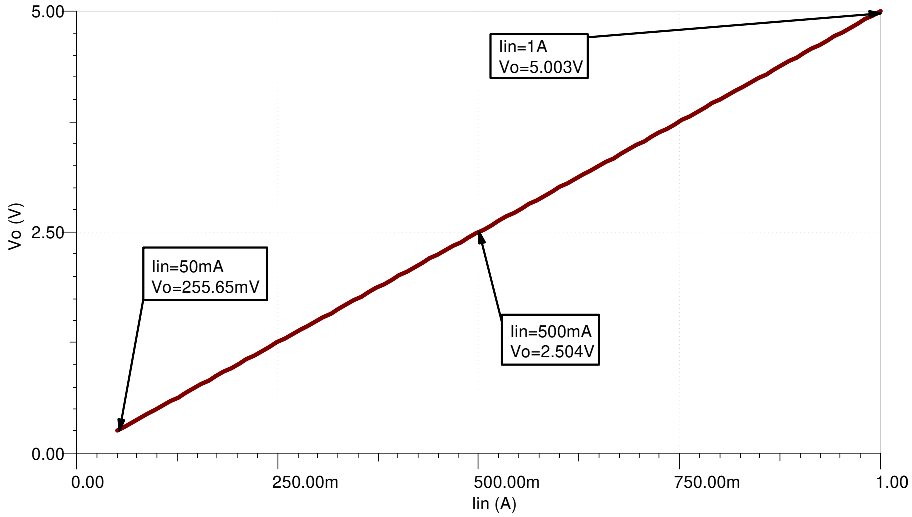
$$V_{cm} = V_{CC} \times \frac{R_3}{R_2 + R_3} = 36V \times \frac{50.5k}{1.01k + 50.5k} = 35.294\ V$$

6. The upper cutoff frequency (f_H) is set by the non–inverting gain (noise gain) of the circuit and the gain bandwidth (GBW) of the op amp.

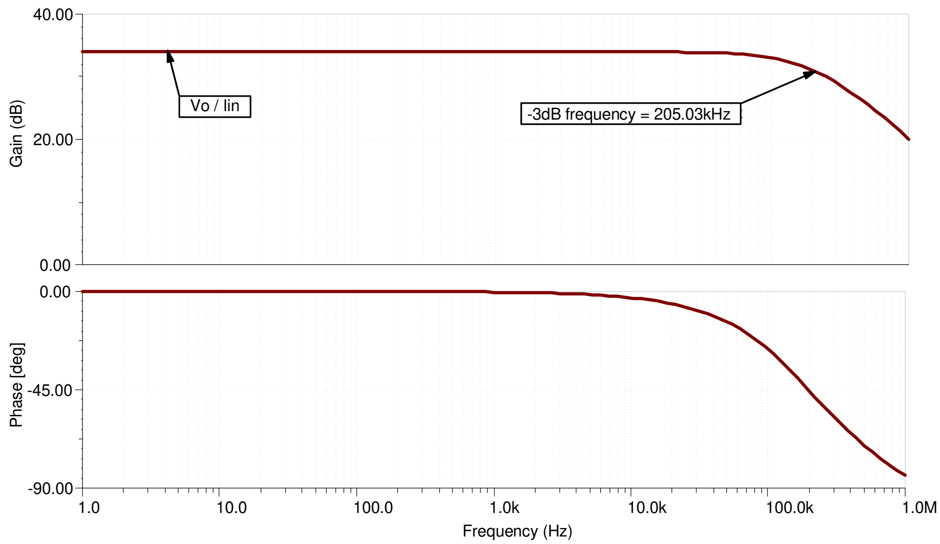
$$f_H = \frac{GBW}{\text{Noise Gain}} = \frac{10MHz}{51\frac{V}{V}} = 196.1 \quad kHz$$

Design Simulations

DC Simulation Results



AC Simulation Results



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOMAV4
3. TI Precision Labs

Design Featured Op Amp

OPA192	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	5 µV
I_q	1 mA
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA192	

Design Alternate Op Amp

OPA2990	
V_{cc}	2.7 V to 40 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	250 µV
I_q	120 µA
I_b	10 pA
UGBW	1.25 MHz
SR	5V/µs
#Channels	2
OPA2990	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 30, 2018 to February 13, 2019	Page
• Downstyle title. Added *Design Alternate Op Amp* table	1

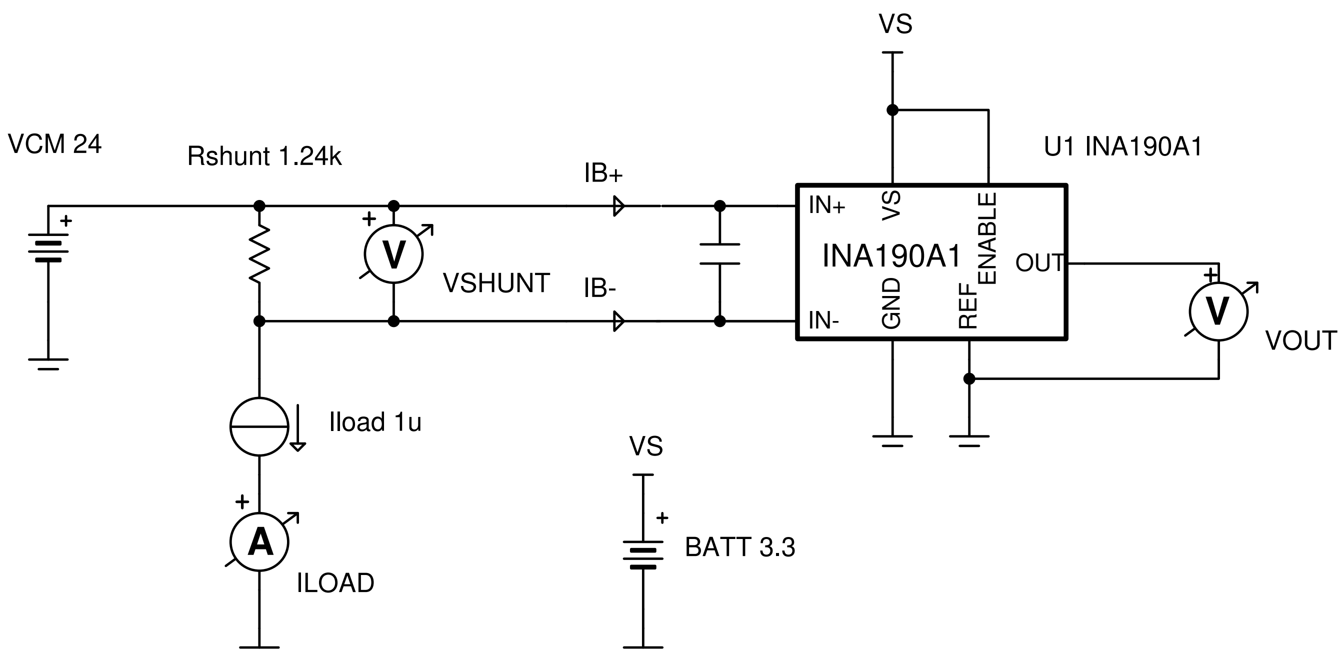
Analog Engineer's Circuit

Low (Microamp), High-Side, Current-Sensing Circuit with Current-Sensing Amplifier at High Voltage and Overtemperature

Input			Output		Supply			Temperature	
$I_{load\ Min}$	$I_{load\ Max}$	V_{CM}	$V_{OUT\ Min}$	$V_{OUT\ Max}$	$I_{Q\ Max}$	V_{VS}	V_{ee}	Low	High
1 µA	104 µA	$-0.1\ V \le V_{CM} \le 40\ V$	31.0 mV at 1 µA	3.224 V at 104 µA	65 µA	3.3 V	GND (0 V)	0°C	85°C

Design Description

This circuit demonstrates how to use a current sense amplifier to accurately and robustly measure small micro-amp currents and maximize dynamic range. The following error analysis can be applied to many current sense amplifiers. This design relies on using a precision, low input-bias current sense amplifier and analyzing the dynamic error due to input bias currents on large shunt resistors.



Design Notes

1. The *Getting Started with Current Sense Amplifiers* video series introduces implementation, error sources, and advanced topic for using current sense amplifiers.
2. Choose a precision 0.1% shunt resistor to limit gain error at higher currents.
3. Choose a low input-bias current (high input-impedance) amplifier such as the INA190.
4. Ensure VCM is within the operating VCM range of INA190: –0.1 V to 40 V.
5. Error significantly reduces if DC offsets are calibrated out with one-point calibration or if device operates under the same conditions as the *INA190 Low-Supply, High-Accuracy, Low- and High-Side Current-Shunt Monitor With Picoamp Bias Current and Enable* data sheet specifies (V_{VS} = 1.8 V, V_{CM} = 12 V, V_{REF} = 0.9 V, T_A = 25°C). A two-point calibration can be done to eliminate gain error.
6. It is recommended to add ≥ 1 nF input differential capacitor to INA190 inputs when working with large shunt resistors and DC currents.
7. Follow best practices for layout according to the data sheet: decoupling capacitor close to VS pin, routing the input traces for IN+ and IN- as a differential pair, and so forth.

Design Steps

1. Given the design requirements, ensure the shunt resistor achieves a maximum total error of 3.51% at 1 µA load current. Assume all offset and gain errors are negative. Note that error due to input bias current (I_{IB}) is a function of the V_{SHUNT} and input differential impedance (R_{DIFF}) where R_{DIFF} = I_{IB+}/V_{DIFF}. Since I_{IB-} starts around +500 pA and decreases as V_{SHUNT} increases, this generates a negative input offset error. See the *IB+ and IB- vs Differential Input Voltage* plot in the data sheet.

$$T_{MIN} = 0^{o}C; T_{MAX} \quad 85^{o}C$$

$$I_{LOAD\_MINIMUM} = 1\mu A$$

$$R_{SHUNT} = 1240\Omega, 0.1\%$$

$$V_{VS} = 3.3V; V_{CM} = 24V; V_{REF} = GND = 0V$$

$$V_{OSI\_MAX} \quad -15\mu V$$

$$V_{OS\_CMRR\_MAX} = |12V - V_{CM}| \cdot 10^{-CMRR_{MIN}/20dB} = 12V \cdot 10^{-132dB/20dB} \quad -3.01\mu V$$

$$V_{OS\_PSRR\_MAX} = |1.8V - V_{VS}| \cdot PSRR_{MAX} \quad 3.2V \cdot 5^{\mu V}/_{V} \quad -7.5\mu V$$

$$V_{OS\_RVRR\_MAX} = |0.9V - V_{REF}| \cdot RVRR_{MAX} \quad 0.9V \cdot 10^{\mu V}/_{V} \quad -9\mu V$$

$$V_{OS\_Drift\_MAX} = |25°C - T_{MAX}| \cdot \left(\frac{dV_{OS}}{dT}\right)_{MAX} \quad 60°C \cdot 80^{nV}/_{°C} \quad -4.8\mu V$$

$$V_{OS\_IB\_MAX} \quad func\{V_{SHUNT}\} = R_{SHUNT} \cdot \left[\frac{-V_{SHUNT}}{R_{DIFF}} + I_{IB\_Typ}\right] = 1240\Omega \cdot \left[\frac{-1.24mV}{2.3M\Omega} + 0.5nA\right] \quad -48.5nV$$

$$V_{OS\_MAX} \quad V_{OSI\_MAX} + V_{OS\_CMRR} + V_{OS\_PSRR} + V_{OS\_RVRR} + V_{OS\_Drift\_Max} + V_{OS\_IB\_MAX}$$

$$V_{OS\_MAX} \quad -39.4\mu V$$

$$R_{shunt\_tolerance} \quad -0.1\% \quad 0.001$$

$$GE_{25C\_MAX} \quad -0.3\% \quad -0.003$$

$$GE_{Drift\_MAX} \quad -7^{ppm}/_{°C} \cdot (85°C - 25°C) \cdot 10^{-6} \quad -0.00042$$

$$Gain_{MAX} \quad 25 \cdot (1 + GE_{25C\_MAX} + GE_{Drift\_MAX}) \quad 25 \cdot (0.99758) \quad 24.940^{V}/_{V}$$

$$V_{OUT\_MIN\_1\mu A} \quad [V_{OS\_MAX} + I_{LOAD} \cdot R_{SHUNT} \cdot (1 + R_{shunt\_tolerance})] \cdot Gain_{MAX} \quad 29.9mV$$

$$V_{OUT\_IDEAL\_1\mu A} \quad [I_{LOAD\_MINIMUM} \cdot R_{SHUNT}] \cdot Gain = 31.0mV$$

$$Error = 100 \cdot (V_{OUT\_MIN} - V_{OUT\_IDEAL}) / V_{OUT\_IDEAL}$$

$$Error_{1\mu A} = -3.51\%$$

$$Error_{6\mu A} \quad -0.91\%$$

2. Ensure the sensed current range fits within the output dynamic range of the device. This depends upon two specifications: Swing-to-V_{VS} (V_{SP}) and Zero-current Output Voltage (V_{ZL}). V_{ZL} is specified over -40°C to +125°C at V_{VS} = 1.8 V, V_{REF} = 0 V, V_{SENSE} = 0 mV, V_{CM} = 12 V, and R_L = 10 kΩ. Since data sheet conditions do not match the conditions of this design, extrapolate what the maximum V_{ZL} would be.
   a. Calculate the maximum possible positive offset for testing conditions of V_{ZL}. Call this $V_{OS\_TestConditions}$.
   b. Convert this input offset into an output offset by multiplying by maximum possible gain.
   c. Determine the Headroom voltage by taking difference between the V_{ZL_MAX} from data sheet and the previously determined maximum output offset.
   d. Calculate V_{ZL_MAX} in this design by adding the Headroom voltage to the maximum possible output offset for this design.
   e. Ensure that the minimum V_{OUT} at 1µA is greater than V_{ZL_MAX}. Note V_{OUT_MIN} at 1µA assumes worst-case scenario of –1% tolerance for R_{SHUNT} and negative input offsets.

$$V_{OS\_TestConditions} \quad V_{OSI\_MAX} + |0.9V - 0V| \cdot RVRR_{MAX} + |125°C + 40°C| \cdot \left(\frac{dV_{OS}}{dT}\right)_{MAX}$$

$$V_{OS\_TestConditions} \quad +15\mu V + 9\mu V + 13.2\mu V = 37.2\mu V$$

$$\text{Headroom} \quad V_{ZL\_MAX\_DATASHEET} - V_{OS\_TestConditions} \cdot Gain_{MAX}$$

$$\text{Headroom} \quad 3mV - 0.933mV \quad 2.07mV$$

$$V_{ZL\_MAX} \quad \text{Headroom} + V_{OS\_MAX} \cdot Gain_{MAX} \quad 2.07mV + (39.4\mu V \cdot 25.061 \tfrac{V}{V}) \quad 3.06mV$$

$$V_{OUT\_MIN\_1\mu A} \quad 29.9mV > V_{ZL\_MAX}$$

   f. Now ensure the maximum V_{OUT} at 104 µA is less than V_{SP_MIN}. Note V_{OUT_MAX} at 104 µA assumes worst-case scenario of +1% tolerance for R_{SHUNT} and positive input offsets.

$$V_{SP\_MIN} \quad V_{VS} - 40mV \quad 3.26V$$

$$V_{OUT\_MAX} \quad \left[R_{SHUNT} \cdot (1 + R_{shunt\_tolerance}) \cdot I_{LOAD\_MAX} + V_{OS\_MAX}\right] \cdot Gain_{MAX}$$

$$V_{OUT\_MAX} \quad [1240\Omega \cdot (1.001) \cdot 104\mu A - 29.6\mu V] \cdot 25.061 \tfrac{V}{V} = 3.234V$$

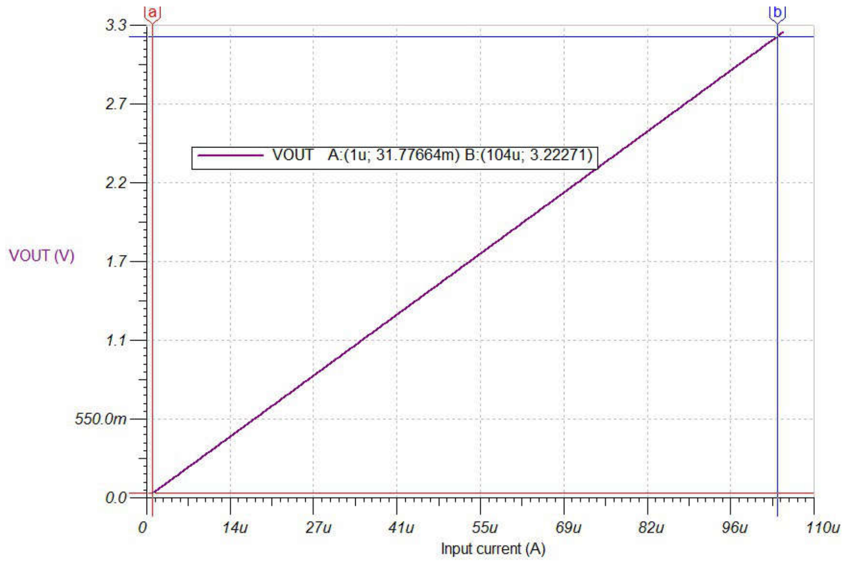
$$V_{OUT\_MAX} < V_{SP\_MIN}$$

3. Generate *Total Error vs Load Current* curves based upon the total error equations in Step 1. Do this for the typical and maximum data sheet specifications.

Design Simulations

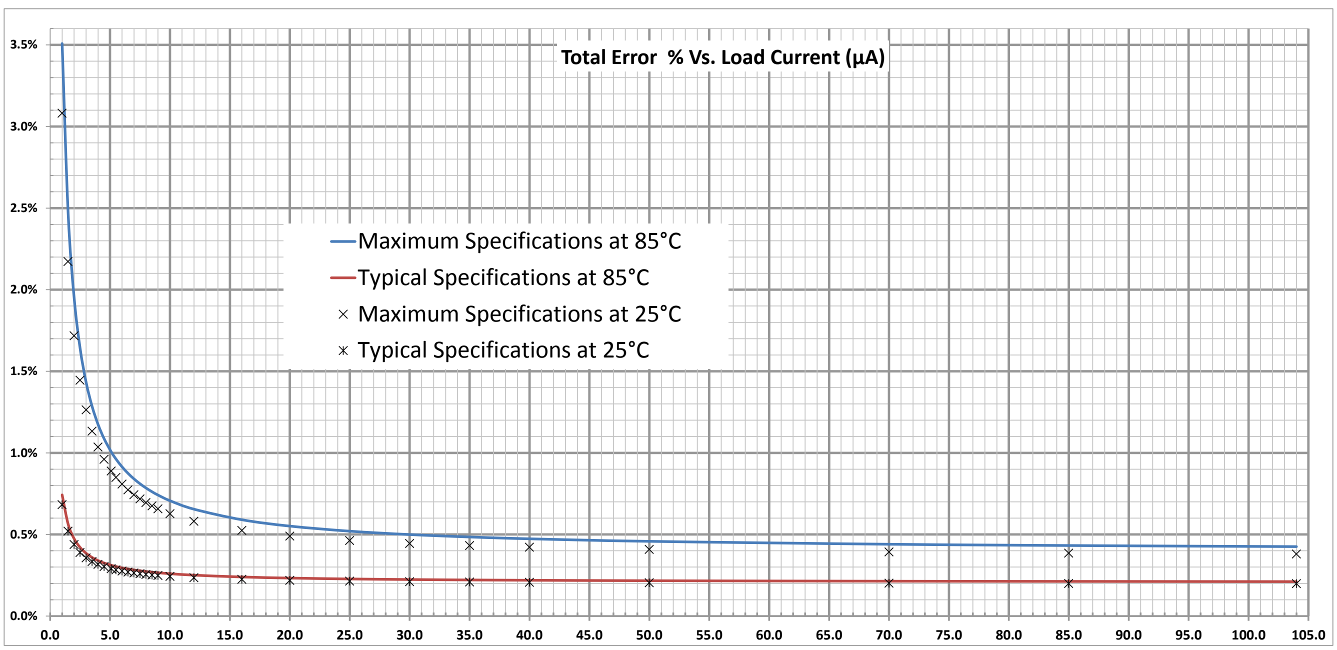
DC Simulation Results

The following graph shows a linear output response for load currents from 1 µA to 104 µA



Total Error Calculations

The following graph shows the total absolute error over temperature using both the assured limit specifications and the typical specifications. Note that accuracy is limited by the offset voltage at the lowest current sensed and limited by gain error at higher currents. Active offset chopping limits the error due to temperature.



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOMAI6.

Getting Started with Current Sense Amplifiers video series

Getting started with current sense amplifiers

Application Note on Power-Saving Topologies for TI Current Shunt Monitors

Extending Voltage Range of Current Shunt Monitor

Current Sense Amplifiers on TI.com

Current sense amplifiers – Products

For direct support from TI Engineers use the E2E community

TI E2E™ design support forums

Design Featured Current Shunt Monitor

INA190A1	
V_{VS}	1.8 V to 5 V (operating)
V_{CM}	-0.3 V to 42 V (survivability)
V_{OUT}	Up to (V_{VS}) + 0.3 V
V_{OS}	±3 µV to ±15 µV
I_Q	48 µA to 65 µA
I_{IB}	0.5 nA to 3 nA
BW	45 kHz at 25 V/V (A1 gain variant)
# of Channels	1
INA190	

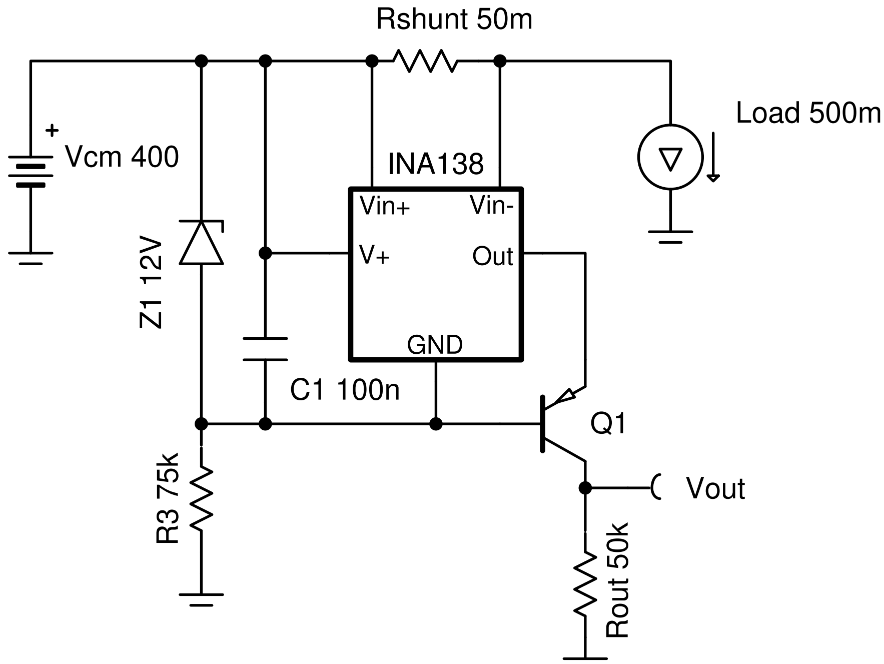
Analog Engineer's Circuit

High-Voltage, High-Side Floating Current Sensing Circuit Using Current Output, Current Sense Amplifier

Input		Output		Supply		
$I_{load\ Min}$	$I_{load\ Max}$	$V_{out\ Min}$	$V_{out\ Max}$	$V_{cm\ Min}$	$V_{cm\ Max}$	V_{ee}
0.5 A	9.9 A	250 mV	4.95 V	12 V	400 V	GND (0 V)

Design Description

This cookbook is intended to demonstrate a method of designing an accurate current sensing solution for systems with high common mode voltages. The principle aspect of this design uses a unidirectional circuit to monitor a system with V_{cm} = 400 V by floating the supplies of the device across a Zener diode from the supply bus (V_{cm}). This cookbook is based on the *High Voltage 12 V – 400 V DC Current Sense Reference Design*.



Design Notes

1. The *Getting Started with Current Sense Amplifiers* video series introduces implementation, error sources, and advanced topics for using current sense amplifiers.
2. This example is for high V_{CM}, high-side, unidirectional, DC sensing.
3. To minimize error, make the shunt voltage as large as the design will allow. For the INA138 device, keep V_{sense} >> 15 mV.
4. The relative error due to input offset increases as shunt voltage decreases, so use a current sense amplifier with low offset voltage. A precision resistor for R_{shunt} is necessary because R_{shunt} is a major source of error.
5. The INA138 is a current-output device, so voltages referenced to ground are achieved with a high voltage bipolar junction transistor (BJT).
   - Ensure the transistor chosen for Q1 can withstand the maximum voltage across the collector and emitter (for example, need 400 V, but select > 450 V for margin).
   - Multiple BJTs can be stacked and biased in series to achieve higher voltages
   - High beta of this transistor reduces gain error from current that leaks out of the base

Design Steps

1. Determine the operating load current and calculate R_{shunt}:
   - Recommended V_{sense} is 100mV and maximum recommended is 500 mV, so the following equation can be used to calculate R_{shunt} where V_{sense} ≤ 500 mV:

$$R_{shunt} = \frac{V_{sense\ max}}{I_{load\ max}} \rightarrow \frac{0.5V}{10A} = 50m\Omega$$

   - For more accurate and precise measurements over the operating temperature range, a current monitor with integrated shunt resistor can be used in some systems. The benefits of using these devices are explained in *Getting Started with Current Sense Amplifiers, Session 16: Benefits of Integrated Precision Shunt Resistor*.
2. Choose a Zener diode to create an appropriate voltage drop for the INA138 supply:
   - The Zener voltage of the diode should fall in the INA138 supply voltage range of 2.7 V to 36 V and needs to be larger than the maximum output voltage required.
   - The Zener diode voltage regulates the INA138 supply and protects from transients.
   - Data sheet parameters are defined for 12 V V_{in+} to the GND pin so a 12 V Zener is chosen.
3. Determine the series resistance with the Zener diode:
   - This resistor (R3) is the main power consumer due to its voltage drop (up to 388 V in this case). If R3 is too low, it will dissipate more power, but if it is too high R3 will not allow the Zener diode to avalanche properly. Since the data sheet specifies I_Q for V_S = 5 V, estimate the maximum quiescent current of the INA138 device at V_S = 12 V to be 108 μA and calculate R3 using the bias current of the Zener diode, 5 mA, as shown:

$$R_3 = \frac{V_{CM} - V_{zener}}{I_{zener} + I_{INA138}} = \frac{400V - 12V}{5mA + 108\mu A} \approx 75.96k\Omega$$

$$\text{standard value} \rightarrow 75k\Omega$$

   - The power consumption of this resistor is calculated using the following equation:

$$Power_{R3} = \frac{(V_{cm} - V_{Zener})^2}{R3} \rightarrow \frac{(400V - 12V)^2}{75k\Omega} \approx 2.007W$$

4. Calculate R_{out} using the equation for output current in the INA138 data sheet.
   - This system is designed for 10 V/V gain where V_{out} = 1 V if V_{sense} = 100 mV:

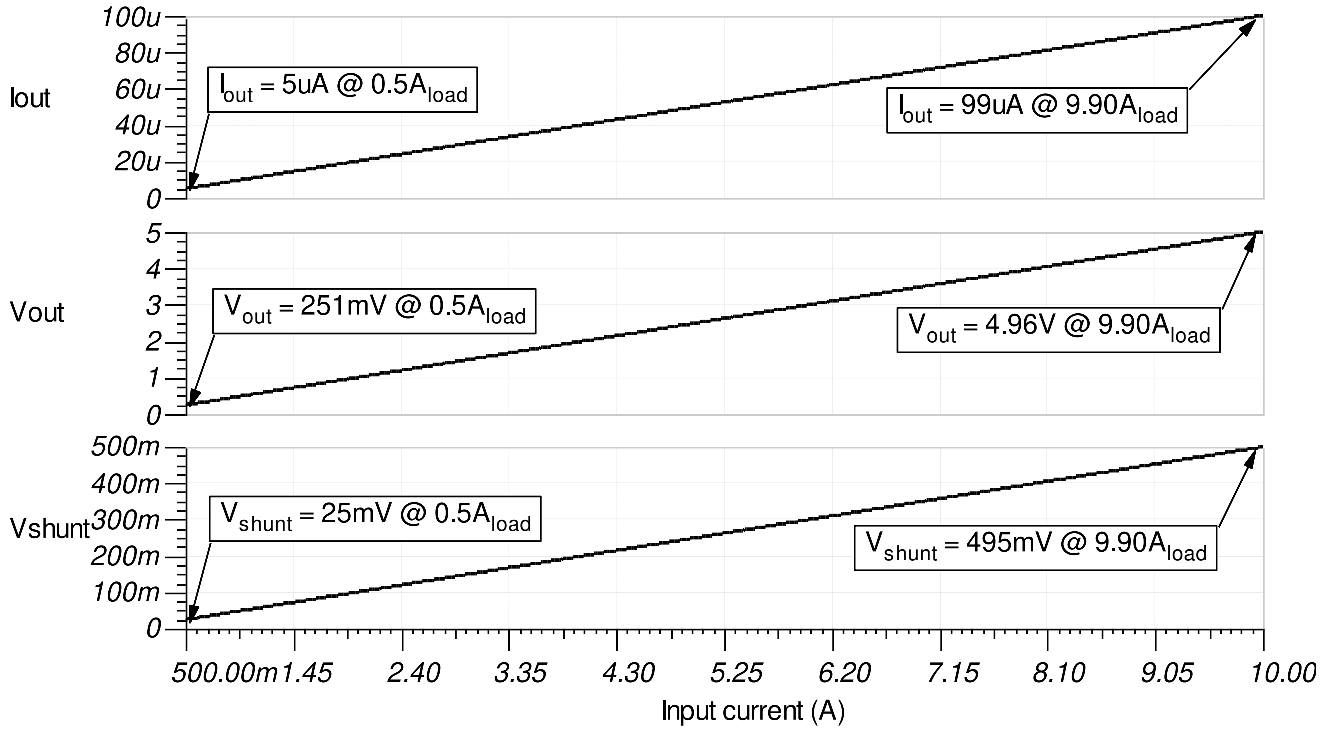
$$I_{out\ INA138} = 200\frac{\mu A}{V} \times (V_{sense\ max}) \rightarrow 200\frac{\mu A}{V} \times (0.5V) = 100\mu A$$

$$R_{out} = \frac{V_{out\ max}}{I_{out\ INA138}} \rightarrow \frac{5V}{100\mu A} = 50k\Omega$$

Design Simulations

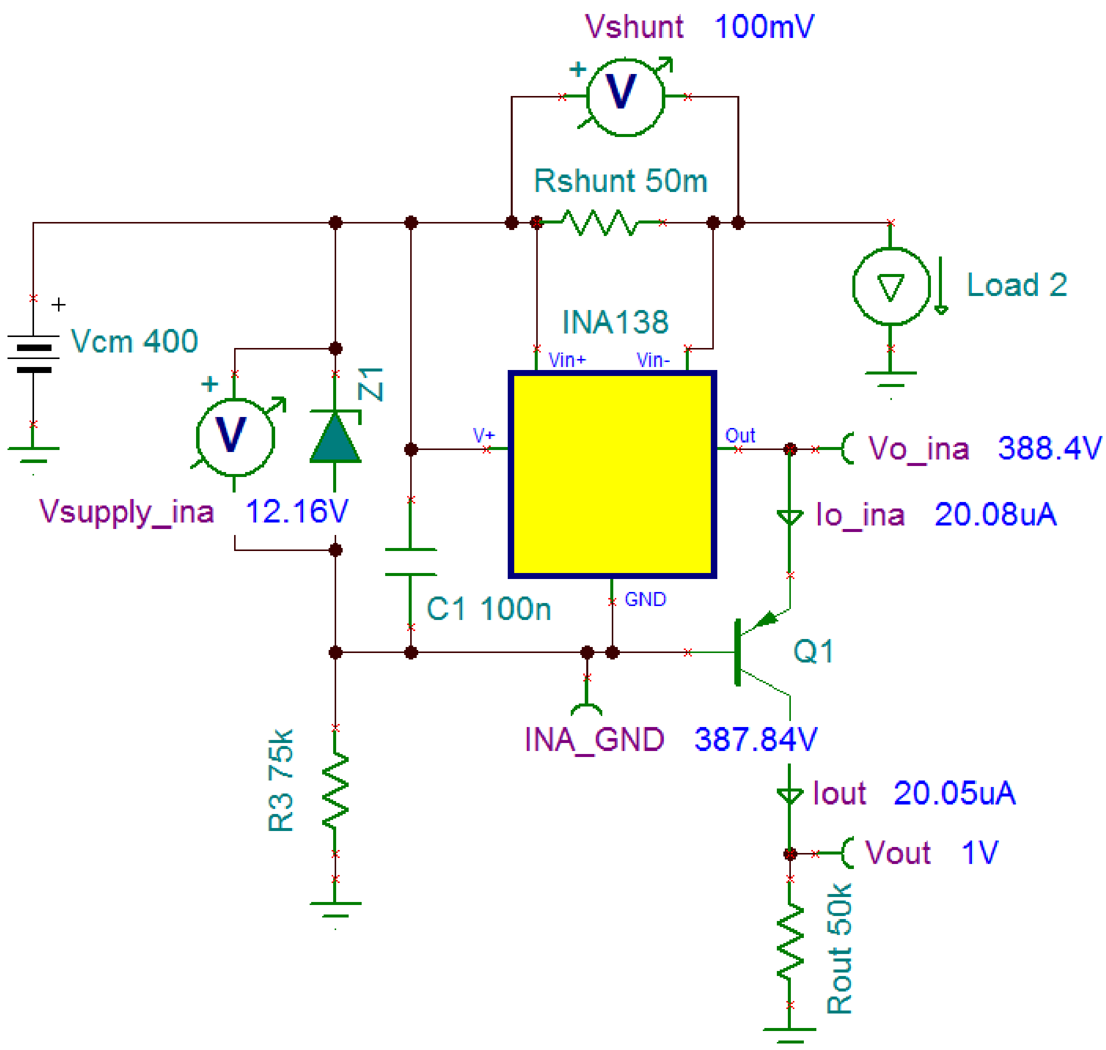
DC Simulation Results

The following graph shows a linear output response for load currents from 0.5 A to 10 A and 12 V ≤ V_{cm} ≤ 400 V. I_{out} and V_{out} remain constant over a varying V_{cm} once the Zener diode is reverse biased.



Steady State Simulation Results

The following image shows this system in DC steady state with a 2 A load current. The output voltage is 10× greater than the measured voltage across R_{shunt}.



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SGLC001.

Getting Started with Current Sense Amplifiers video series:

https://training.ti.com/getting-started-current-sense-amplifiers

Abstract on Extending Voltage Range of Current Shunt Monitor:

Extending Voltage Range of Current Shunt Monitor

High Voltage 12 V – 400 V DC Current Sense Reference Design:

TIDA=00332

Cookbook Design Files:

SGLC001

Current Sense Amplifiers on TI.com:

Current sense amplifiers - Products

For direct support from TI Engineers use the E2E community:

TI E2E™ design support forums

Design Featured Current Shunt Monitor

INA138	
V_{ss}	2.7 V to 36 V
$V_{in\ cm}$	2.7 V to 36 V
V_{out}	Up to (V+) -0.8 V
V_{os}	±0.2 mV to ±1 mV
I_q	25 µA to 45 µA
I_b	2 µA
UGBW	800 kHz
# of Channels	1
INA138	

Design Alternate Current Shunt Monitor

INA168	
V_{ss}	2.7 V to 60 V
$V_{in\ cm}$	2.7 V to 60 V
V_{out}	Up to (V+) -0.8 V
V_{os}	±0.2 mV to ±1 mV
I_q	25 µA to 45 µA
I_b	2 µA
UGBW	800 kHz
# of Channels	1
INA168	

Analog Engineer's Circuit

AC-coupled transimpedance amplifier circuit

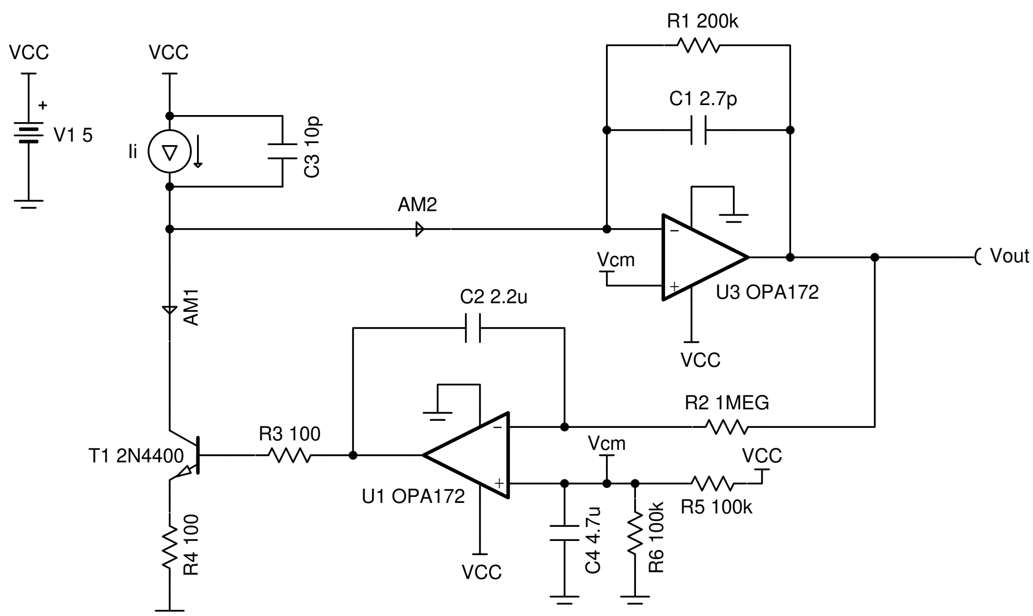
Amplifiers

Design Goals

Input Current		Ambient light current	Output voltage		Target Bandwidth	Supply	
I_{iMin}	I_{iMax}		V_{oMin}	V_{oMax}		V_{cc}	V_{ee}
–10µA	10µA	100µA	0.5V	4.5V	300kHz	5V	0V

Design Description

This circuit uses an op amp configured as a transimpedance amplifier to amplify the AC signal of a photodiode (modeled by I_i and C_3). The circuit rejects DC signals using a transistor to sink DC current out of the photodiode through the use of an integrator in a servo loop. The bias voltage applied to the non-inverting input prevents the output from saturating to the negative supply rail in the absence of input current.



Design Notes

1. Use a JFET or CMOS input op amp with low-bias current to reduce DC errors.
2. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability and help reduce noise.
3. The junction capacitance of photodiode changes with reverse bias voltage which will influence the stability of the circuit.
4. Reverse-biasing the photodiode can reduce the effects of dark current.
5. A resistor, R_3, may be needed on the output of the integrator amplifier.
6. An emitter degeneration resistor, R_4, should be used to help stabilize the BJT.
7. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions.

Design Steps

The transfer function of the circuit is:

$$V_{out} = -I_i \times R_1$$

1. Calculate the value of the feedback resistor, R_1, to produce the desired output swing.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax} - I_{iMin}} = \frac{4.5V - 0.5V}{10\mu A - (-10\mu A)} = 200k\Omega$$

2. Calculate the feedback capacitor to limit the signal bandwidth.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_p} = \frac{1}{2\pi \times 200k\Omega \times 300kHz} = 2.65pF \approx 2.7pF \text{ (Standard Value)}$$

3. Calculate the gain bandwidth of the amplifier needed for the circuit to be stable.

$$GBW = \frac{C_i + C_1}{2\pi \times R_1 \times C_1^2} = \frac{23pF + 2.7pF}{2\pi \times 200k\Omega \times (2.7pF)^2} = 2.97MHz$$

Where:

$$C_i = C_{pd} + C_b + C_d + C_{cm} = 10pF + 5pF + 4pF + 4pF = 23pF$$

Given:

- C_{pd}: Junction capacitance of photodiode
- C_b: Output capacitance of BJT
- C_d: Differential input capacitance of the amplifier
- C_{cm}: Common-mode input capacitance of the inverting input

4. Set the cutoff frequency of the integrator circuit, f_I, to 0.1Hz to only allow signals near DC to be subtracted from the photodiode output current. The cutoff frequency is set by R_2 and C_2. Select R_2 as 1MΩ.

$$C_2 = \frac{1}{2\pi \times R_2 \times f_I} = \frac{1}{2\pi \times 1M\Omega \times 0.1Hz} = 1.59\mu F \approx 2.2\mu F \text{ (Standard Value)}$$

5. Select R_3 as 100Ω to isolate the capacitance of the BJT from op amp and stabilize the amplifier. For more information on stability analysis, see the Design References section [2].
6. Bias the output of the circuit by setting the input common mode voltage of the integrator circuit to mid-supply. Select R_5 and R_6 as 100kΩ.

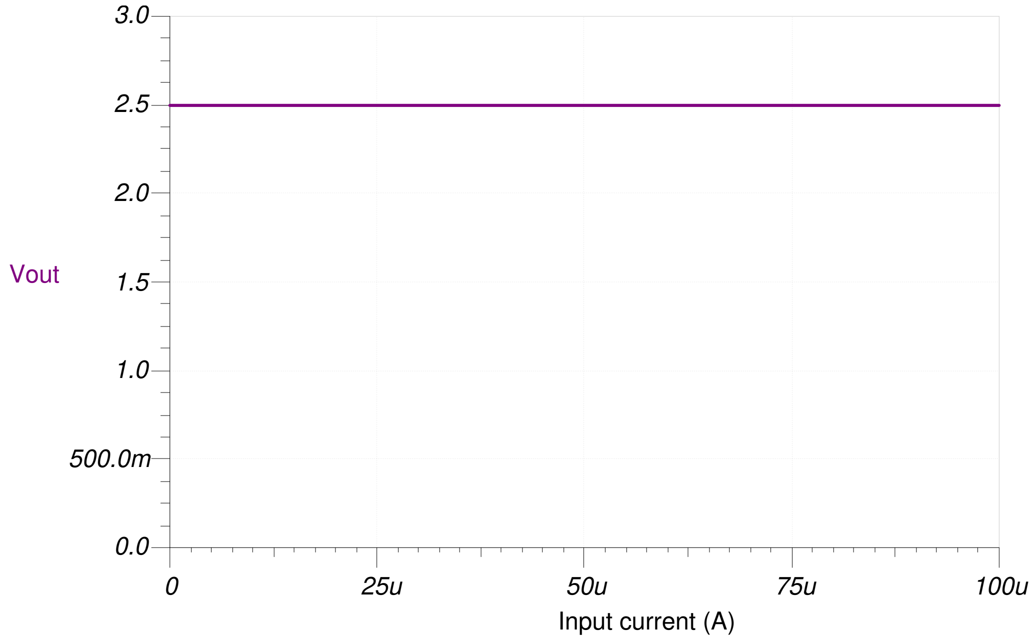
$$Vcm = \frac{R_6}{R_5 + R_6} \times Vcc = \frac{100k\Omega}{100k\Omega + 100k\Omega} \times 5V = 2.5V$$

7. Calculate capacitor C_2 to filter the power supply and resistor noise. Set the cutoff frequency to 1Hz.

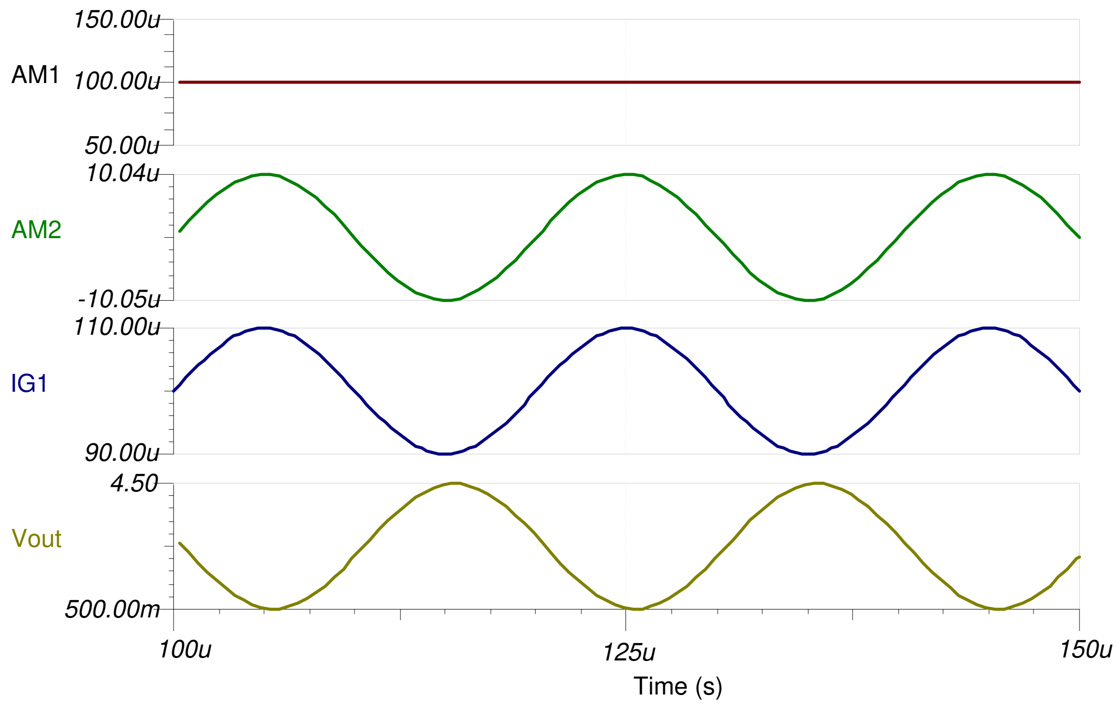
$$C_2 = \frac{1}{2\pi \times (R_2 || R_3) \times 1Hz} = \frac{1}{2\pi \times (100k\Omega || 100k\Omega) \times 1Hz} = 3.183\mu F \approx 4.7\mu F$$

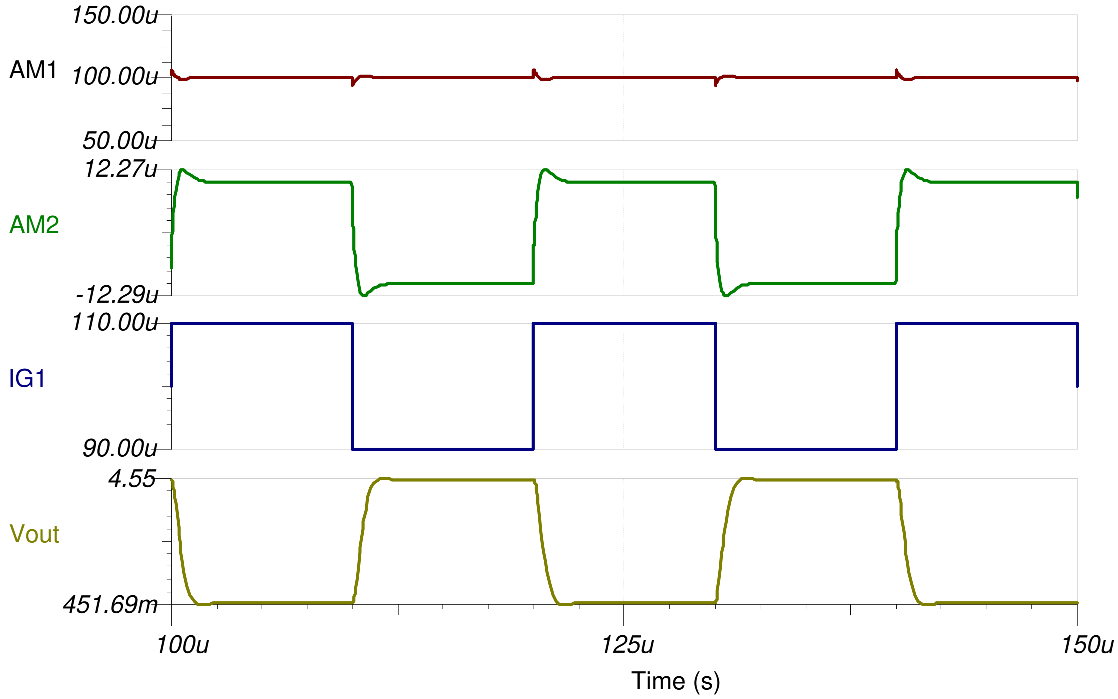
Design Simulations

DC Simulation Results

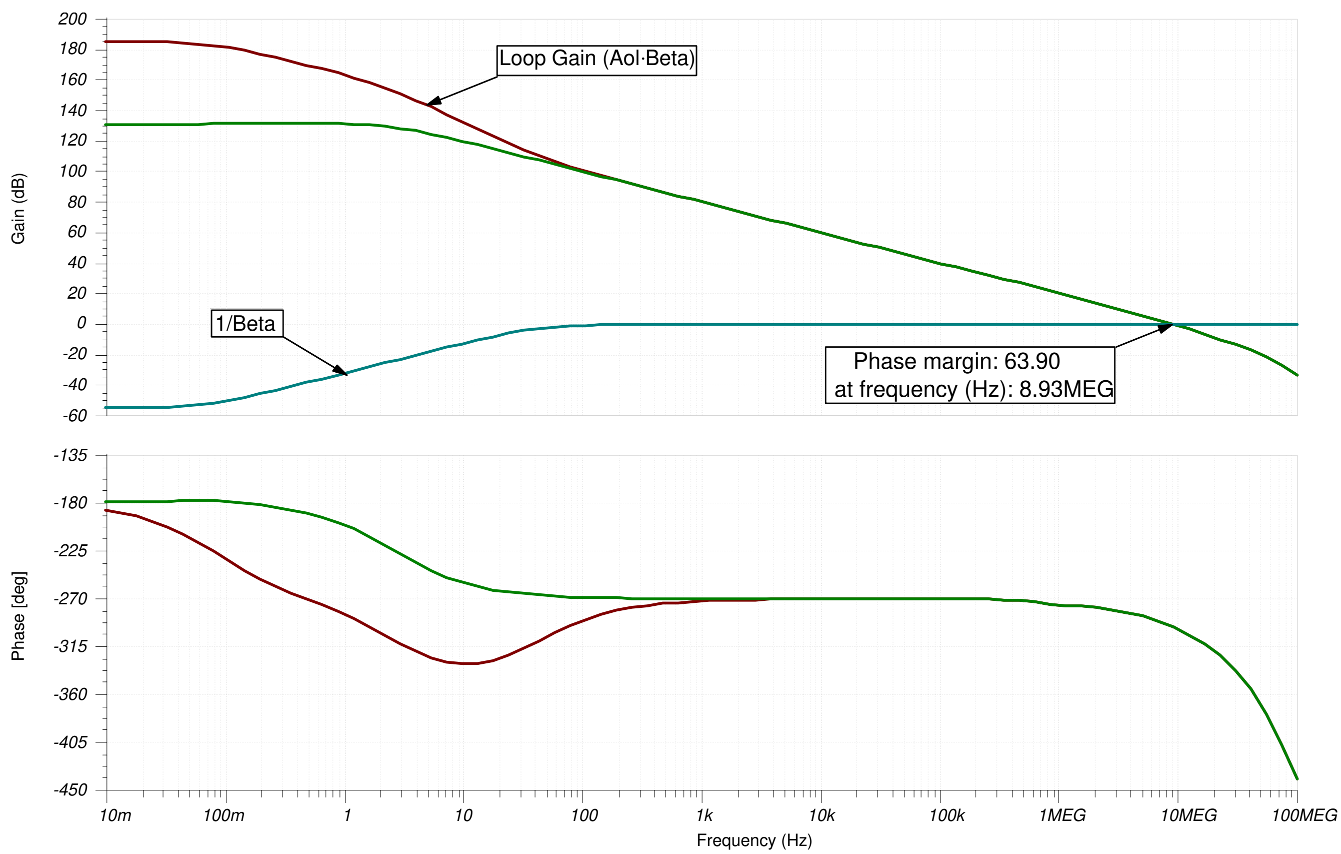


Transient Simulation Results

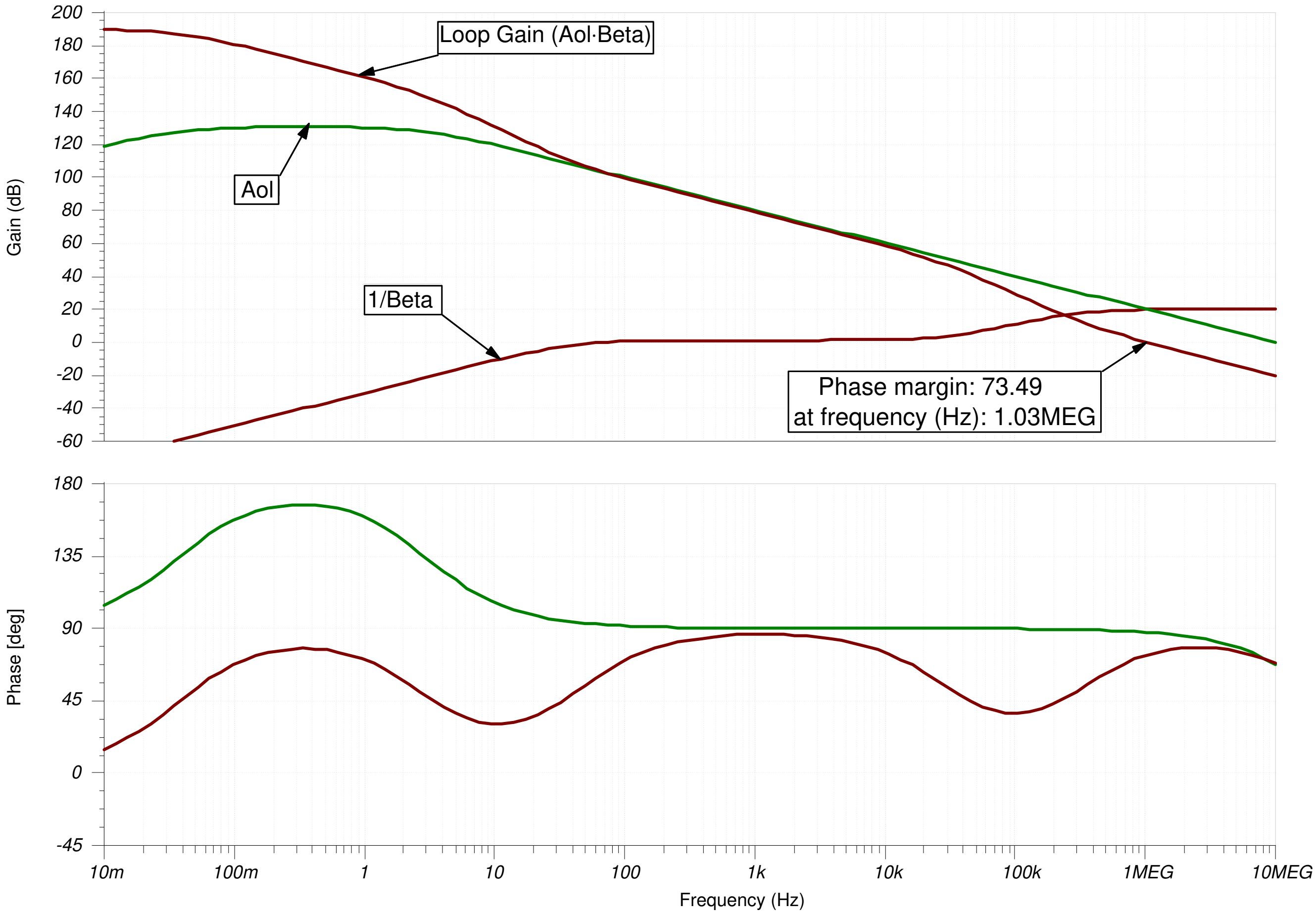




Integrator Open Loop Stability



TIA Stability Results



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. TI Precision Labs

Design Featured Op Amp

OPA172	
V_{cc}	±2.25V to ±18V, 4.5V to 36V
V_{inCM}	(V–) – 0.1V to (V+) – 2V
V_{out}	Rail-to-rail
V_{os}	0.2mV
I_q	1.6mA
I_b	8pA
UGBW	10MHz
SR	10V/µs
#Channels	1,2,4
www.ti.com/product/OPA172	

Design Alternate Op Amps

	OPA2991	TLV9042
V_{ss}	±1.35V to ±20V, 2.7V to 40V	±0.6V to ±2.75V, 1.2V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	125µV	0.6mV
I_q	560µV	10uA
I_b	1pA	1pA
UGBW	4.5MHz	350kHz
SR	20V/µs	0.2V/us
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/OPA2991	www.ti.com/product/TLV9042

Analog Engineer's Circuit

Transimpedance amplifier with T-network circuit

TEXAS INSTRUMENTS

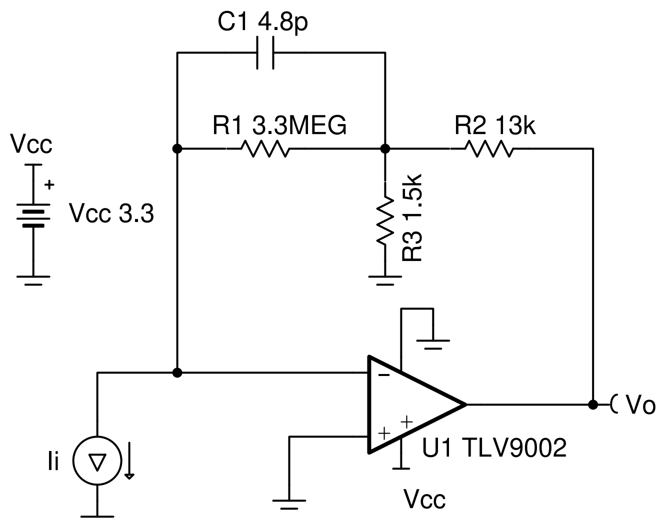
Amplifiers

Design Goals

Input		Output		BW	Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}
0A	100nA	0V	3.2V	10kHz	3.3V	0V

Design Description

This transimpedance amplifier with a T-network feedback configuration converts an input current into an output voltage. The current-to-voltage gain is based on the T-network equivalent resistance which is larger than any of the resistors used in the circuit. Therefore, the T-network feedback configuration circuit allows for very high gain without the use of large resistors in the feedback or a second gain stage, reducing noise, stability issues, and errors in the system.



Design Notes

1. C_1 and R_1 set the input signal cutoff frequency, f_p.
2. Capacitor C_1 in parallel with R_1 helps limit the bandwidth, reduce noise, and also improve the stability of the circuit if high-value resistors are used.
3. The common-mode voltage is the voltage at the non-inverting input and does not vary with input current.
4. A bias voltage can be added to the non-inverting input to bias the output voltage above the minimum output swing for 0A input current.
5. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
6. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth see the *Design References* section.

Design Steps

The transfer function of this circuit follows:

$$V_o = I_i \times \left(\frac{R_2 \times R_1}{R_3} + R_1 + R_2 \right)$$

1. Calculate the required gain:

$$\text{Gain} = \frac{V_{oMax}}{I_{oMax}} = \frac{3.2V}{100nA} = 3.2 \times 10^7 \frac{V}{A}$$

2. Choose the resistor values to set the pass-band gain:

$$\text{Gain} = \left(\frac{R_2 \times R_1}{R_3} + R_1 + R_2 \right)$$

   Since R_1 will be the largest resistor value in the system choose this value first then choose R_2 and calculate R_3. Select R_1 = 3.3MΩ and R_2 = 13kΩ. R_1 is very large due to the large transimpedance gain of the circuit. R_2 is in the ~10k ohm range so the op amp can drive it easily.

$$R_3 = \left(\frac{R_2 \times R_1}{\text{Gain} - R_1 - R_2} \right) = \left(\frac{13k\Omega \times 3.3M\Omega}{3.2 \times 10^7 \frac{V}{A} - 3.3M\Omega - 13k\Omega} \right) = 1.5k\Omega$$

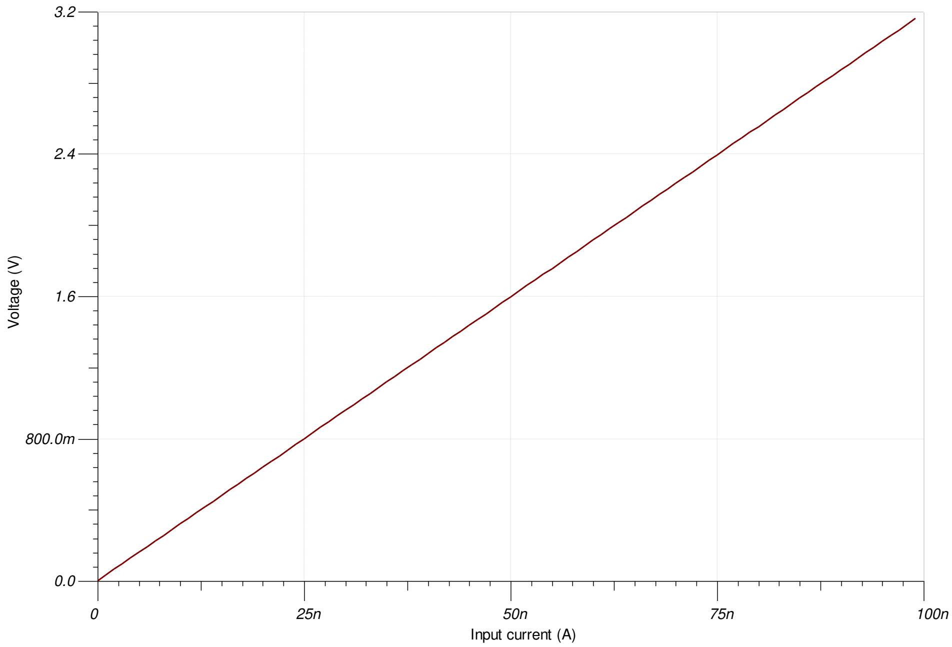
3. Calculate C_1 to set the location of f_p.

$$C_1 = \frac{1}{2\,\pi \times R_1 \times f_p} = \frac{1}{2\pi \times 3.3M\Omega \times 10kHz} = 4.82pF \approx 4.8pF \text{ (Standard Value)}$$

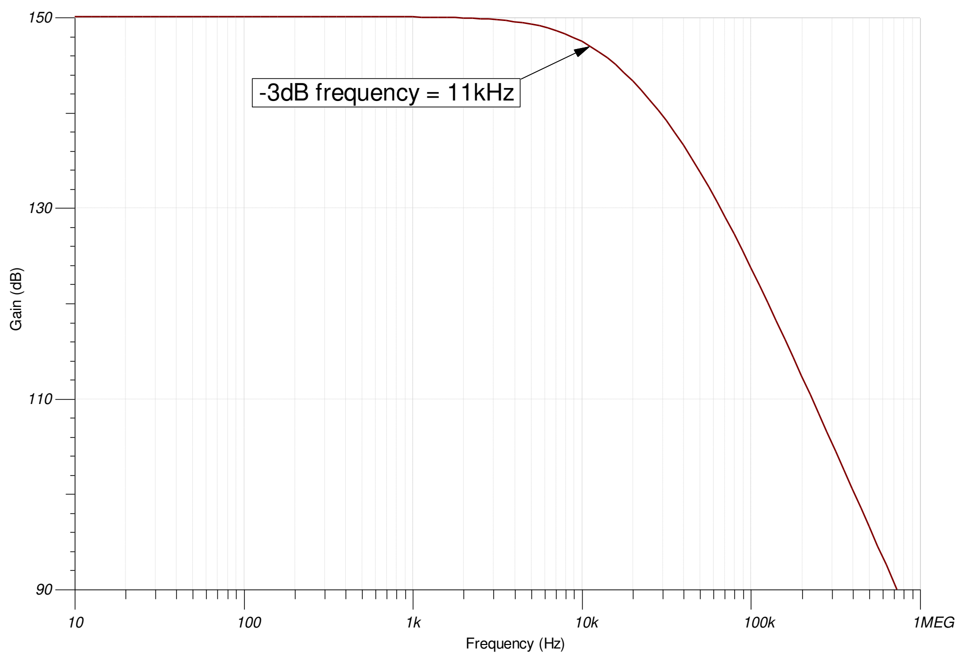
4. Run a stability analysis to make sure that the circuit is stable. For more information on how to run a stability analysis see the *TI Precision Labs - Op amp: Stability* video.

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. See SPICE file, SBOMB39.
3. See TIPD176, www.ti.com/tool/tipd176.
4. For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC please visit TI Precision Labs.

Design Featured Op Amp

TLV9002	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail–to–rail
V_{os}	0.4mV
I_q	60µA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9002	

Design Alternate Op Amp

OPA375	
V_{cc}	2.25V to 5.5V
V_{inCM}	V_{ee} to (V_{cc} –1.2V)
V_{out}	Rail–to–rail
V_{os}	0.15mV
I_q	890µA
I_b	10pA
UGBW	10MHz
SR	4.75V/µs
#Channels	1
www.ti.com/product/OPA375	

Low-Drift, Low-Side, Bidirectional Current Sensing Circuit with Integrated Precision Gain

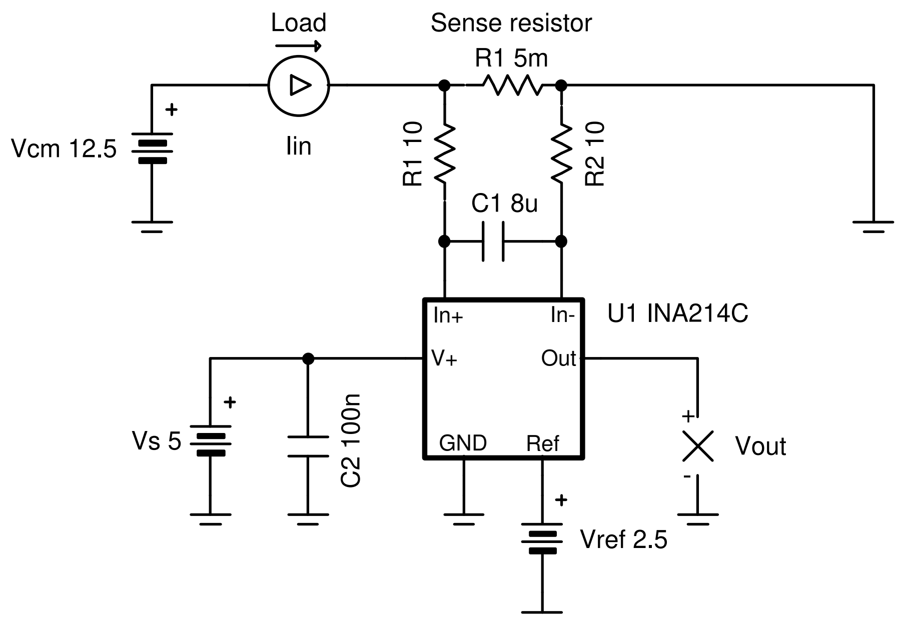
TEXAS INSTRUMENTS

Design Goals

Input			Output		Supply	
I_{inMin}	I_{inMax}	V_{cm}	V_{outMin}	V_{outMax}	V_s	V_{ref}
–4A	4A	12.5 V	0.5 V	4.5 V	5	2.5 V

Design Description

The low-side bidirectional current-shunt monitor solution illustrated in the following image can accurately measure currents from –4A to 4A, and the design parameters can easily be changed for different current measurement ranges. Current-shunt monitors from the INA21x family have integrated precision gain resistors and a zero-drift architecture that enables current sensing with maximum drops across the shunt as low as 10mV full-scale.



Design Notes

- To avoid additional error, use $R_1 = R_2$ and keep the resistance as small as possible (no more than 10Ω, as stated in *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*).
- Low-side sensing should not be used in applications where the system load cannot withstand small ground disturbances or in applications that need to detect load shorts.
- The *Getting Started with Current Sense Amplifiers* video series introduces implementation, error sources, and advanced topics that are good to know when using current sense amplifiers.

Design Steps

1. Determine V_{ref} based on the desired current range:

   With a current range of –4A to 4A, then half of the range is below 0V, so set:

$$V_{ref} = \frac{1}{2} V_s = \frac{5}{2} = 2.5\,V$$

2. Determine the desired shunt resistance based on the maximum current and maximum output voltage:

   To not exceed the swing-to-rail and to allow for some margin, use V_{outMax} = 4.5V. This, combined with maximum current of 4A and the V_{ref} calculated in step 1, can be used to determine the shunt resistance using the equation:

$$R_1 = \frac{V_{outMax} - V_{ref}}{\text{Gain} \times I_{loadMax}} = \frac{4.5 - 2.5}{100 \times 4} = 5\,m\Omega$$

3. Confirm V_{out} will be within the desired range:

   At the maximum current of 4A, with Gain = 100V/V, R_1 = 5mΩ, and V_{ref} = 2.5V:

$$V_{out} = I_{load} \times \text{Gain} \times R_1 + V_{ref} = 4 \times 100 \times 0.005 + 2.5 = 4.5\,V$$

   At the minimum current of -4A, with Gain = 100V/V, R_1 = 5mΩ, and V_{ref} = 2.5V:

$$V_{out} = I_{load} \times \text{Gain} \times R_1 + V_{ref} = -4 \times 100 \times 0.005 + 2.5 = 0.5\,V$$

4. Filter cap selection:

   To filter the input signal at 1kHz, using $R_1 = R_2$ = 10Ω:

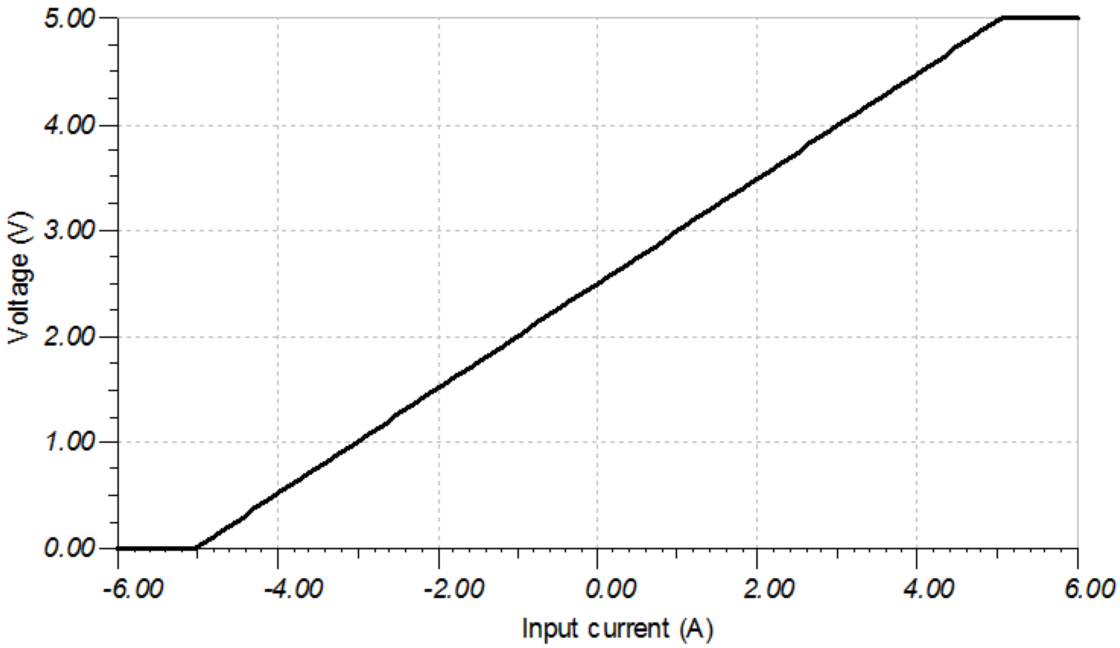
$$C_1 = \frac{1}{2\pi(R_1 + R_2)F_{-3\,dB}} = \frac{1}{2\pi(10 + 10)1000} = 7.958 \times 10^{-6} \approx 8\,\mu F$$

For more information on signal filtering and the associated gain error, see *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*.

Design Simulations

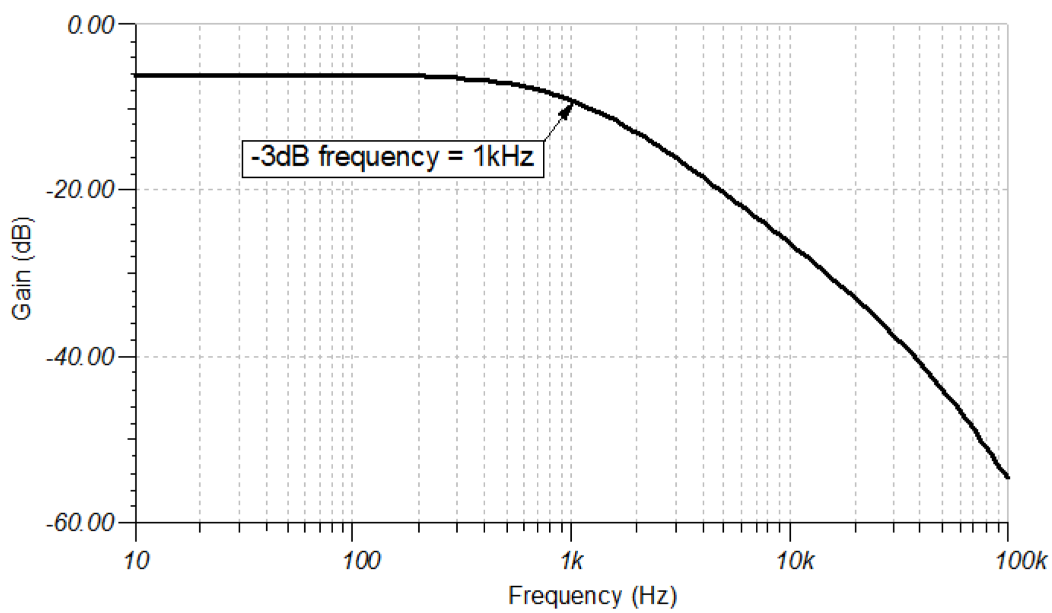
DC Analysis Simulation Results

The following plot shows the simulated output voltage V_{out} for the given input current I_{in}.



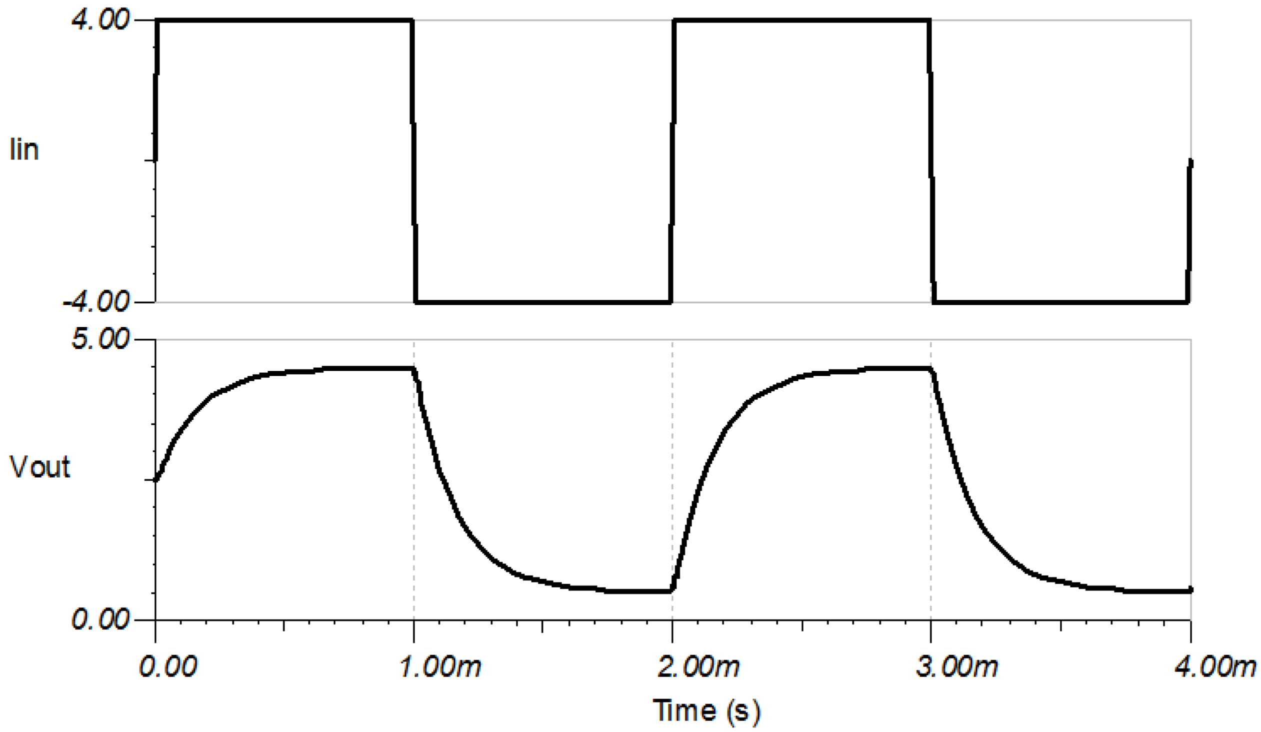
AC Analysis Simulation Results

The following plot shows the simulated gain vs frequency, as designed for in the design steps.



Transient Analysis Simulation Results

The following plot shows the simulated delay and settling time of the output V_{out} for a step response in I_{in} from –4A to 4A.



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Circuit SPICE simulation File: http://proddms.itg.ti.com/fnview/sboc518

Getting Started with Current Sense Amplifiers video series: https://training.ti.com/getting-started-current-sense-amplifiers

Current Sense Amplifiers on TI.com: http://www.ti.com/amplifier-circuit/current-sense/products.html

For direct support from TI Engineers use the E2E community: http://e2e.ti.com

Design Featured Current Sense Amplifier

INA214C	
V_s	2.7 V to 26 V
V_{cm}	GND-0.1 V to 26 V
V_{out}	GND-0.3V to V_s+0.3 V
V_{os}	±1μV typical
I_q	65μA typical
I_b	28μA typical
http://www.ti.com/product/INA214	

Design Alternate Current Sense Amplifiers

INA199C	
V_s	2.7 V to 26 V
V_{cm}	GND-0.1 V to 26 V
V_{out}	GND-0.3 V to V_s+0.3 V
V_{os}	±5μV typical
I_q	65μA typical
I_b	28μA typical
http://www.ti.com/product/INA199	

INA181	
V_s	2.7 V to 5.5 V
V_{cm}	GND-0.2 V to 26 V
V_{out}	GND-0.3 V to V_s+0.3 V
V_{os}	±100μV typical
I_q	65μA typical
I_b	195μA typical
http://www.ti.com/product/INA181	

Revision History

Revision	Date	Change
A	December 2020	Changed step three from "At the minimum current of 4A" to "At the minimum current of -4A"

Analog Engineer's Circuit

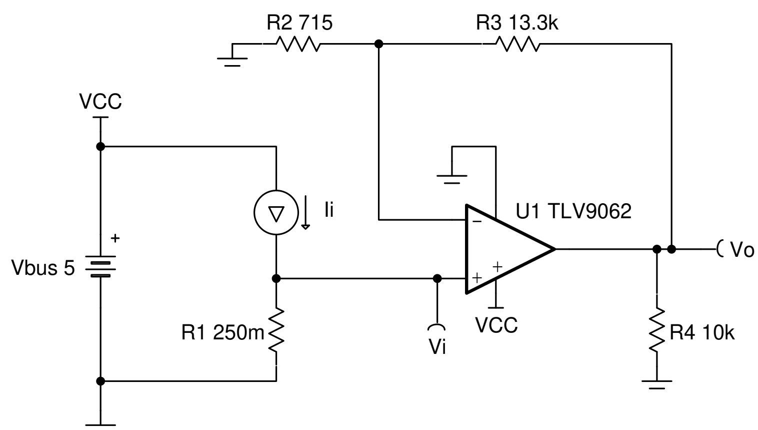
Single-supply, low-side, unidirectional current-sensing circuit

Design Goals

Input		Output		Supply		Full–Scale Range Error
I_{iMax}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	FSR_{Error}
1A	250mV	50mV	4.9V	5V	0V	0.2%

Design Description

This single–supply, low–side, current sensing solution accurately detects load current up to 1A and converts it to a voltage between 50mV and 4.9V. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings.



Design Notes

1. Use the op amp linear output operating range, which is usually specified under the test conditions.
2. The common–mode voltage is equal to the input voltage.
3. Tolerance of the shunt resistor and feedback resistors will determine the gain error of the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. If trying to detect zero current with output swing to GND, a negative charge pump (such as LM7705) can be used as the negative supply in this design to maintain linearity for output signals near 0V. [5]
6. Using high–value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
7. The small–signal bandwidth of this circuit depends on the gain of the circuit and gain bandwidth product (GBP) of the amplifier.
8. Filtering can be accomplished by adding a capacitor in parallel with R_3 . Adding a capacitor in parallel with R_3 will also improve stability of the circuit if high–value resistors are used.
9. For more information on op amp linear operating region, stability, capacitive load drive, driving ADCs, and bandwidth please see the Design References section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

1. Define the full–scale shunt voltage and calculate the maximum shunt resistance.

$$V_{iMax} = 250\ \text{mV} \quad \text{at} \quad I_{iMax} = 1\ \text{A}$$

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250\ \text{mV}}{1\ \text{A}} = 250\ \text{m}\ \Omega$$

2. Calculate the gain required for maximum linear output voltage.

$$V_{iMax} = 250\ \text{mV} \quad \text{and} \quad V_{oMax} = 4.9\ \text{V}$$

$$\text{Gain} = \frac{V_{oMax}}{V_{iMax}} = \frac{4.9\ \text{V}}{250\ \text{mV}} = 19.6\ \frac{\text{V}}{\text{V}}$$

3. Select standard values for R_2 and R_3.

   From Analog Engineer's calculator, use "Find Amplifier Gain" and get resistor values by inputting gain ratio of 19.6.

   R_2 = 715 Ω (0.1% Standard Value)

   R_3 = 13.3 kΩ (0.1% Standard Value)

4. Calculate minimum input current before hitting output swing–to–rail limit. I_{iMin} represents the minimum accurately detectable input current.

$$V_{oMin} = 50\ \text{mV}; \quad R_1 = 250\ \text{m}\ \Omega$$

$$V_{iMin} = \frac{V_{oMin}}{\text{Gain}} = \frac{50\ \text{mV}}{19.6\ \frac{\text{V}}{\text{V}}} = 2.55\ \text{mV}$$

$$I_{iMin} = \frac{V_{iMin}}{R_1} = \frac{2.55\ \text{mV}}{250\ \text{m}\ \Omega} = 10.2\ \text{mA}$$

5. Calculate Full scale range error and relative error. V_{os} is the typical offset voltage found in data sheet.

$$FSR_{error} = \left(\frac{V_{os}}{V_{iMax} - V_{iMin}}\right) \times 100 = \left(\frac{0.3\ \text{mV}}{247.45\ \text{mV}}\right) \times 100 = 0.121\ \%$$

$$\text{Relative Error at } I_{iMax} = \left(\frac{V_{os}}{V_{iMax}}\right) \times 100 = \left(\frac{0.3\ \text{mV}}{250\ \text{mV}}\right) \times 100 = 0.12\ \%$$

$$\text{Relative Error at } I_{iMin} = \left(\frac{V_{os}}{V_{iMin}}\right) \times 100 = \left(\frac{0.3\ \text{mV}}{2.5\ \text{mV}}\right) \times 100 = 12\ \%$$

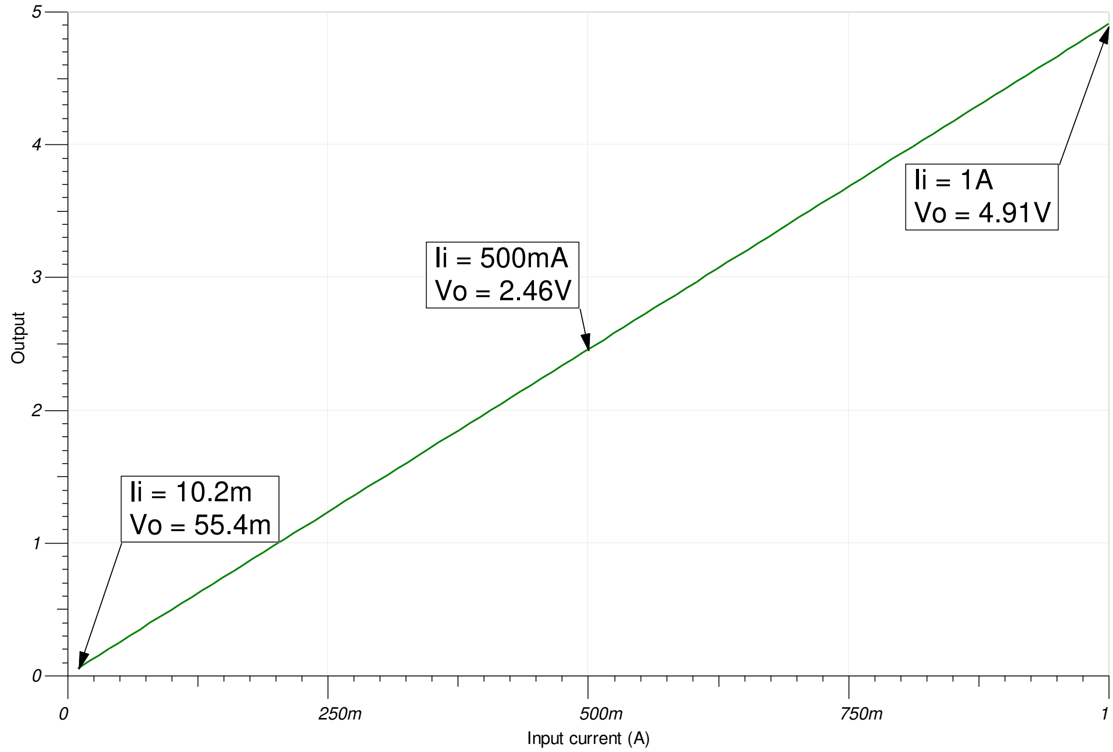
6. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_2 || R_3)} > \frac{GBP}{G}$$

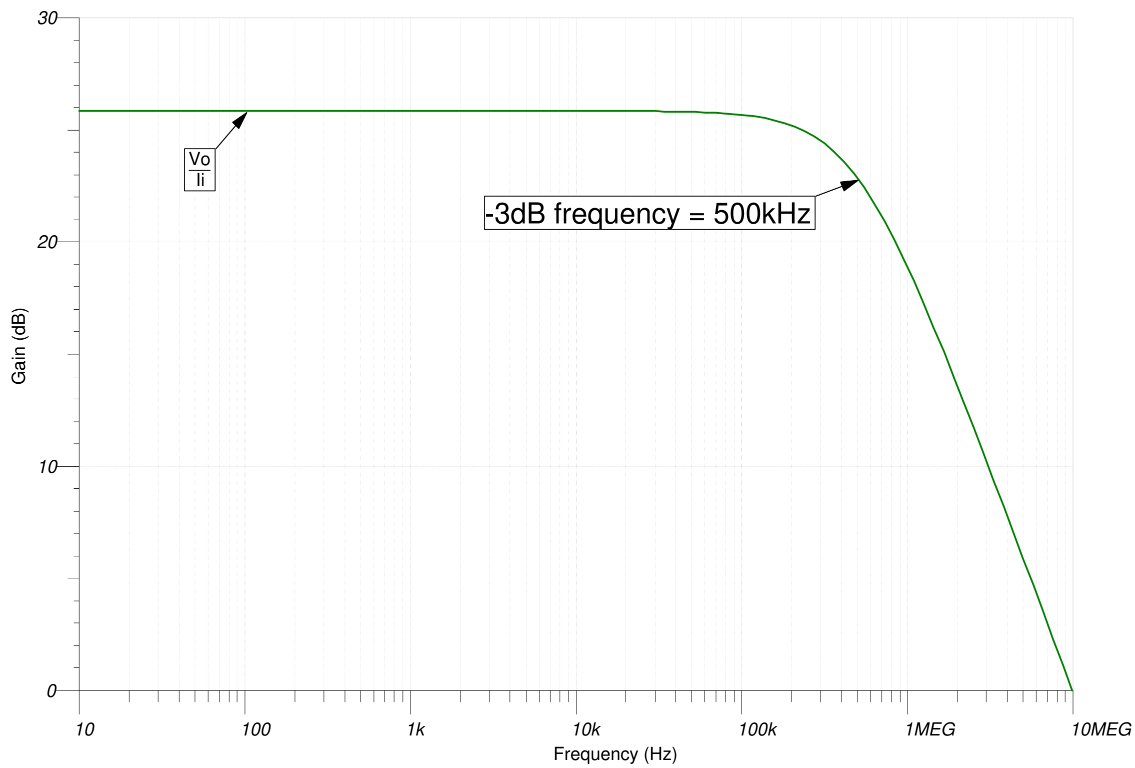
$$\frac{1}{2 \times \pi \times (3\text{pF} + 3\text{pF}) \times \left(\frac{715\ \Omega \times 13.3\ \text{k}\Omega}{715\ \Omega + 13.3\ \text{k}\Omega}\right)} > \frac{10\ \text{MHz}}{19.6\ \frac{V}{V}} = 39.1\ \text{MHz} > 510\ \text{kHz}$$

Design Simulations

DC Simulation Results



AC Simulation Results



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOC523
3. TI Precision Designs TIPD129, TIPD104
4. TI Precision Labs
5. *Single-Supply, Low-Side, Unidirectional Current-Sensing Solution with Output Swing to GND Circuit*

Design Featured Op Amp

TLV9061	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1,2,4
www.ti.com/product/tlv9061	

Design Alternate Op Amp

OPA375	
V_{cc}	2.25V to 5.5V
V_{inCM}	(V–) to ((V+)–1.2V)
V_{out}	Rail–to–rail
V_{os}	0.15mV
I_q	890µA
I_b	10pA
UGBW	10MHz
SR	4.75V/µs
#Channels	1
www.ti.com/product/OPA375	

For battery operated or power conscious designs, outside of the original design goals described earlier, where lowering total system power is desired.

LPV821	
V_{cc}	1.7V to 3.6V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	1.5µV
I_q	650nA/Ch
I_b	7pA
UGBW	8kHz
SR	3.3V/ms
#Channels	1
www.ti.com/product/LPV821	

Analog Engineer's Circuit

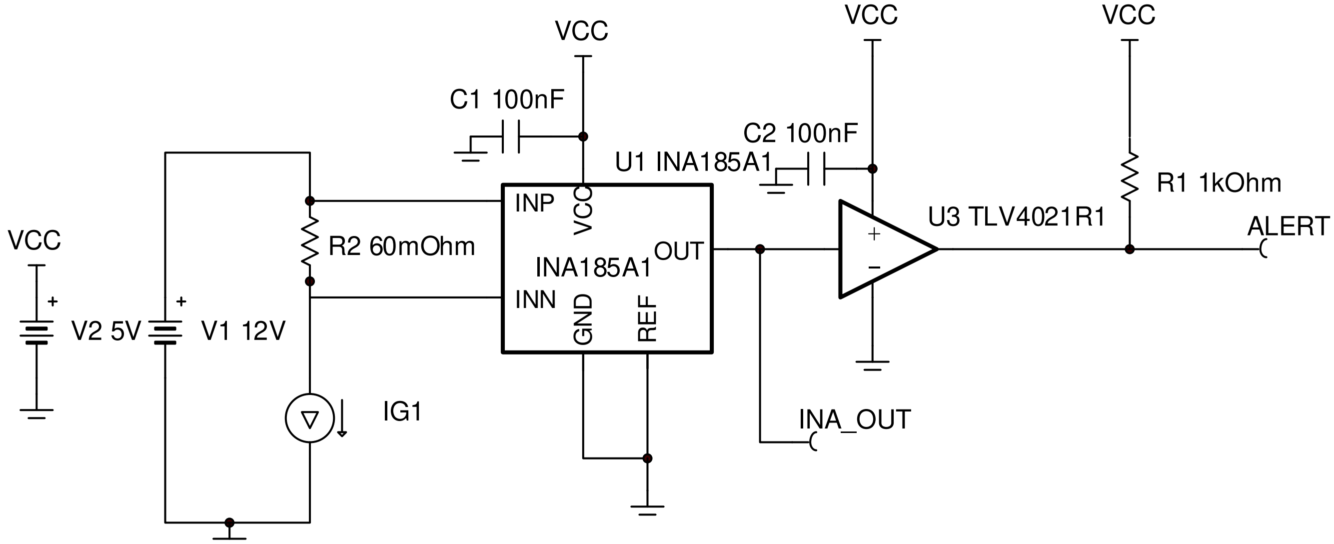
Fast-Response Overcurrent Event Detection Circuit

Design Goals

Input		Overcurrent Conditions		Output		Supply	
$I_{load\ Min}$	$I_{load\ Max}$	I_{OC_TH}	t_{resp}	V_{out_OC}	$V_{out\_release}$	V_S	V_{REF}
80 mA	900 mA	1 A	< 2 µs	1.2 V	1.18 V	5 V	0 V

Design Description

This is a fast-response unidirectional current-sensing solution, generally referred to as overcurrent protection (OCP), that can provide a < 2 µs time response, t_{resp}, overcurrent alert signal to power off a system exceeding a threshold current. In this particular setup, the normal operating load is from 80 mA to 900 mA, with the overcurrent threshold defined at 1 A (I_{OC_TH}). The current shunt monitor is powered from a 5 V supply rail. OCP can be applied to both high-side and low-side topologies. The solution presented in this circuit is a high-side implementation. This circuit is useful in smart speakers and docking stations.



Design Notes

1. Use decoupling capacitors C1 and C2 to ensure the device supply is stable. Place the decoupling capacitor as close to the device supply pin as possible.
2. If a larger dynamic current measurement range is required with a higher trip point, a voltage divider from the INA185 OUT pin to ground can be incorporated with the divider output going to the TLV4021R1 input.

Design Steps

1. Determine the slew rate, SR, needed to facilitate a fast enough response when paired with the propagation delay of a comparator. In this example, the TLV4021 device is selected as the external comparator due to its quick propagation delay (t_P = 450 ns) and its quick fall time (t_f = 4 ns). The worst case occurs when the load ramps from 0 A to 1 A ($\Delta V_{out} = V_{trip} - 0$ V). Device offset (V_{OS} × gain) can be subtracted from Vtrip in the numerator for less aggressive slew rates.

$$SR = \frac{\Delta V_{out}}{t_{resp} - t_P - t_F} = \frac{1.2V}{2\mu s - 450ns - 4ns} = 0.78V/\mu s$$

2. Choose a current shunt monitor with a slew rate greater than or equal 0.78 V/µs. The INA185 device satisfies the requirement with a typical slew of 2 V/µs.
3. For maximum headroom between the lowest measured current level and the overcurrent level, select the smallest gain variant of the chosen current shunt monitor. A 20 V/V current shunt monitor paired with 1.2 V comparator reference is adequate in this case.
4. Calculate the R_{shunt} value given 20 V/V gain. Use the nearest standard value shunt, preferably lower than the calculated shunt to avoid railing the output prematurely.

$$\mathrm{R_{shunt}} = \frac{\mathrm{V_{trip}}}{\mathrm{gain} \times \mathrm{I}_{trip}} = \frac{1.2\mathrm{V}}{20\mathrm{V/V} \times 1\mathrm{A}} = 0.06\Omega$$

$$\mathrm{R_{standard\ \ shunt}} = 60\mathrm{m}\Omega\ (\text{standard } 1\%\text{ value})$$

5. Check that the minimum meaningful current measurement is significantly higher than the current shunt monitor input offset voltage. The recommended maximum error from offset, $error_{VOS}$ is 10%.

$$\mathrm{I_{Device\ \_min}} = \frac{\mathrm{V}_{OS}}{\frac{\mathrm{error}_{V_{OS}}}{100} \times \mathrm{R}_{shunt}} = \frac{450\mu V}{\frac{10}{100} \times 0.06\Omega} = 75mA$$

6. Check that $I_{Load\ Max}$ is below the hysteresis threshold, $I_{Release\_TH}$, to ensure that the ALERT signal is cleared after the system has taken corrective action to bring the load back under the upper limit of the normal operating range. In this case there is 83mA of margin between the 900 mA normal operating region maximum and the hysteresis level imposed by the comparator.

$$\mathrm{I_{Release\ \_TH}} = \frac{\mathrm{V}_{trip} - 20mV}{\mathrm{gain} \times \mathrm{R}_{shunt}} = \frac{1.2V - 20mV}{20V/V \times 0.06\Omega} = 0.983A$$

Design Simulations

DC Simulation Results

The DC transfer characteristic curve confirms that the OCP trigger occurs from a 1 A load.

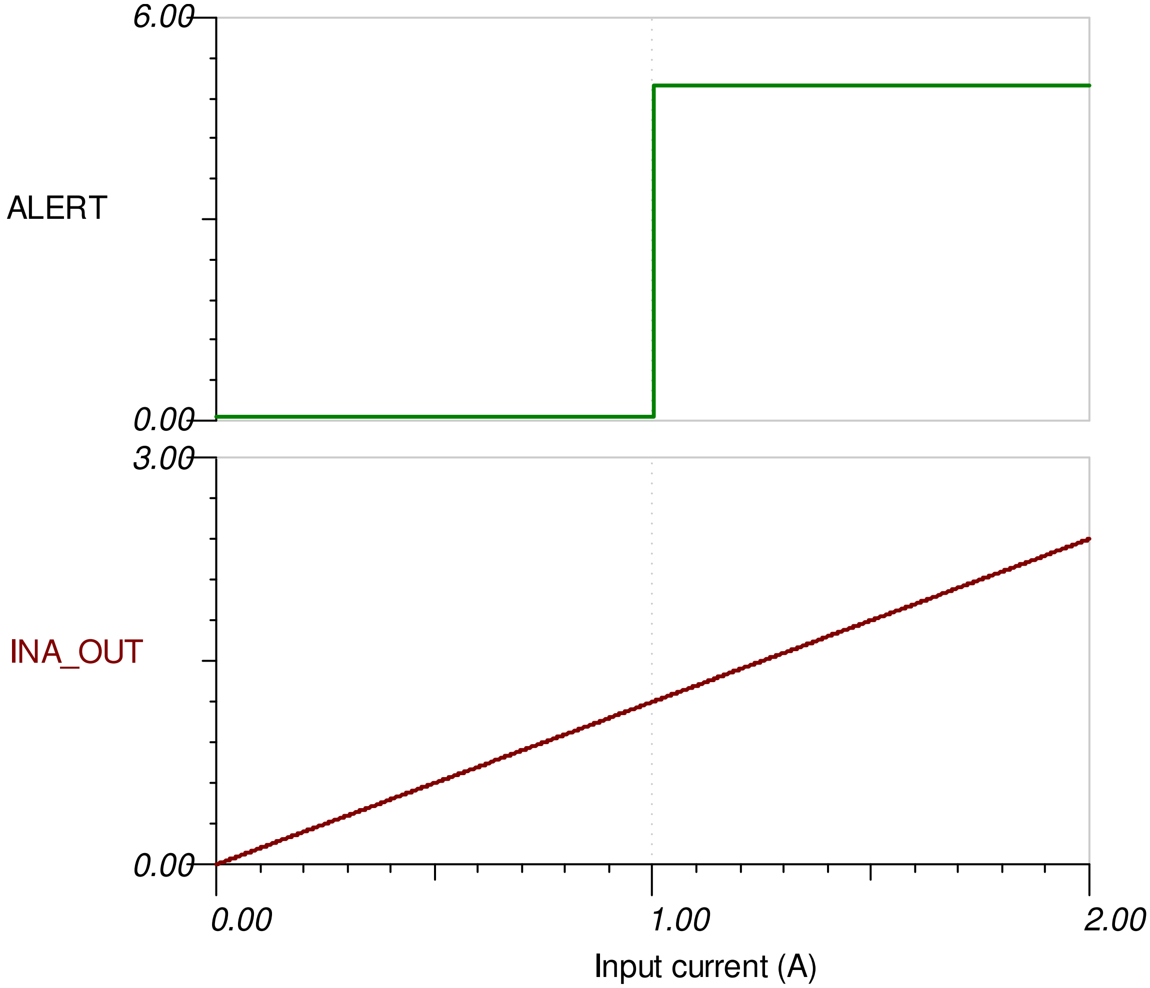
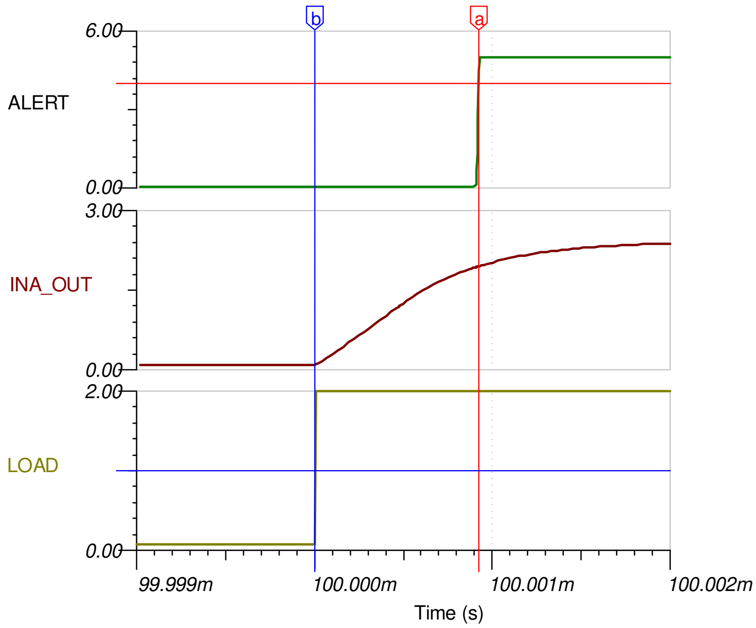


Figure 1-1.

Transient Simulation Results

The following result confirms that the INA185 device paired with the TLV4021 device can trigger an ALERT within 2 µs of the overcurrent threshold being exceeded. In this case, a typical value of almost 1µs is achieved. Please keep in mind that models used in these simulations are designed around typical device characteristics. Real-world performance many vary based on normal device variations.



A				
	x:	100.0009289184ms	y:	4 V
B				
	x:	100.00001ms	y:	1 A
A-B				
	x:	918.9184ns	y:	

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Key Files for Overcurrent Protection Circuit

Source files for this design:

High-Side OCP Tina Model

Low-Side OCP Tina Model

Getting Started With Current Sense Amplifiers Video Series

Getting started with current sense amplifiers

Design Featured Current Sense Amplifier

INA185	
V_S	2.7 V to 5.5 V
V_{CM}	GND-0.2 V to 26 V
V_{OUT}	GND + 500 µV to V_S – 0.02 V
Gain	20 V/V, 50 V/V, 100 V/V, 200 V/V
V_{OS}	±100 µV typical
SR	2 V/µs typical
I_q	200 µA typical
I_B	75 µA typical
INA185	

Design Alternate Current Sense Monitor

	INA181	INA180
V_S	2.7 V to 5.5 V	2.7 V to 5.5 V
V_{CM}	GND-0.2 V to 26 V	GND-0.2 V to 26 V
V_{OUT}	GND + 500 µV to V_S – 0.02 V	GND + 500 µV to V_S – 0.02 V
Gain	20 V/V, 50 V/V, 100 V/V, 200 V/V	20 V/V, 50 V/V, 100 V/V, 200 V/V
V_{OS}	±100 µV typical	±100 µV typical
SR	2 V/µs typical	2 V/µs typical
I_q	195 µA typical	197 µA typical
I_B	75 µA typical	80 µA typical
	INA181	INA180

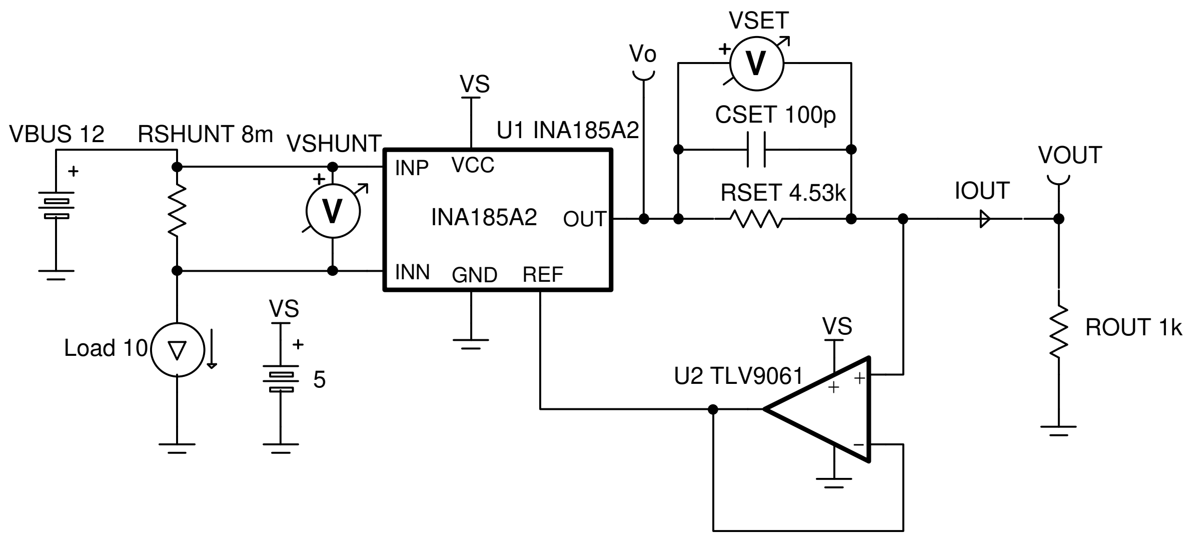
Analog Engineer’s Circuit Amplifiers

Adjustable-gain, current-output, high-side current-sensing circuit

Input			Output			Error	Supply		
$I_{LOAD\ Min}$	$I_{LOAD\ Max}$	V_{CM}	$I_{OUT\ Min}$	$I_{OUT\ Max}$	Bandwidth	at $I_{LOAD\ Min}$	$I_{Q\ Max}$	V_S	V_{ee}
1A	10A	12V	88.3μA	883μA	200kHz	2.2% maximum, 0.3% typical	260 + 750μA	5V	GND (0V)

Design Description

This circuit demonstrates how to convert a voltage-output, current-sense amplifier (CSA) into a current-output circuit using an operational amplifier (op amp) and a current-setting resistor (R_{SET}). Taking advantage of the matched internal resistor gain network of the current-sense amplifier, this circuit utilizes the Howland Current Pump method to create a current source that is proportional to the sense current. The overall circuit gain is adjustable by changing the load resistor value (R_{OUT}). Additionally, multiple circuits can be summed together to determine total current from multiple sources.



Design Notes

1. The *Getting Started with Current Sense Amplifiers* video series introduces implementation, error sources, and advanced topics for using current sense amplifiers.
2. Choose precision 0.1% resistors to limit gain error at higher currents.
3. The output current (I_{OUT}) is sourced from the VS supply, which adds to the I_Q of the current sense amplifier.
4. Use the V_{OUT} versus I_{OUT} curve ("claw-curve") of the CSA (U1) to set the I_{OUT} limit during I_{LOAD_Max}. If a higher amount of current is needed, then consider adding a buffer to the output of the current sense amplifier. A buffer on the output allows for smaller R_{OUT}.
5. For applications with higher bus voltages, simply substitute in a bidirectional current sense amplifier with a higher rated input voltage.
6. The V_{OUT} voltage is the input common-mode voltage (V_{CM}) for the op amp.
7. Offset errors can be calibrated out with one-point calibration given that a known sense current is applied and the circuit is operating in the linear region. Gain error calibration requires a two-point calibration.
8. Include a small feed-forward capacitor (C_{SET}) to increase BW and decrease V_{OUT} settling time to a step response in current. Increasing C_{SET} too much introduces gain peaking in the system gain curve, which results in output overshoot to a step response.
9. Multiple circuits can sum their current outputs into a single load resistor, but note that the headroom voltage for each individual circuit will decrease. The INA2181 and INA4181 devices are multi-channel CSAs that have similar performance to the INA185 device.
10. Follow best practices for printed-circuit board (PCB) layout according to the data sheet: decoupling capacitor close to the VS pin, routing the input traces for IN+ and IN– as a differential pair, and so forth.

Design Steps

1. To satisfy system requirements, the minimum shunt (V_{SHUNT_MIN}) voltage value must be sufficiently greater than the known offsets of the amplifiers. Here is the equation for the worst-case maximum output current:

$$I_{OUT\_MAX\_Worst-Case} \quad \frac{V_{SET\_MAX}}{R_{SET} \cdot (1 - Tolerance_{Rset})}$$

$$I_{OUT\_MAX\_Worst-Case} \quad \frac{Gain_{INA185} \cdot (1 + GainError) \cdot \left[V_{SHUNT\_MIN} + V_{OS\_INA185}\right] + V_{OS\_TLV9061}}{R_{SET} \cdot (1 - Tolerance_{Rset})}$$

2. Since offset errors dominate at the low currents, negate resistor tolerance and gain error for establishing V_{SHUNT_MIN}. Set the error of V_{SET} to 2.2% to determine the following condition:

$$V_{SHUNT\_MIN} > \left(\frac{1}{2.2\%}\right) \cdot \left\{V_{OS\_INA185} + \frac{V_{OS\_TLV9061}}{Gain_{INA185}}\right\}$$

3. V_{OUT_MIN} also needs to be large enough so the common-mode voltage (V_{CM}) and output voltage ($V_{OUT\_TLV9061}$) of the TLV9061 device are in the optimal operating region. The TLV9061 device is a rail-to-rail-input-output (RRIO) op amp so it can operate with very small V_{CM} and output voltages, but A_{OL} will vary. Testing conditions for data sheet CMRR and A_{OL} show that choosing V_{OUT_MIN} > 50 mV will provide sufficient A_{OL} when circuit sensing minimum load current.

$$V_{OUT\_TLV9061} \quad V_{CM\_TLV9061} \quad V_{OUT}$$

$$V_{OUT\_MIN} > 50\,mV \text{ for good TLV9061 } A_{OL}$$

4. The scaling of R_{OUT} and R_{SET} can be determined by setting three parameters: V_{O_MAX}, I_{OUT_MAX}, and R_{OUT}. It is critical that I_{OUT_MAX} does not exceed the driving capability of the CSA or else V_{O_MAX} will droop and the circuit will loose headroom voltage. Use the swing-to-rail specification and the V_{OUT} versus I_{OUT} data sheet curve to determine optimal values.
   a. Choose V_{O_MAX} = 4.9V
   b. Choose I_{OUT_MAX} = 900µA

c. Choose R_{OUT} = 1kΩ

5. Using the system of equations for V_{OUT}, solve for R_{SET}. Choose the closest larger 1% resistor value. Note that rounding up the R_{SET} value will decrease the I_{OUT_MAX} from initially chosen 900µA.

$$V_{SET\_MAX} \quad I_{OUT\_MAX} \cdot R_{SET}$$

$$V_{OUT\_MAX} \quad I_{OUT\_MAX} \cdot R_{OUT}$$

$$V_{OUT\_MAX} \quad V_{O\_MAX} - V_{SET\_MAX}$$

$$R_{SET} \quad \frac{V_{O\_MAX} - I_{OUT\_MAX} \cdot R_{OUT}}{I_{OUT\_MAX}} \quad 4444.3\Omega$$

$$R_{SET} \quad 4530\Omega,\ 1\%$$

6. Now choose an INA185 gain variant and solve for R_{SHUNT}. Choose a 1% resistor value. Note that R_{SET} is independent of gain and R_{SHUNT} can be calculated for each gain variant.

$$V_{OUT\_MAX} \quad I_{OUT\_MAX} \cdot R_{OUT} \quad 900\,mV$$

$$V_{SET\_MAX} \quad V_{O\_MAX} - V_{OUT\_MAX} \quad 4V$$

$$V_{IN\_MAX} \quad \frac{V_{SET\_MAX}}{Gain_{INA185A2}} \quad \frac{4V}{50\frac{V}{V}} \quad 80\,mV$$

$$R_{SHUNT} \quad \frac{V_{IN\_MAX}}{I_{LOAD\_MAX}} \quad \frac{80\,mV}{10\,A}$$

$$R_{SHUNT} \quad 8\,m\Omega$$

7. Now check if V_{OUT_MIN} and V_{SHUNT_MIN} are large enough to achieve 2% error at 1A with updated values. Use the maximum offset specifications of the devices when calculating error.

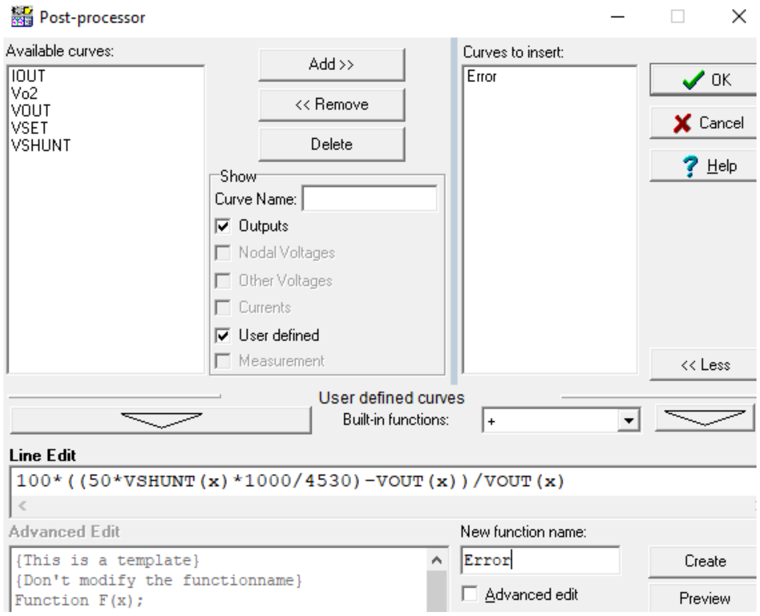
$$V_{SHUNT\_MIN} > \left(\frac{1}{2.2\%}\right) \cdot \left\{V_{OS\_INA185A2} + \frac{V_{OS\_TLV9061}}{GAIN_{INA185A2}}\right\} \quad 45.45 \cdot \left\{130\mu V + \frac{2mV}{50\frac{V}{V}}\right\} \quad 7.73\,mV$$

$$V_{SHUNT\_MIN} \quad 1A \cdot 8m\Omega = 8mV > 7.73mV$$

$$V_{OUT\_MIN} \quad V_{SHUNT\_MIN} \cdot Gain_{INA185A2} \cdot \frac{R_{OUT}}{R_{SET}}$$

$$V_{OUT\_MIN} \quad 8mV \cdot 50\frac{V}{V} \cdot \frac{1k\Omega}{4.53k\Omega} \quad 88\,mV > 50\,mV$$

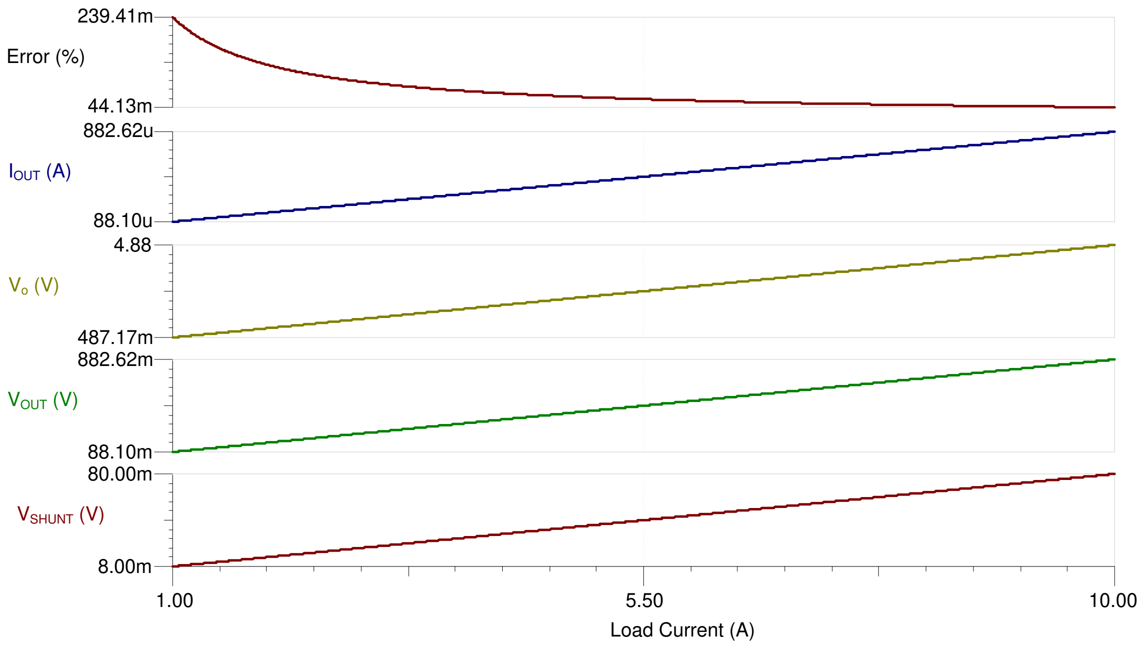
8. Run a simulation in TINA-TI software using available models. Note that these models use typical specifications. Calculate *Error* in the TINA-TI *Post-processor* window.



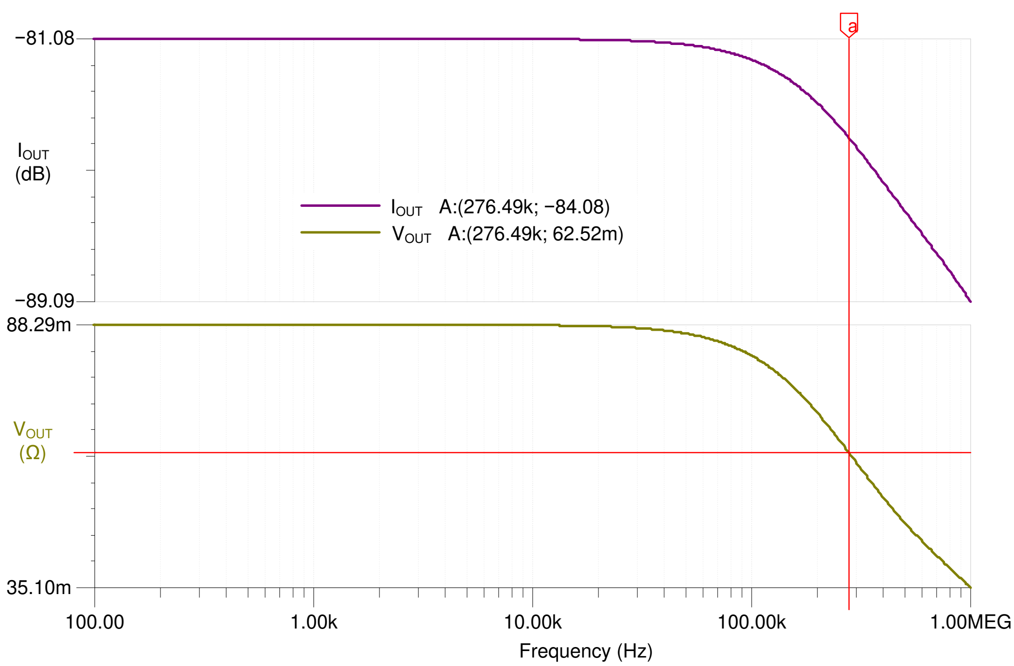
Design Simulations

DC Simulation Results

The following graph shows a linear output response for load currents from 1A to 10A.



AC Simulation Result – I_{LOAD} to I_{OUT} (V_{OUT}) circuit gain



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOMAI6.

Getting Started with Current Sense Amplifiers video series

https://training.ti.com/getting-started-current-sense-amplifiers

Current Sense Amplifiers on TI.com

http://www.ti.com/amplifier-circuit/current-sense/products.html

Comprehensive Study of the Howland Current Pump

http://www.ti.com/analog/docs/litabsmultiplefilelist.tsp?literatureNumber=snoa474a&docCategoryId=1&familyId=78

For direct support from TI Engineers use the E2E community

http://e2e.ti.com

Design Featured Current Sense Amplifier

INA185A2	
V_S	2.7V to 5.5V (operational)
V_{CM}	0V to 26V
Swing to V_S (V_{SP})	V_S – 0.02V
V_{OS}	±25μV to ±130μV at 12V V_{CM}
I_Q	200μA to 260μA
I_{IB}	75μA at 12V
BW	210kHz at 50V/V (A2 gain variant)
# of channels	1
Body size (including pins)	1.60 mm × 1.60 mm
http://www.ti.com/product/ina185	

Design Featured Operational Amplifier

TLV9061 (TLV9061S is shutdown version)	
V_S	1.8V to 5.5V
V_{CM}	(V–) – 0.1V < V_{CM} < (V+) + 0.1V
CMRR	103dB
A_{OL}	130dB
V_{OS}	±1.6mV maximum
I_Q	750μA maximum
I_B (input bias current)	± 0.5pA
GBP (gain bandwidth product)	10MHz
# of channels	1 (2 and 4 channel packages available)
Body size (including pins)	0.80 mm × 0.80 mm
http://www.ti.com/product/tlv9061	

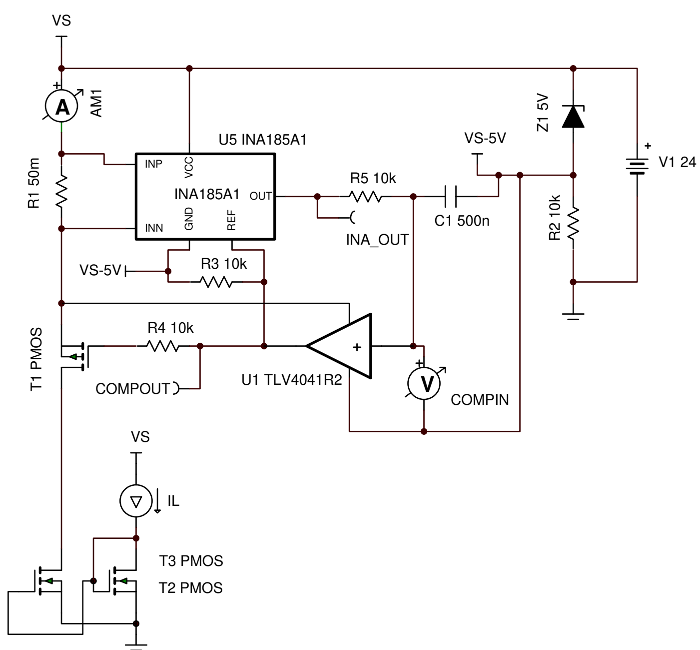
Current Limiting with Comparator Circuit

Design Goals

LOAD CURRENT (I_L)	SYSTEM SUPPLY (V_S)	CURRENT SENSE AMP	COMPARATOR OUTPUT STATUS	
Over Current (I_{OC})	Typical	Gain	Over Current	Normal Operation
200 mA	24 V	20 V/V	$V_{OH} = V_S$	$V_{OL} = V_S - 5$ V

Design Description

This high-side, current sensing solution uses a current sense amplifier, a comparator with an integrated reference, and a P-channel MOSFET to create an over-current latch circuit. When a load current greater than 200 mA is detected, the circuit disconnects the system from its power source. Since the comparator drives the gate of the P-channel MOSFET and feeds the signal back into the reference pin of the current sense amplifier, the comparator output will latch (hold the gate source voltage of the P-channel MOSFET to 0 V) until power to the circuit is cycled.



Design Notes

1. Select a precision, current sense amplifier (INA) with an external reference pin so its output voltage can be adjusted.
2. Select a comparator with a rail-to-rail input so its output will be valid over the entire operating voltage range of the current sense amplifier.
3. Select a comparator with a push-pull output stage that can drive the gate of a MOSFET and an integrated reference to optimize circuit accuracy.
4. Create a floating 5 V supply that can power the INA and comparator.

Design Steps

1. Select the value of R_1 so V_{SHUNT} is at least 100x greater than the current sense amplifier input offset voltage (V_{OS}). Note that making R_6 very large will improve OC detection accuracy but will reduce supply headroom and power dissipation.

$$V_{SHUNT} = (I_{OC} \times R_1) \geq 100 \times V_{OS}$$

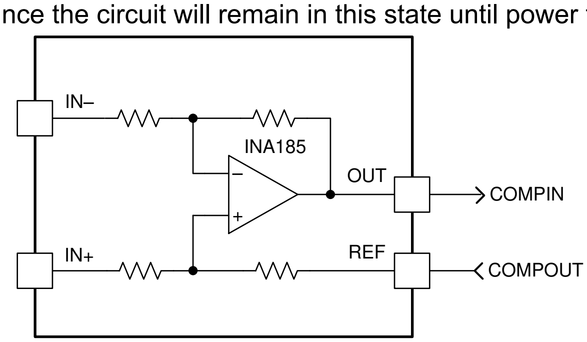
$$\text{Set} \quad R_1 \geq \frac{100 \times V_{OS}}{I_{OC}} = 50\text{m}\Omega \quad \text{for} \quad I_{OC} = 200\text{mA} \quad \& \quad V_{OS} = 100\mu V$$

2. Determine the desired gain (A_V) option for the INA based on the switching threshold of the comparator. When the load current (I_L) reaches the over-current threshold (I_{OC}), the INA output must cross the switching threshold (V_{TH}) of the comparator.

$$V_{TH} = (I_{OC} \times R_1) \times A_V = 0.2\text{V}$$

$$\text{Set} \quad A_V = \frac{V_{TH}}{I_{OC} \times R_1} = \frac{0.2}{0.2 \times 0.05} = 20\text{V/V} \quad \text{for} \quad R_1 = 50\text{m}\Omega$$

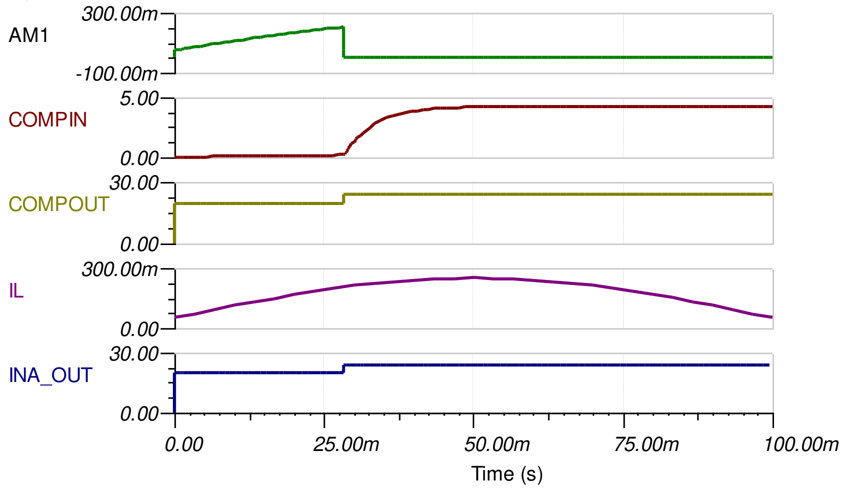
3. Since many INA's and comparators have 5 V operating voltage ranges, a 5 V supply voltage needs to be derived from the system supply V_S. In addition, the 5 V supply needs to float below V_S so the comparator output can drive the source-gate voltage of the P-channel MOSFET to 0 V when an over-current condition occurs and 5 V when the load current is less than I_{OC}. The method used in this circuit is a 5 V zener diode with a 10 kΩ bias resistor (R_2). Other options such as shunt regulators can also be utilized as long as proper bias current through the device is maintained.
4. A low pass filter is added between the INA output and the comparator input to attenuate any high frequency current spikes. It is more important to trigger the over-current latch with a delay than to falsely disconnect the system from the supply voltage. The low pass filter is derived from R_5 and C_1. Since the switching threshold of the comparator is 0.2 V, the delay is less than 1 time constant ($R_5 \times C_1$=5 ms).
5. A current limiting resistor R_4 is inserted between the comparator output and the gate of the P-channel MOSFET. Setting R_4 to 10 kΩ reduces current spikes on the supply when the comparator output needs to charge the MOSFET gate-source capacitance as a compromise to increasing the charge time. Inserting R_4 also serves the purpose of protecting the comparator output from any supply transients that can be present on the supply line.
6. The output of the comparator is directly connected to the REF pin of the INA in order to apply an offset to the INA's output voltage. When $I_L < I_{OC}$, the comparator output is low (equal to V_S-5 V) and no offset is added to the INA. However, when $I_L > I_{OC}$, the comparator output goes high (equal to V_S) and a 5 V offset is added to the INA. This offset causes the INA output to saturate at a level equal to V_S. Since an INA output level of V_S is higher than the V_{TH} of the comparator, the comparator output will remain high. This condition is referred to as a *latched* output state since the circuit will remain in this state until power to the circuit is cycled.



7. R_3 is added between the INA reference pin (REF) and GND (V_S-5 V) to ensure a proper ground path as the 5 V supply ramps up to the comparator minimum operating voltage.
8. If a latching feature is not preferred, the comparator output can be disconnected from the current sense amplifier reference pin and R_3 can be replaced with a short. In this configuration, the circuit will behave as a 200 mA current limiter.

Design Simulations

Transient Simulation Results



Design References

See Circuit SPICE Simulation File, SBVM944.

Design Featured Comparator

TLV4041R2	
V_S	1.6 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{OUT}	Push-Pull
Integrated Reference	200 mV ± 3 mV
I_Q	2 µA
t_{PD}	360 ns
TLV4041R2	

Design Featured Current Sense Amplifier

INA185	
V_S	2.7 V to 5.5 V
V_{inCM}	-0.2 V to 26 V
Gain Options	20 V/V, 50 V/V, 100 V/V, 200 V/V
Gain Error	0.2 %
V_{OS}	100 µV (A1), 25 µV (A2, A3, and A4)
I_Q	200 µA
INA185	

Low-side, bidirectional current sensing circuit

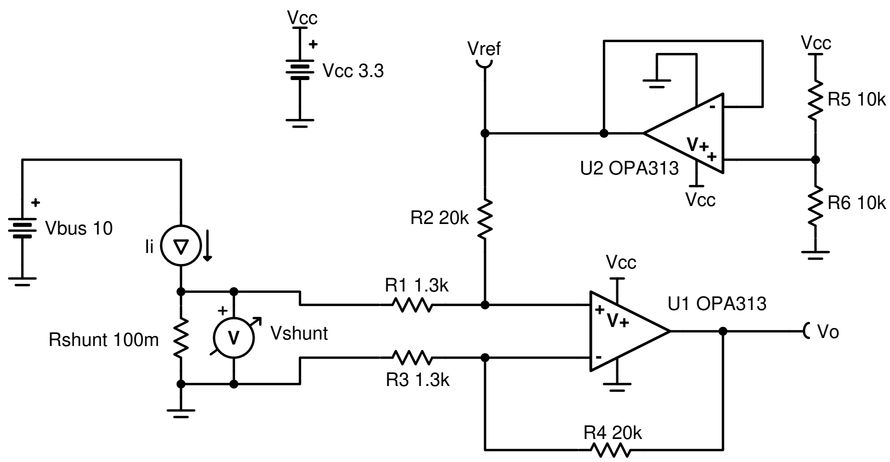
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–1A	1A	110mV	3.19V	3.3V	0V	1.65V

Design Description

This single-supply low-side, bidirectional current sensing solution can accurately detect load currents from –1A to 1A. The linear range of the output is from 110mV to 3.19V. Low-side current sensing keeps the common-mode voltage near ground, and is thus most useful in applications with large bus voltages.



Design Notes

1. To minimize errors, set $R_3 = R_1$ and $R_4 = R_2$.
2. Use precision resistors for higher accuracy.
3. Set output range based on linear output swing (see A_{ol} specification).
4. Low-side sensing should not be used in applications where the system load cannot withstand small ground disturbances or in applications that need to detect load shorts.

Design Steps

1. Determine the transfer equation given $R_4 = R_2$ and $R_1 = R_3$.

$$V_o = \left(I_i \times R_{shunt} \times \frac{R_4}{R_3}\right) + V_{ref}$$

$$V_{ref} = V_{cc} \times \left(\frac{R_6}{R_5 + R_6}\right)$$

2. Determine the maximum shunt resistance.

$$R_{shunt} = \frac{V_{shunt}}{I_{imax}} = \frac{100mV}{1\ \ A} = 100m\Omega$$

3. Set reference voltage.
   a. Since the input current range is symmetric, the reference should be set to mid supply. Therefore, make R_5 and R_6 equal.

$$R_5 = R_6 = 10k\Omega$$

4. Set the difference amplifier gain based on the op amp output swing. The op amp output can swing from 100mV to 3.2V, given a 3.3-V supply.

$$\text{Gain} = \frac{V_{oMax} - V_{oMin}}{R_{shunt} \times (I_{iMax} - I_{iMin})} = \frac{3.2\ V - 100mV}{100m\Omega \times (1\ \ A - (-1\ \ A))} = 15.5\ \frac{V}{V}$$

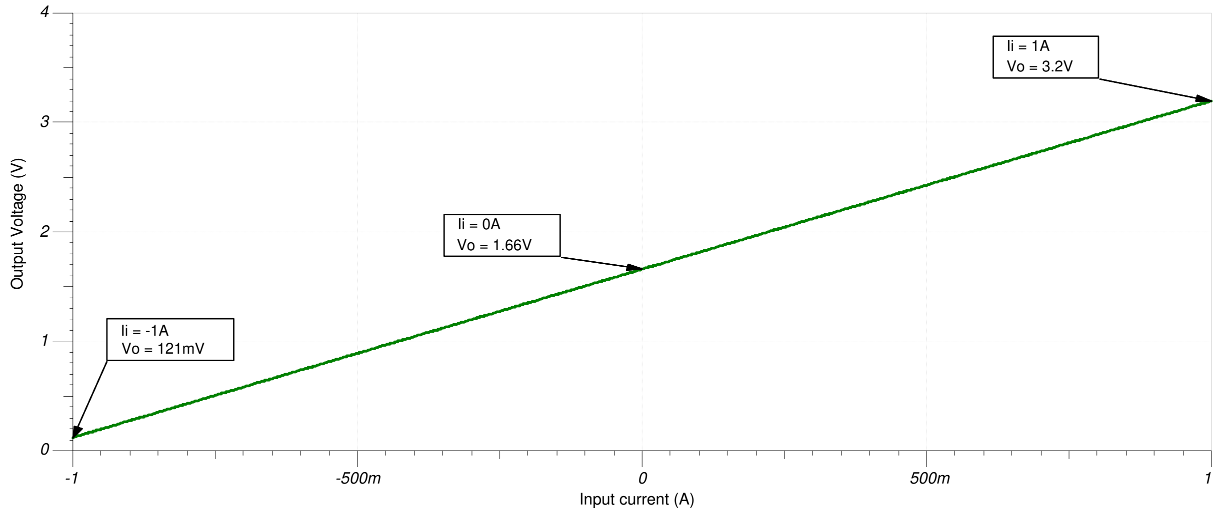
$$\text{Gain} = \frac{R_4}{R_3} = 15.5\ \frac{V}{V}$$

$$\text{Choose } R_1 = R_3 = 1.3k\Omega \text{ (Standard Value)}$$

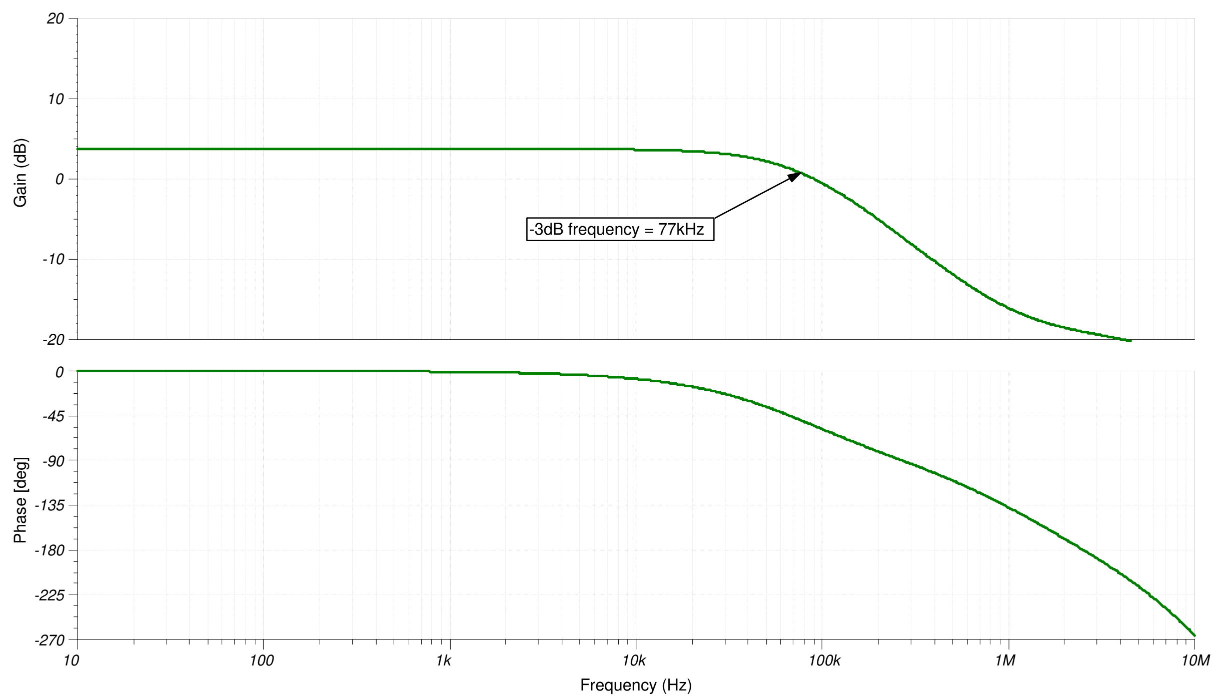
$$R_2 = R_4 = 15.5\frac{V}{V} \times 1.3k\Omega = 20.15\ k\Omega \approx 20k\Omega \text{ (Standard Value)}$$

Design Simulations

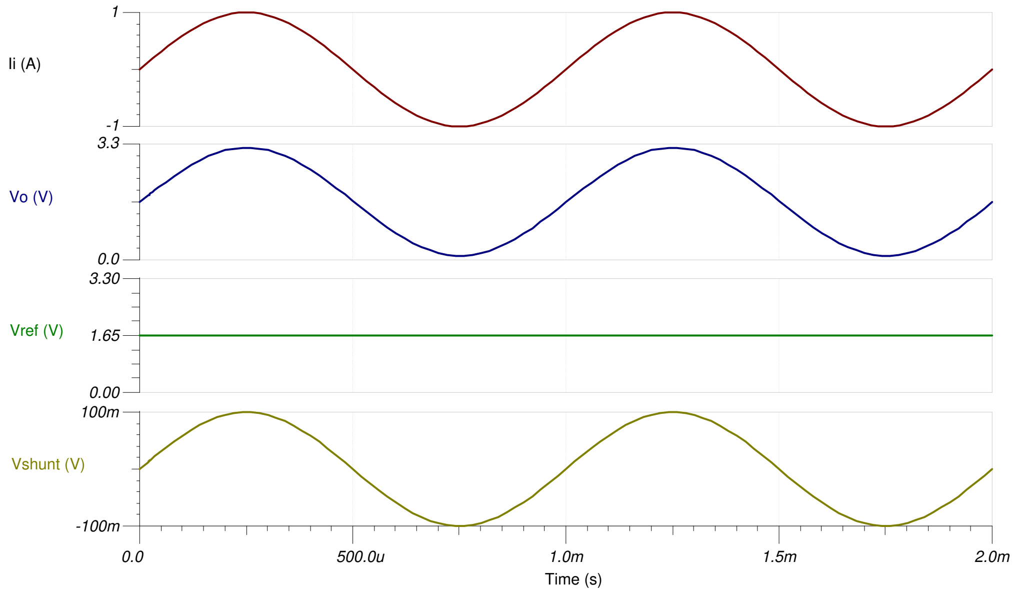
DC Simulation Results



Closed Loop AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC500.

See TIPD175, www.ti.com/tipd175.

Design Featured Op Amp

OPA313	
V_{cc}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	500µV
I_q	50µA/Ch
I_b	0.2pA
UGBW	1MHz
SR	0.5V/µs
#Channels	1, 2, 4
www.ti.com/product/opa313	

Design Alternate Op Amp

	TLV9062	OPA376
V_{cc}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	300µV	5µV
I_q	538µA/Ch	760µA/Ch
I_b	0.5pA	0.2pA
UGBW	10MHz	5.5MHz
SR	6.5V/µs	2V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/tlv9062	www.ti.com/product/opa376

For battery-operated or power-conscious designs, outside of the original design goals described earlier, where lowering total system power is desired.

LPV821	
V_{cc}	1.7V to 3.6V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1.5µV
I_q	650nA/Ch
I_b	7pA
UGBW	8KHz
SR	3.3V/ms
#Channels	1
www.ti.com/product/lpv821	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2018) to Revision B (January 2019) **Page**

- Cookbook landing page 1

Changes from Revision * (February 2018) to Revision A (May 2018) **Page**

- Changed title role to 'Amplifiers' 1
- Added SPICE simulation file link 1
- Added LPV821 as a *Design Alternate Op Amp* for battery-operated or power-conscious designs 1

Analog Engineer's Circuit

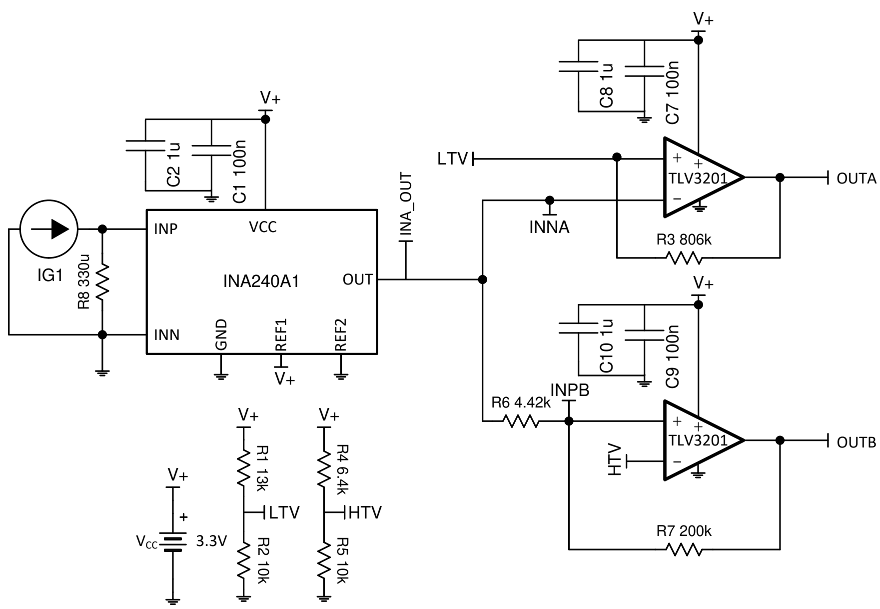
Bidirectional Current Sensing with a Window Comparator Circuit

Design Goals

SYSTEM CURRENT LEVELS				SUPPLY	
Falling OC Threshold	Falling OC Recovery	Rising OC Threshold	Rising OC Recovery	V+	V-
IG1 < -35 A	IG1 > -31 A	IG1 > 100 A	IG1 < 90 A	3.3 V	0 V

Design Description

This bidirectional current sensing solution uses a current-sense amplifier and a high speed dual comparator with a rail-to-rail input common mode range to create over-current (OC) alert signals at the comparator outputs (OUTA and OUTB) if the input current (IG1) rises above 100 A or falls below -35 A. In this implementation, both over-current alert signals are active high, so when the 100 A or -35 A thresholds are crossed, the comparator outputs will go high. External hysteresis is implemented on both comparators so that the comparator outputs will return to logic low states when the current reduces by 10% (90 A and -31 A). While the circuit below has shunt resistor R8 connected to ground, the same circuit is applicable for high side current sensing up to the common mode voltage range of the INA.



Design Notes

1. Select a comparator with rail-to-rail input common mode range.
2. Select a current sense amplifier with low offset voltage and a common mode input range that matches the requirements of the system.

Design Steps

1. To determine the comparator threshold voltages, first calculate the INA240A1 output voltages that correspond to the desired current thresholds. The calculations depend on the gain of the INA240 (20, 50, 100, 200 for A1, A2, A3, A4, respectively), the input current (IG1) and sense resistor (R8), and the reference voltage when the input current is 0 (VREF). Per section 8.3.2 in the INA240 data sheet, R8 is a function of the differential input voltage and the maximum input current to the INA240. Given that the input current in this system swings above 100 A, by keeping R8 small, the power dissipation across R8 will be lessened.

$$\mathrm{INA\_OUT} = \mathrm{VREF} + \mathrm{G} \times (\mathrm{INP} - \mathrm{INN})$$

$$\mathrm{INP} - \mathrm{INN} = \mathrm{IG1} \times \mathrm{R8}$$

$$\mathrm{VREF} = \frac{(\mathrm{V+}) - 0}{2} = \frac{3.3\mathrm{V}}{2} = 1.65\mathrm{V}$$

Using these equations and the desired current thresholds, the following table is generated:

DESCRIPTION		IG1	INA-OUT
$V_{H,\ CHB}$	Overcurrent threshold in forward direction	100 A	1.65 V + 20 x (100 A x 0.33 mΩ) = 2.31 V
$V_{L,\ CHB}$	*Recovery threshold* in forward direction	90 A	1.65 V + 20 x (90 A x 0.33 mΩ) = 2.244 V
$V_{H,\ CHA}$	Overcurrent threshold in reverse direction	-35 A	1.65 V + 20 x (-35 A x 0.33 mΩ) = 1.419 V
$V_{L,\ CHA}$	*Recovery threshold* in reverse direction	-31.5 A	1.65 V + 20 x (-31.5 A x 0.33 mΩ) = 1.4421 V

First, focus on the top comparator (channel A), which is in an inverting comparator configuration. This comparator will swing to a logic high when the current in the reverse direction exceeds -35 A, and will return to a logic low when the current in the reverse direction recovers to -31.5 A. These current levels correspond to voltage levels of 1.419 V and 1.4421 V, respectively.

2. Assume a value for R2 (the bottom resistor in the resistor divider). In this circuit, 10 kΩ is chosen.
3. Derive two equations for R1 in terms of V+, V_L, V_H, R_2, R_3 by analyzing the circuit when INNA = V_L and when INNA = V_H:

$$R_1 = \left(\frac{V_+}{V_L} - 1\right)\left(\frac{R_2R_3}{R_2 + R_3}\right)$$

$$R_1 = \frac{V_+ - V_H}{\frac{V_H}{R_2} - \frac{V_+ - V_H}{R_3}}$$

4. Set these two equations equal to each other and then solve for R_3.

$$\left(\frac{V_+ - V_H}{\frac{V_+}{V_L}} - V_H\right)R_3^{\,2} + \left(\frac{V_+ - V_H}{\frac{V_+}{V_L}} + V_+ - V_H\right)R_2R_3 = 0$$

$$\left(\frac{3.3 - 1.4421}{\frac{3.3}{1.419}} - 1.4421\right)R_3^{\,2} + \left(\frac{3.3 - 1.4421}{\frac{3.3}{1.419}} + 3.3 - 1.4421\right)(10k)R_3 = 0$$

$$R_3 = 0, \quad R_3 = 804.29\mathrm{k}\Omega$$

The standard 1% resistor value closest to this is 806 kΩ.

5. Solve for R_1 using any of the two equations derived in 3:

$$R_1 = \left(\frac{V_+}{V_L} - 1\right)\left(\frac{R_2 R_3}{R_2 + R_3}\right)$$

$$R_1 = \left(\frac{3.3}{1.419} - 1\right)\left(\frac{(10\ \ k\Omega)(806\ \ k\Omega)}{10\ \ k\Omega + 806\ \ k\Omega}\right)$$

$$R_1 = 13.093k\Omega$$

The standard 1% resistor value closest to this is 13 kΩ.

The next step is to focus on the bottom comparator (channel B), which is in a non-inverting configuration. This comparator will swing to a logic high when the current in the forward direction exceeds 100A, and will return to a logic low when the current in the forward direction recovers to 90A. These current levels correspond to voltage levels of 2.31 V and 2.244 V, respectively.

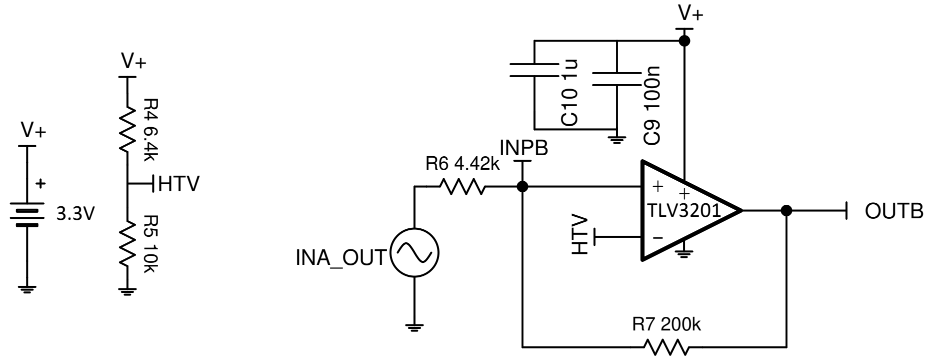


Figure 1-1.

SBOA306 (*High-side current sensing with comparator circuit*) derives two equations for V_{TH} (the voltage on the non-inverting pin) when the comparator output is in a logic low state and a high-impedance state (SBOA306 uses an open-drain comparator). These equations are then set equal to each other creating a quadratic equation to solve for R6. Since TLV3202 is a push-pull device, the output will go to a logic high state instead of a high-impedance state. Thus, the pull-up resistor value is 0 and V_{PU} is V_+

6. Rewrite the quadratic equation to match this circuit:

$$0 = V_+ \times {R_6}^2 + (V_+ \times R_7 + V_L \times (R_7) - V_H \times R_7) \times R_6 + (V_L - V_H) \times \left({R_7}^2\right)$$

$$0 = 3.3 \times {R_6}^2 + (3.3 \times R_7 + 2.244 \times (R_7) - 2.31 \times R_7) \times R_6 + (2.244 - 2.31) \times \left({R_7}^2\right)$$

7. Choose a value for R_7. This resistor dictates the load current of the comparator, and should thus be large. For this circuit, R_7 is assumed to be 200 kΩ.

$$0 = 3.3 \times {R_6}^2 + (3.3 \times 200k + 2.244 \times (200k) - 2.31 \times 200k) \times R_6 + (2.244 - 2.31) \times (200k)^2$$

$$R_6 = 4.47k\Omega$$

The standard 1% resistor value closest to this is 4.42kΩ.

8. Calculate V_{TH} using R_6.

$$V_{TH} = V_H \times \left(\frac{R_7}{R_6 + R_7}\right) = 2.31 \times \frac{200k}{4.42k + 200k} = 2.26V$$

9. Choose a value for R_5. In this case, R_5 is chosen to be 10 kΩ.

$$V_{TH} = V_H \times \left(\frac{R_2}{R_1 + R_2}\right) = 9.802V$$

10. Solve for R_4.

$$R_4 = \frac{R_5 \times (V_S - V_{TH})}{V_{TH}} = \frac{10k \times (3.3 - 2.6)}{2.26} = 4.602 \;\; k\Omega$$

The standard 1% resistor value closest to this is 4.64 kΩ.

Design Simulations

Transient Simulation Results

The below simulation results use a -70A to 130A, 100Hz sine wave for IG1.

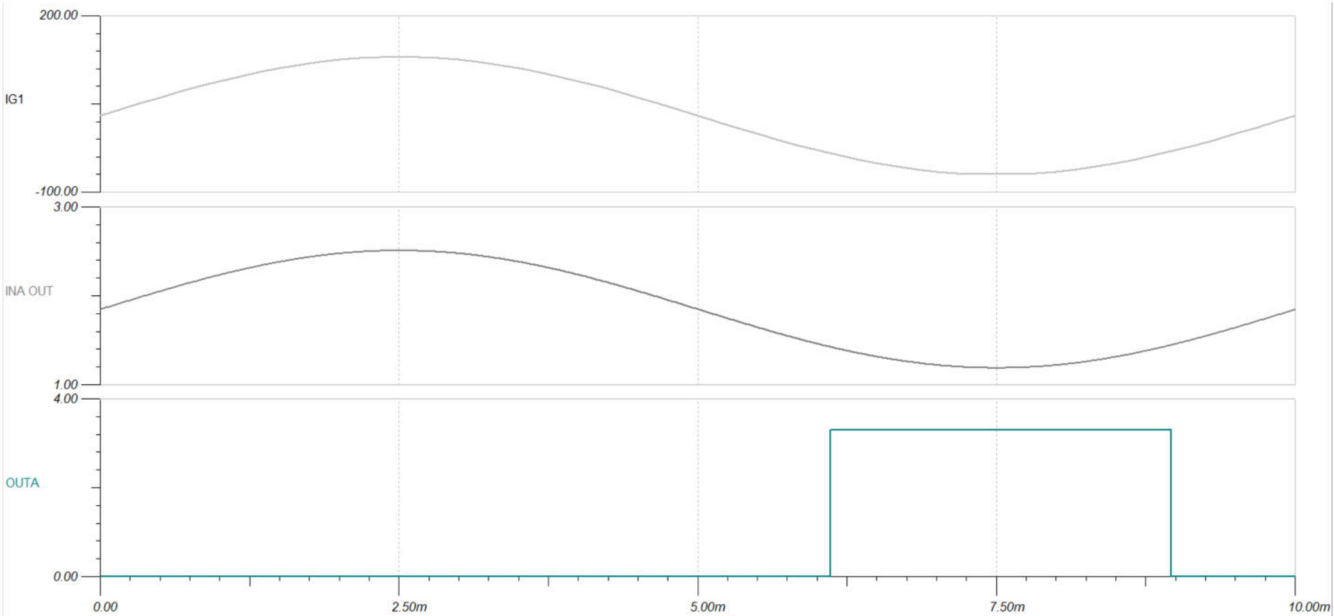


Figure 1-2. Channel A

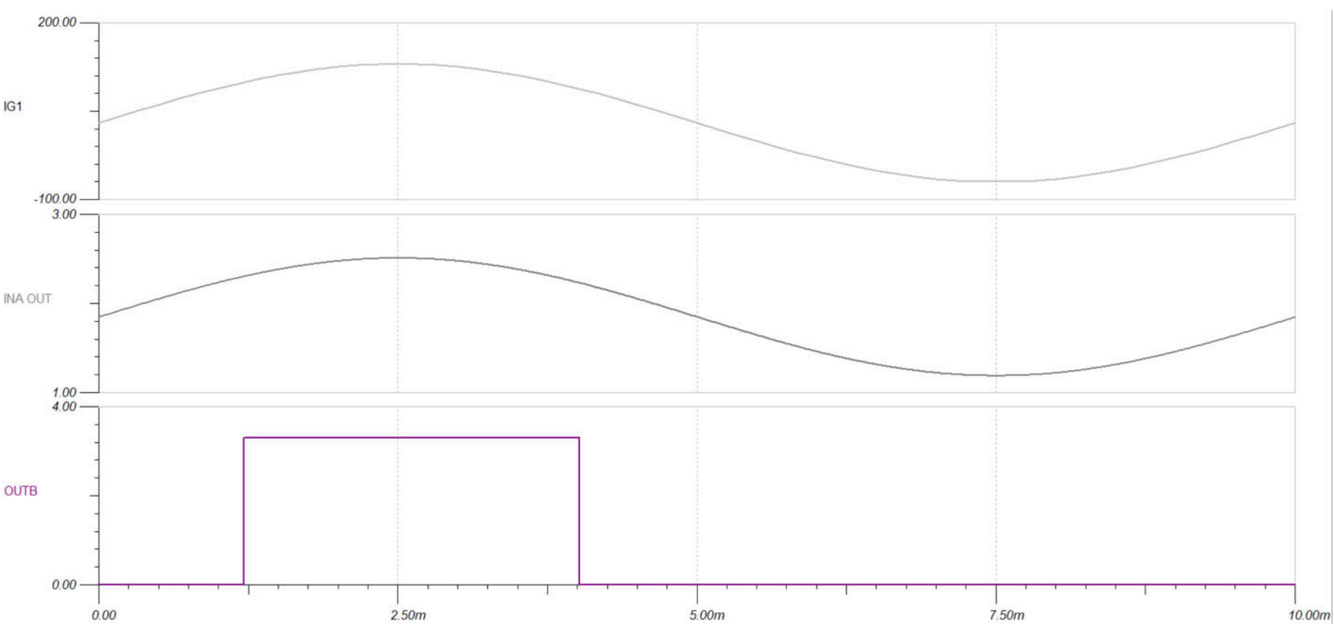


Figure 1-3. Channel B

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File SBOMB05.

Design Featured Comparator

TLV320x	
V_S	2.7 V to 5.5 V
V_{inCM}	200 mV beyond either rail
V_{OUT}	Push-Pull, Rail-to-rail
V_{OS}	1 mV
I_Q	40 µA/channel
$t_{PD(HL)}$	40 ns
#Channels	1, 2
TLV3201-Q1 and TLV3202-Q1	

Design Featured Op Amp

INA240	
V_S	1.6 V to 5.5 V
V_{inCM}	-4 V to 80 V
V_{OUT}	Rail-to-rail
V_{OS}	5 µV
V_{OS} Drift	50 nV/◦C
I_Q	260 ns
Gain Options	20 V/V, 50 V/V, 100 V/V, 200 V/V
INA240	

Analog Engineer's Circuit

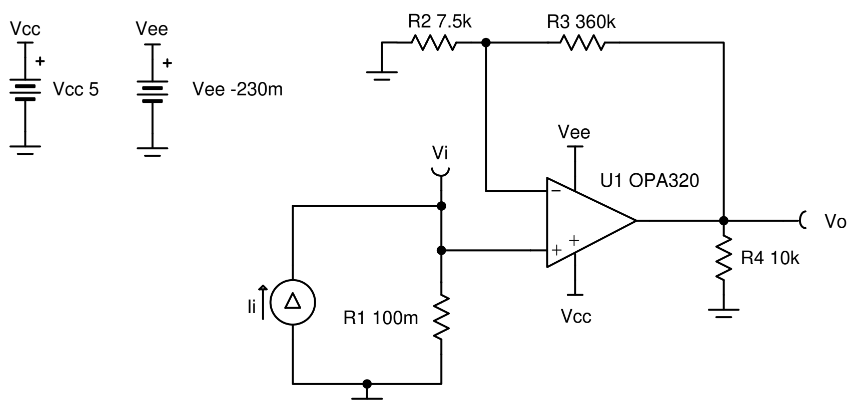
Single-Supply, Low-Side, Unidirectional Current-Sensing Solution With Output Swing to GND Circuit

Design Goals

Input		Output		Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
0 A	1 A	0 V	4.9 V	5 V	0 V	0 V

Design Description

This single-supply, low-side, current sensing solution accurately detects load current between 0 A to 1 A and converts it to a voltage between 0 V to 4.9 V. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings. A negative charge pump (such as the LM7705) is used as the negative supply in this design to maintain linearity for output signals near 0 V.



Design Notes

1. Use precision resistors to minimize gain error.
2. For light load accuracy, the negative supply should extend slightly below ground.
3. A capacitor placed in parallel with the feedback resistor will limit bandwidth and help reduce noise.

Design Steps

1. Determine the transfer function.

$$V_o = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

2. Define the full-scale shunt voltage and shunt resistance.

$$V_{\text{iMax}} = 100\text{mV at} \quad I_{\text{iMax}} = 1A$$

$$R_1 = \frac{V_{\text{iMax}}}{I_{\text{iMax}}} = \frac{100\text{mV}}{1 \quad A} = 100\text{m}\Omega$$

3. Select gain resistors to set the output range.

$$V_{\text{iMax}} = 100\text{mV} \quad \text{and } V_{\text{oMax}} = 4.9V$$

$$\text{Gain} = \frac{V_{\text{oMax}}}{V_{\text{iMax}}} = \frac{4.9V}{100\text{mV}} = 49\frac{V}{V}$$

$$\text{Gain} = 1 + \frac{R_3}{R_2} = 49\frac{V}{V}$$

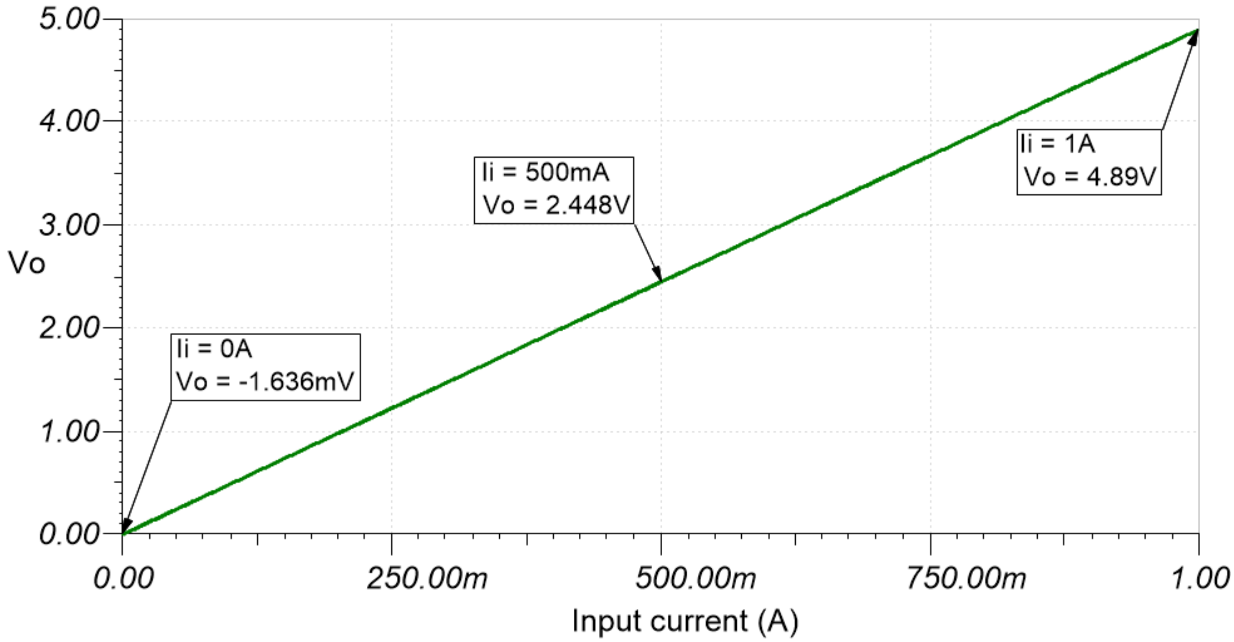
4. Select a standard value for R_2 and R_3.

$$R_2 = 7.5\text{k}\Omega \text{ (0.05\% Standard Value)}$$

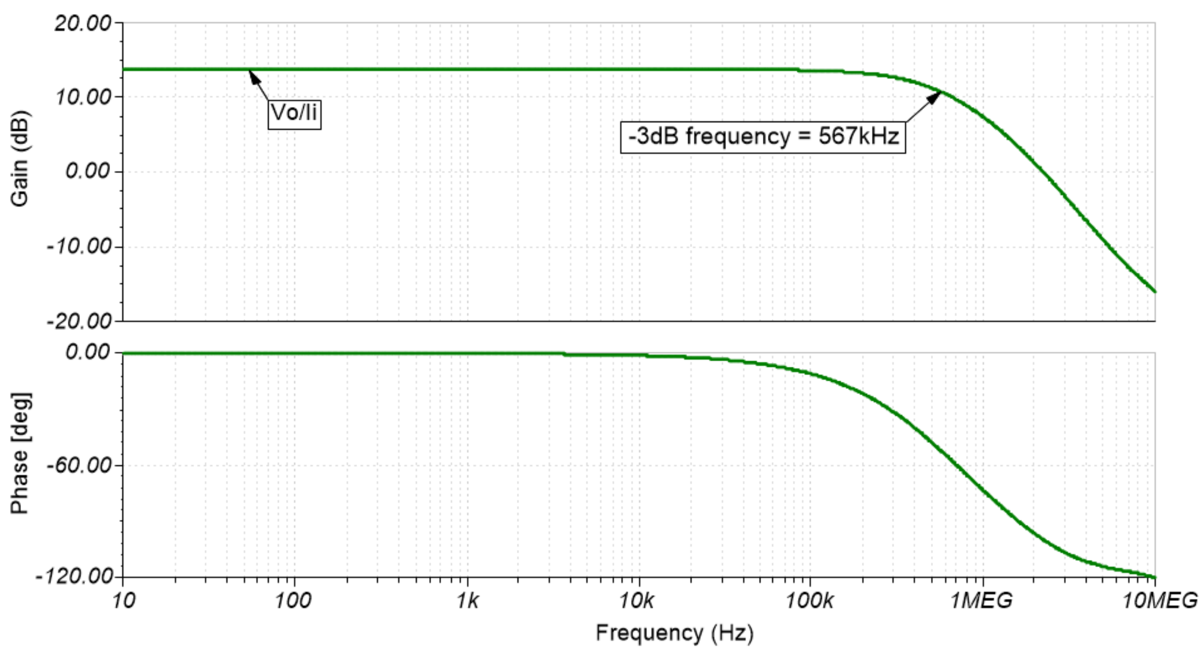
$$R_3 = 48 \times R_2 = 360\text{k}\Omega \text{ (0.05\% Standard Value)}$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC499.

See TIPD129.

Design Featured Op Amp

OPA320	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40 µV
I_q	1.5 mA/Ch
I_b	0.2 pA
UGBW	10 MHz
SR	10 V/µs
#Channels	1 and 2
OPA320	

Design Alternate Op Amp

TLV9002	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	400 µV
I_q	60 µA
I_b	5 pA
UGBW	1 MHz
SR	2 V/µs
#Channels	1, 2, and 4
TLV9002	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019 **Page**

- Downscale the title and changed title role to *Amplifiers*. Added link to circuit cookbook landing page.............. 1

Analog Engineer's Circuit

High-Side, Bidirectional Current-Sensing Circuit with Transient Protection

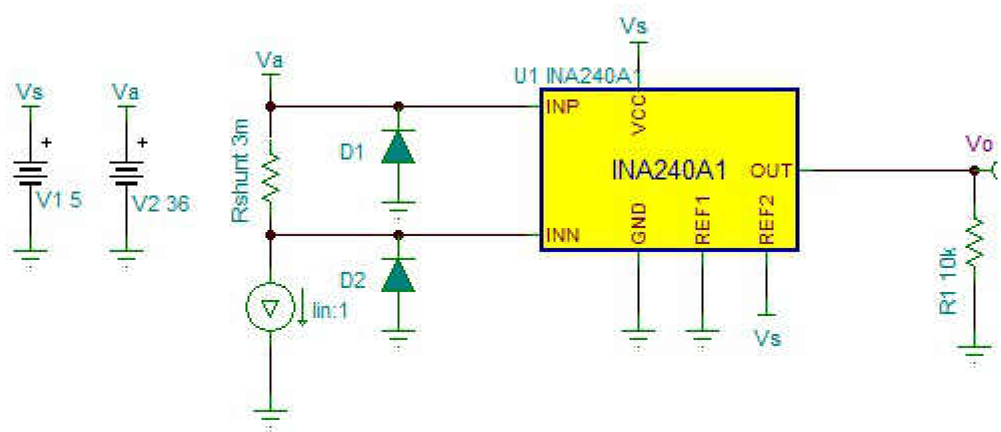
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply			Standoff and Clamp Voltages		EFT Level
I_{inMin}	I_{inMax}	V_{oMin}	V_{oMax}	Vs	GND	V_{ref}	Vwm	Vc	Vpp
–40 A	40 A	100 mV	4.9 V	5 V	0 V	2.5 V	36 V	80 V	2 kV 8/20 µs

Design Description

This high-side, bidirectional current sensing solution can accurately measure current in the range of –40 A to 40 A for a 36 V voltage bus. The linear voltage output is 100 mV to 4.90 V. This solution is also designed to survive IEC61000-4-4 level 4 EFT stress (Voc = 2 kV; Isc = 40 A; 8/20 µs).



Design Notes

1. This solution is targeted toward high-side current sensing.
2. The sense resistor value is determined by minimum and maximum load currents, power dissipation and Current Shunt Amplifier (CSA) gain.
3. Bidirectional current sensing requires an output reference voltage (Vref). Device gain is achieved through internal precision matched resistor network.
4. The expected maximum and minimum output voltage must be within the device linear range.
5. The TVS diode must be selected based on bus voltage, the CSA common-mode voltage specification, and EFT pulse characteristics.

Design Steps

1. Determine the maximum output swing:

$$\mathrm{VswN} = Vref - VoMin = 2.5\mathrm{V} - 0.1\mathrm{V} = 2.4\mathrm{V}$$

$$\mathrm{VswP} = VoMax - Vref = 4.9\mathrm{V} - 2.5\mathrm{V} = 2.4\mathrm{V}$$

2. Determine the maximum value of the sense resistor based on maximum load current, swing and device gain. In this example, a gain of 20 was chosen to illustrate the calculation, alternative gain versions may be selected as well:

$$\mathrm{Rshunt} \le \frac{\mathrm{Vswp}}{\mathrm{Iin\_max} \times \mathrm{Gain}} = \frac{2.4\mathrm{V}}{40\mathrm{A} \times 20} = 3\mathrm{m}\ \Omega$$

3. Calculate the peak power rating of the sense resistor:

$$\mathrm{Pshunt} = \mathrm{Iin\_max}^2 \times \mathrm{Rshunt} = 40\mathrm{A}^2 \times 3\mathrm{m}\ \Omega\ = 5\mathrm{W}$$

4. Determine TVS standoff voltage and clamp voltage:

$$\mathrm{Vwm} = 36\mathrm{V} \quad \text{and} \quad \mathrm{Vc} \le 80\mathrm{V}$$

5. Select a TVS diode.

   For example, SMBJ36A from Littelfuse™ satisfies the previous requirement, with peak pulse power of 600 W (10/1000 μs) and current of 10.4 A.
6. Make sure the TVS diode satisfies the design requirement based on the TVS operating curve.

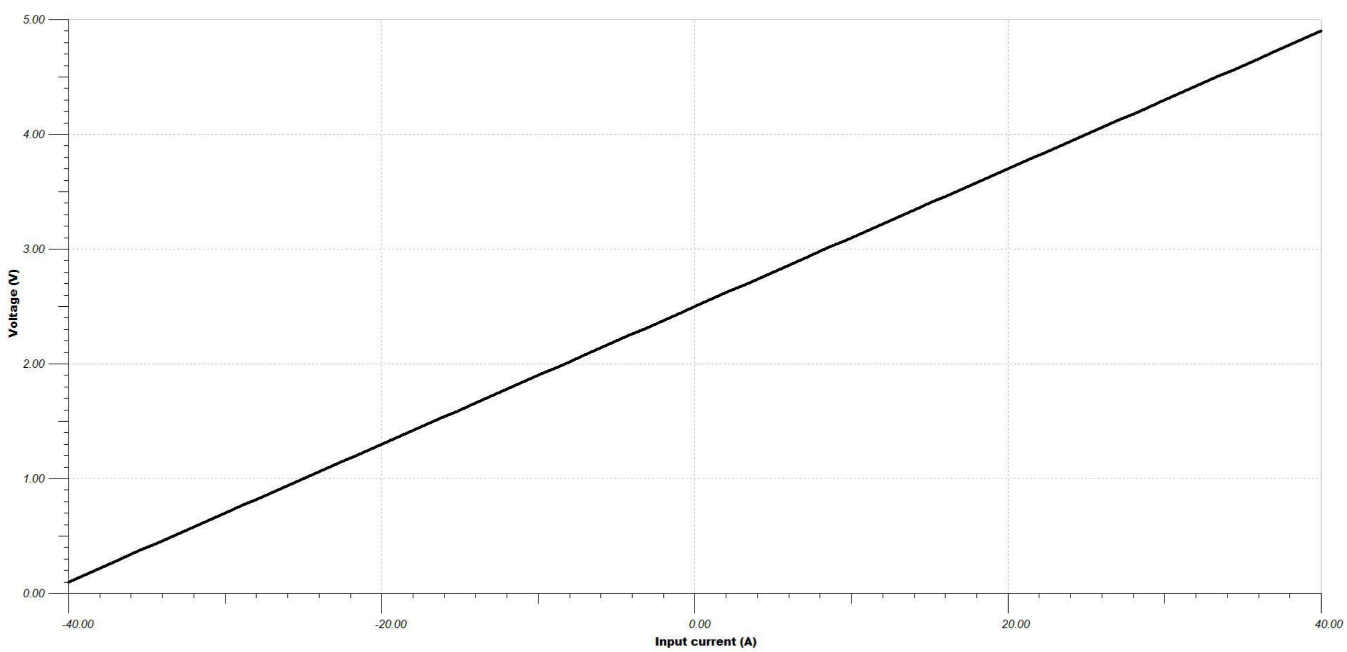
   Peak pulse power at given excitation (8/20 μs) is estimated to be around 3.5 kW, which translates to peak pulse current:

$$\mathrm{Ipp} = \frac{3.5\mathrm{kW}}{600\mathrm{W}} \times 10.4\mathrm{A} = 60\mathrm{A}$$

This is above the maximum excitation (short circuit) current of 40 A. The select TVS effectively protects the circuit against the specified EFT strike.

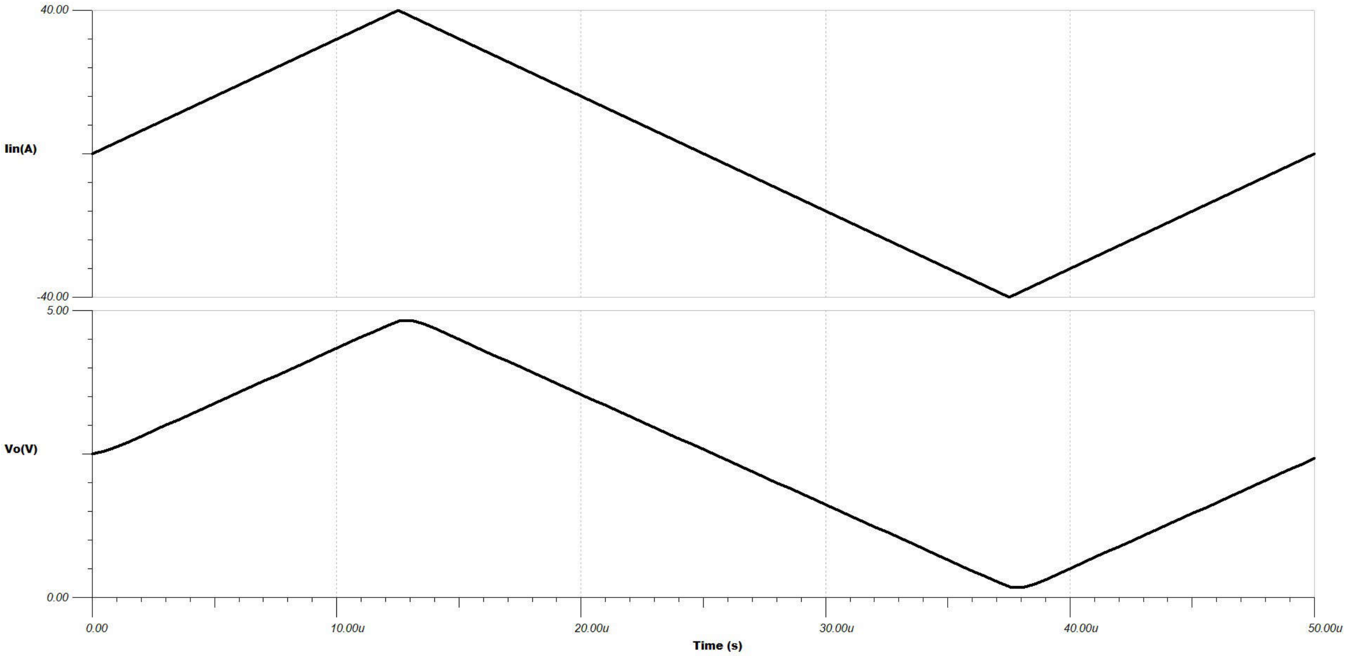
Design Simulations

DC Transfer Characteristics

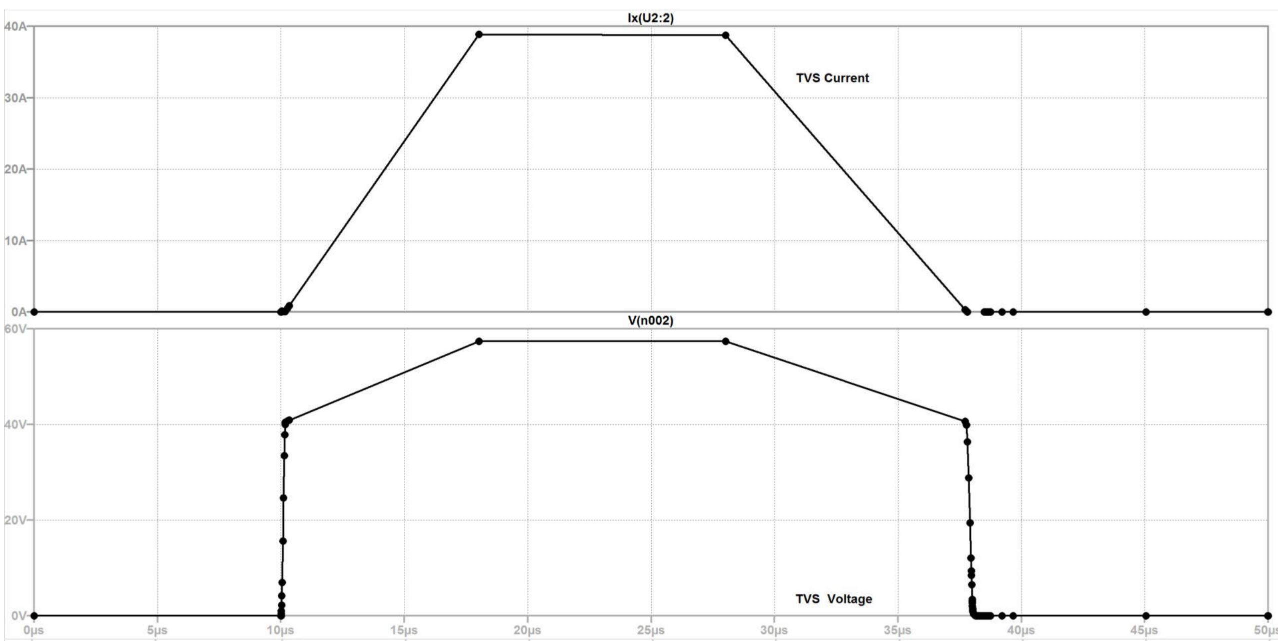


Transient Simulation Results

The output is a scaled version of the input.



TVS Diode Transient Response Under EFT Excitation



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

For more information on transient protection of the current sense amplifiers, see *TIDA-00302* and the *Current Sense Amplifier Training Videos*.

Design Featured Current Sense Amplifier

INA240A1	
V_s	2.7 V to 5.5 V
V_{CM}	–4 V to 80 V
V_{os}	Rail-to-rail
V_{os}	5 µV
I_B	80 µA
BW	400 kHz
Vos Drift	50 nV/°C
INA240A1	

Design Alternate

INA282	
V_s	2.7 V to 18 V
V_{CM}	–14 V to 80 V
V_{os}	20 µV
I_B	25 µA
BW	10 kHz
Vos Drift	0.3 µV/°C
INA282	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from May 15, 2018 to February 19, 2019 **Page**

- Changed VinMin and VinMax in the *Design Goals* table to IinMin and IinMax, respectively............................. 1

3-Decade, Load-Current Sensing Circuit

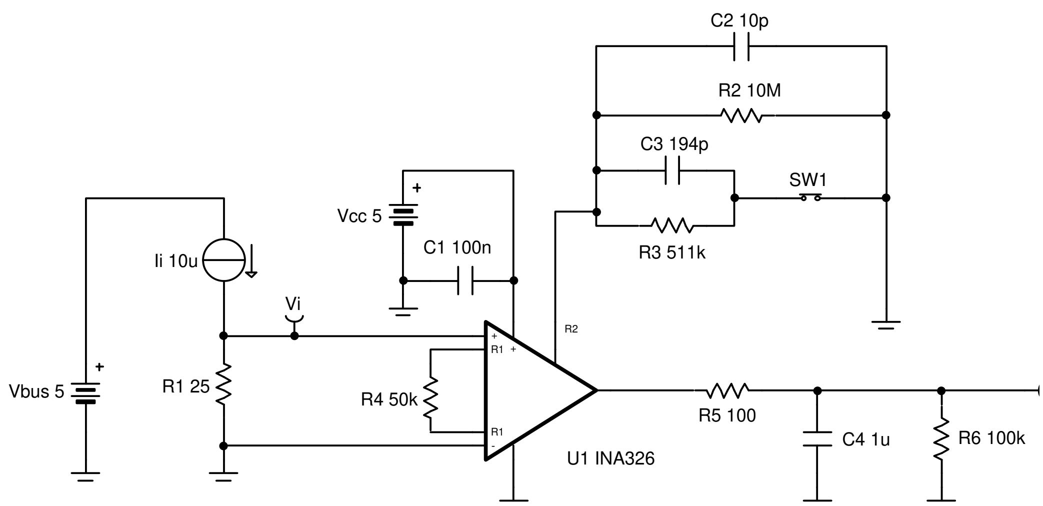
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
10 µA	10 mA	100 mV	4.9 V	5.0 V	0 V	0 V

Design Description

This single-supply, low-side, current-sensing solution accurately detects load current between 10 µA and 10 mA. A unique yet simple gain switching network was implemented to accurately measure the three-decade load current range.



Design Notes

1. Use a maximum shunt resistance to minimize relative error at minimum load current.
2. Select 0.1% tolerance resistors for R_1, R_2, R_3, and R_4 in order to achieve approximately 0.1% FSR gain error.
3. Use a switch with low on-resistance (R_{on}) to minimize interaction with feedback resistances, preserving gain accuracy.
4. Minimize capacitance on INA326 gain setting pins.
5. Scale the linear output swing based on the gain error specification.

Design Steps

1. Define full-scale shunt resistance.

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250mV}{10mA} = 25\Omega$$

2. Select gain resistors to set output range.

$$G_{IiMax} = \frac{V_{oMax}}{V_{iMax}} = \frac{V_{oMax}}{R_1 \times I_{iMax}} = \frac{4.9V}{25\Omega \times 10mA} = 19.6\frac{V}{V}$$

$$G_{IiMin} = \frac{V_{oMin}}{V_{iMin}} = \frac{V_{oMin}}{R_1 \times I_{iMin}} = \frac{100mV}{25\Omega \times 10\mu A} = 400\frac{V}{V}$$

$$R_2 = \frac{R_4 \times G_{IiMin}}{2} = \frac{50k\Omega \times 400\frac{V}{V}}{2} = 10M\Omega$$

$$R_2 \parallel R_3 = \frac{R_4 \times G_{IiMax}}{2} = \frac{50k\Omega \times 19.6\frac{V}{V}}{2} = 490k\Omega$$

$$R_3 = \frac{490k\Omega \times R_2}{R_2 - 490k\Omega} = 515.25k\Omega \approx 511k\Omega \text{ (Standard Value)}$$

3. Select a capacitor for the output filter.

$$f_p = \frac{1}{2 \times \pi \times R_5 \times C_4} = \frac{1}{2 \times \pi \times 100\Omega \times 1\ \ \mu F} = 1.59kHz$$

4. Select a capacitor for gain and filtering network.

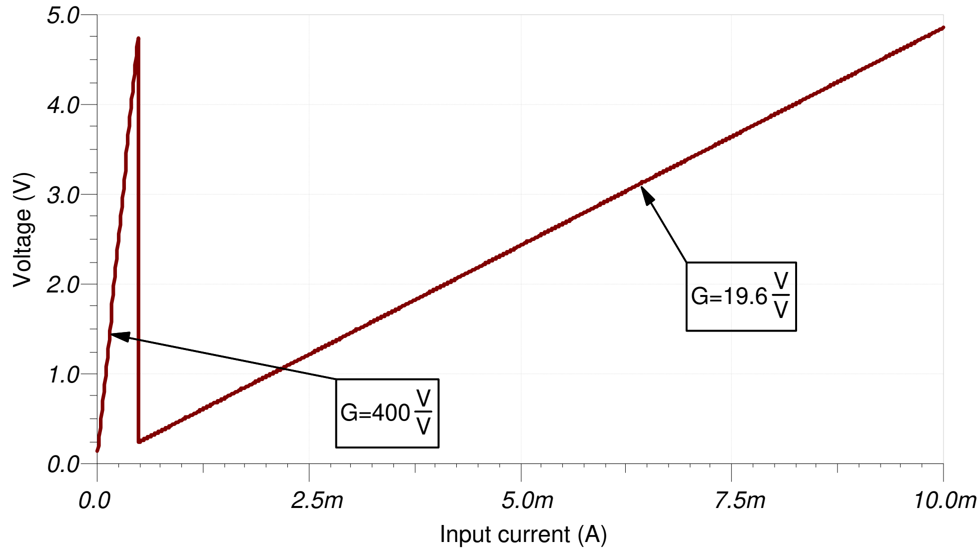
$$C_2 = \frac{1}{2 \times \pi \times R_2 \times f_p} = \frac{1}{2 \times \pi \times 10M\Omega \times 1.59kHz} = 10pF$$

$$C_3 = \frac{1}{2 \times \pi \times (R_2||R_3) \times f_p} - C_2 = \frac{1}{2 \times \pi \times (10M\Omega||511k\Omega) \times 1.59kHz} - 10pF$$

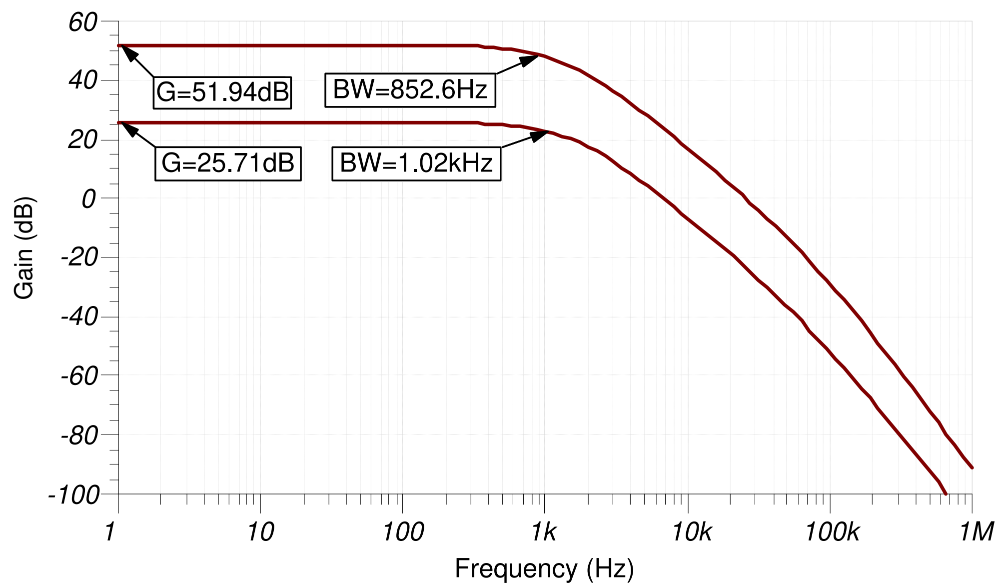
$$C_3 = 196pF \approx 194pF \text{ (Standard Value)}$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC498.

See TIPD104, Current Sensing Solution, 10 µA-10 mA, Low-Side, Single Supply.

Design Featured Op Amp

INA326	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.1 mV
I_q	3.4 mA
I_b	2 nA
UGBW	1 kHz
SR	Filter limited
#Channels	1
INA326	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 28, 2018 to February 1, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.............1

PWM Generator Circuit

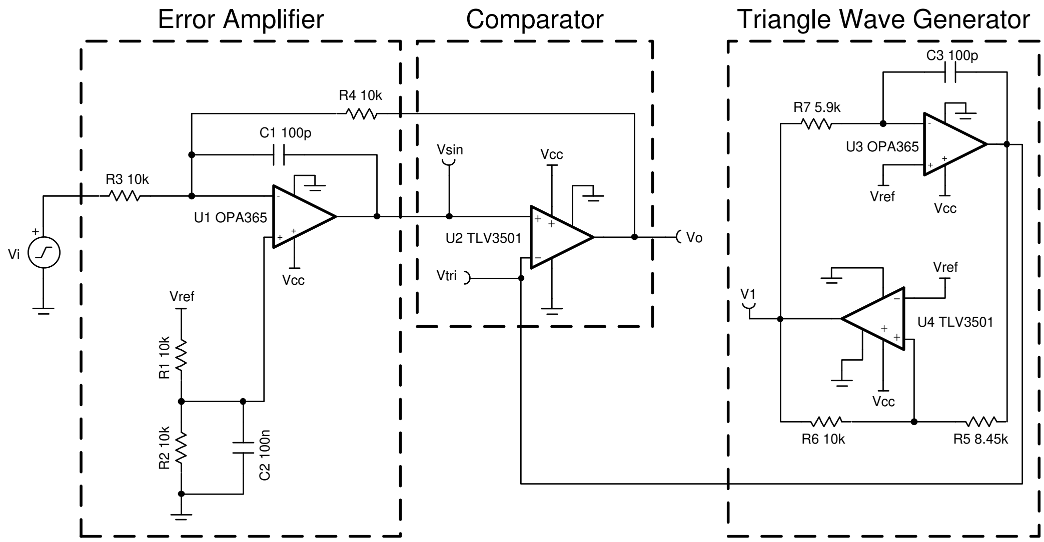
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–2.0 V	2.0 V	0 V	5 V	5 V	0 V	2.5 V

Design Description

This circuit utilizes a triangle wave generator and comparator to generate a 500 kHz pulse-width-modulated (PWM) waveform with a duty cycle that is inversely proportional to the input voltage. An op amp and comparator (U_3 and U_4) generate a triangle waveform which is applied to the inverting input of a second comparator (U_2). The input voltage is applied to the non-inverting input of U_2. By comparing the input waveform to the triangle wave, a PWM waveform is produced. U_2 is placed in the feedback loop of an error amplifier (U_1) to improve the accuracy and linearity of the output waveform.



Design Notes

1. Use a comparator with push-pull output and minimal propagation delay.
2. Use an op amp with sufficient slew rate, GBW, and voltage output swing.
3. Place the pole created by C_1 below the switching frequency and well above the audio range.
4. V_{ref} must be low impedance (for example, output of an op amp).

Design Steps

1. Set the error amplifier inverting signal gain.

$$\mathrm{Gain} = -\frac{R_4}{R_3} = -1\frac{V}{V}$$

$$\mathrm{Select}\ R_3 = R_4 = 10\mathrm{k\Omega}$$

2. Determine R_1 and R_2 to divide V_{ref} to cancel the non-inverting gain.

$$V_{o\_dc} = \left(1 + \frac{R_4}{R_3}\right)\left(\frac{R_2}{R_1 + R_2}\right) \times \mathrm{Vref}$$

$$R_1 = R_2 = R_3 = R_4 = 10\mathrm{k\Omega},\ V_{o\_dc} = 2.5\mathrm{V}$$

3. The amplitude of V_{tri} must be chosen such that it is greater than the maximum amplitude of V_i (2.0 V) to avoid 0% or 100% duty cycle in the PWM output signal. Select V_{tri} to be 2.1 V. The amplitude of V_1 = 2.5 V.

$$V_{tri}\ (\mathrm{Amplitude}) = \frac{R_5}{R_6} \times V_1\left(\mathrm{Amplitude}\right)$$

$$\mathrm{Select}\ R_6\ \mathrm{to\ be}\ 10\mathrm{k\Omega},\quad \mathrm{then\ compute}\ R_5$$

$$R_5 = \frac{V_{tri}(\mathrm{Amplitude}) \times R_6}{V_1\ \ (\mathrm{Amplitude})} = 8.4\mathrm{k\Omega} \approx 8.45\mathrm{k\Omega}\ (\mathrm{Standard\ Value})$$

4. Set the oscillation frequency to 500 kHz.

$$f_t = \frac{R_6}{4 \times R_7 \times R_5 \times C_3}$$

$$\mathrm{Set}\ C_3 = 100\mathrm{pF},\ \mathrm{then\ compute}\ R_7$$

$$R_7 = \frac{R_6}{4 \times f_t \times R_5 \times C_3} = 5.92\mathrm{k\Omega} \approx 5.90\mathrm{k\Omega}\ (\mathrm{Standard\ Value})$$

5. Choose C_1 to limit amplifier bandwidth to below switching frequency.

$$f_p = \frac{1}{2 \times \pi \times R_4 \times C_1}$$

$$C_1 = 100\mathrm{pF} \rightarrow f_p = 159\mathrm{kHz}$$

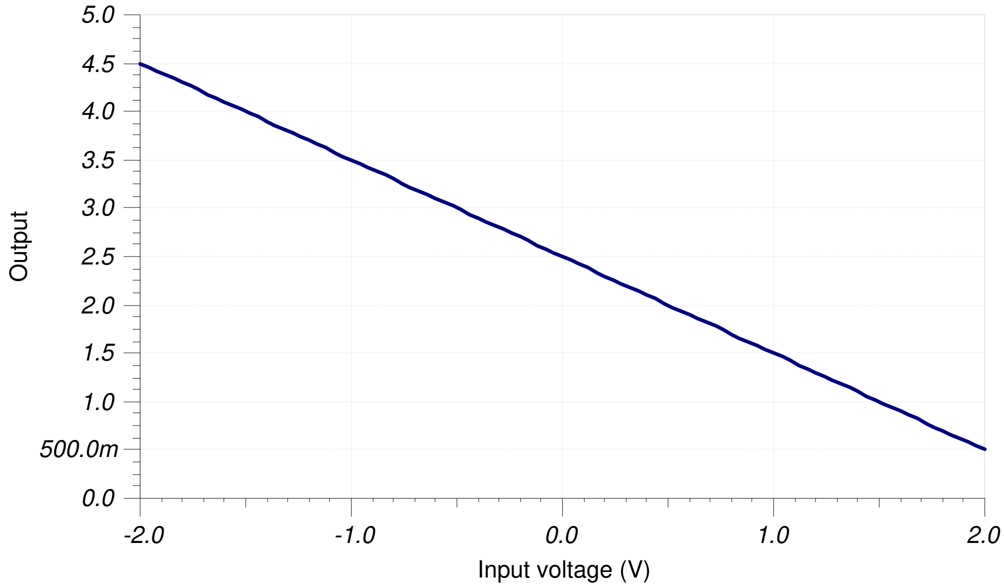
6. Select C_2 to filter noise from V_{ref}.

$$C_2 = 100\mathrm{nF}\ (\mathrm{Standard\ Value})$$

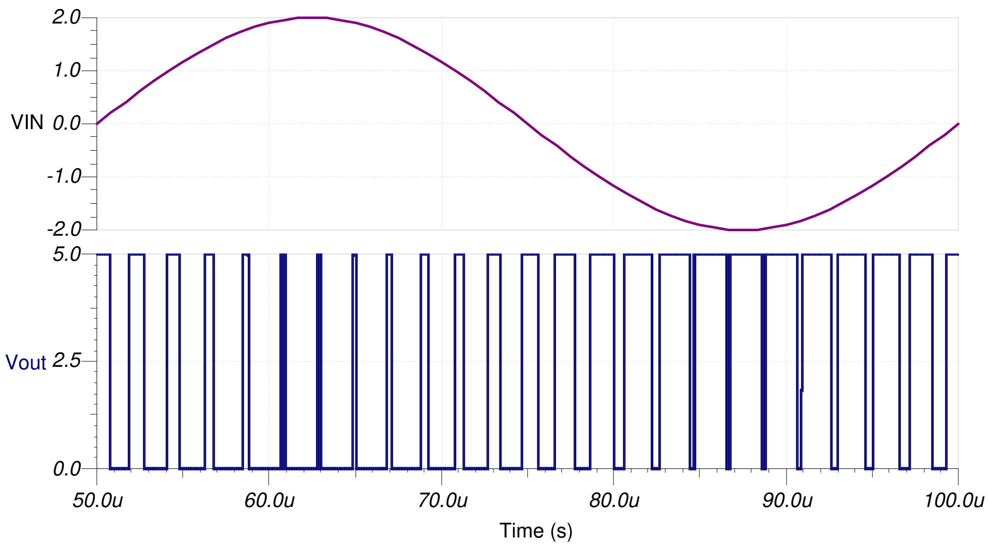
$$f_{div} = \frac{1}{2 \times \pi \times C_2 \times \frac{R_1 \times R_2}{R_1 + R_2}} = 320\mathrm{Hz}$$

Design Simulations

DC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC502.

See TIPD108, Analog PWM Generator 5V, 500 kHz PWM Output

Design Featured Op Amp

OPA2365	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	100 µV
I_q	4.6 mA
I_b	2 pA
UGBW	50 MHz
SR	25 V/µs
#Channels	2
OPA2365	

Design Comparator

TLV3502	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	3.2 mA
I_b	2 pA
UGBW	—
SR	—
#Channels	2
TLV3502	

Design Alternate Op Amp

OPA2353	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	3 mV
I_q	5.2 mA
I_b	0.5 pA
UGBW	44 MHz
SR	22 V/µs
#Channels	2
OPA2352	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from January 19, 2018 to February 1, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.............	1

Sine wave generator circuit

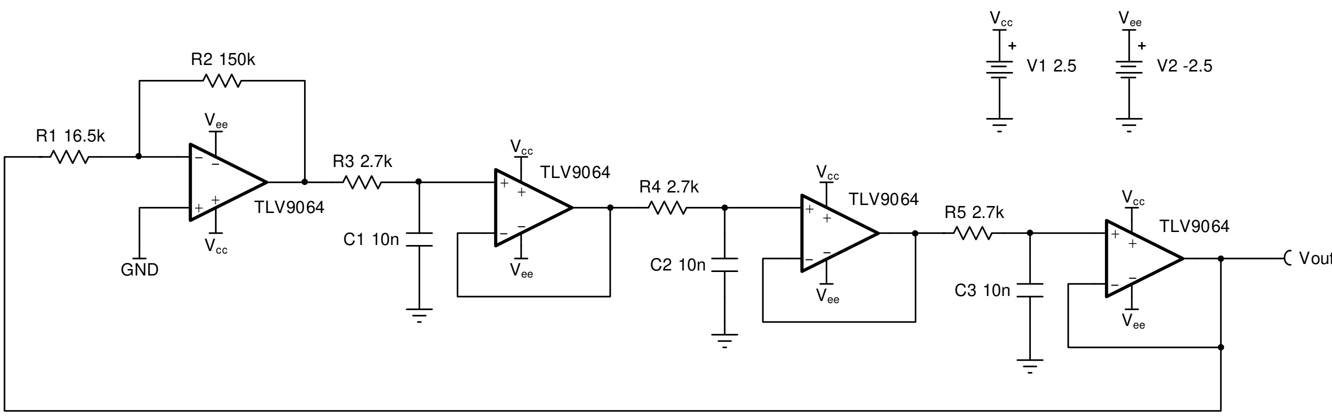
Amplifiers

Design Goals

AC Specifications		Supply	
AC Gain	$f_{oscillation}$	V_{cc}	V_{ee}
8V/V	10kHz	2.5V	–2.5V

Design Description

This circuit uses a quad channel op amp with ±2.5-V supplies to generate a 10kHz, low-distortion sine wave. The amplifiers buffer each RC filter stage, which yields a low-distortion output.



Design Notes

1. Using excessively large feedback resistors, R_1 and R_2, can lead to a shift in oscillation frequency, and an increase in noise and distortion.
2. The first stage resistors, R_1 and R_2, must be selected to provide a sufficiently large gain. Otherwise, oscillations at the output will dampen. However, an excessively large gain at the first stage will lead to higher output distortion and a decreased frequency of oscillation.
3. Heavy loading of the output leads to degradation in the oscillation frequency.
4. At higher frequencies (> 10 kHz), the phase delay of the amplifier becomes significant. The result will be a frequency of oscillation that is lower than calculated or expected. Thus, some margin must be included when selecting values for the loading elements of the first, second, and third stages (R_3, R_4, R_5, C_1, C_2, and C_3) for higher-frequency designs to ensure the desired oscillation frequency is achieved.
5. Choose an amplifier with at least 100 times the required gain bandwidth product. This will ensure the actual and calculated oscillation frequencies match.
6. For more precise control of the oscillation frequency, use passive components with lower tolerances.

Design Steps

For a classical feedback system, oscillation occurs when the product of the open loop gain, A_{OL}, and the feedback factor, β, is equal to –1, or 1 at 180°. Therefore, each RC stage in the design must contribute 60° of phase shift. Since each stage is isolated by a buffer, the feedback factor, β, of the first stage must have a magnitude of $(1/2)^3$. Therefore the gain (1/β) must be at least 8V/V.

1. $$A_{OL} \times \beta = A_{OL} \times \left(\frac{1}{RCs + 1}\right)^3$$

   Select the first stage feedback resistors for the gain necessary to maintain oscillation.

   $$\text{Gain} = \frac{R_2}{R_1} \geq 8\frac{V}{V}$$

   $$R_1 = 16.5k\Omega,\ \ R_2 = 150k\Omega\ (\text{Standard Values})$$

2. Calculate components R_3, R_4, R_5, C_1, C_2, and C_3 to set the oscillation frequency. Select C_1, C_2, and C_3 as 10nF.

   $$f_{oscillation} = \frac{\tan(60°)}{2\pi \times R \times C} = 10\text{kHz}$$

   $$C_{1,2,3} = 10\text{nF (Standard Values)}$$

   $$R_{3,4,5} = \frac{\tan(60°)}{2\pi \times C \times f_{oscillation}} = \frac{1.73}{2\pi \times 10\text{nF} \times 10\text{kHz}} = 2757\Omega \approx 2.7\text{k}\Omega\ (\text{Standard Values})$$

3. Ensure the selected op amp has the bandwidth to oscillate at the desired frequency.

   $$f_{oscillation} \ll \frac{GBW}{Gain} = \frac{GBW}{\left(\frac{R_2}{R_1}\right) + 1}$$

   $$10\text{kHz} \ll \frac{10\text{MHz}}{\left(\frac{150\text{k}\Omega}{16.5\text{k}\Omega}\right) + 1} \cong 991\text{kHz}$$

4. Ensure the selected op amp has the slew rate necessary to oscillate at the desired frequency. Use the full power bandwidth equation to calculate the necessary slew rate and ensure it is less than the slew rate of the amplifier. While the exact amplitude of oscillation is difficult to predict, you can ensure that our amplifier is fast enough to generate the needed sine wave by ensuring that the output can swing from rail-to-rail.

   $$SR_{req} = V_{peak} \times 2\pi\, f_{oscillation} = 2.5V \times 2\pi \times 10\text{kHz} = 0.157\frac{V}{\mu s},\ \text{given}\ \ V_{cc} = V_{peak}$$

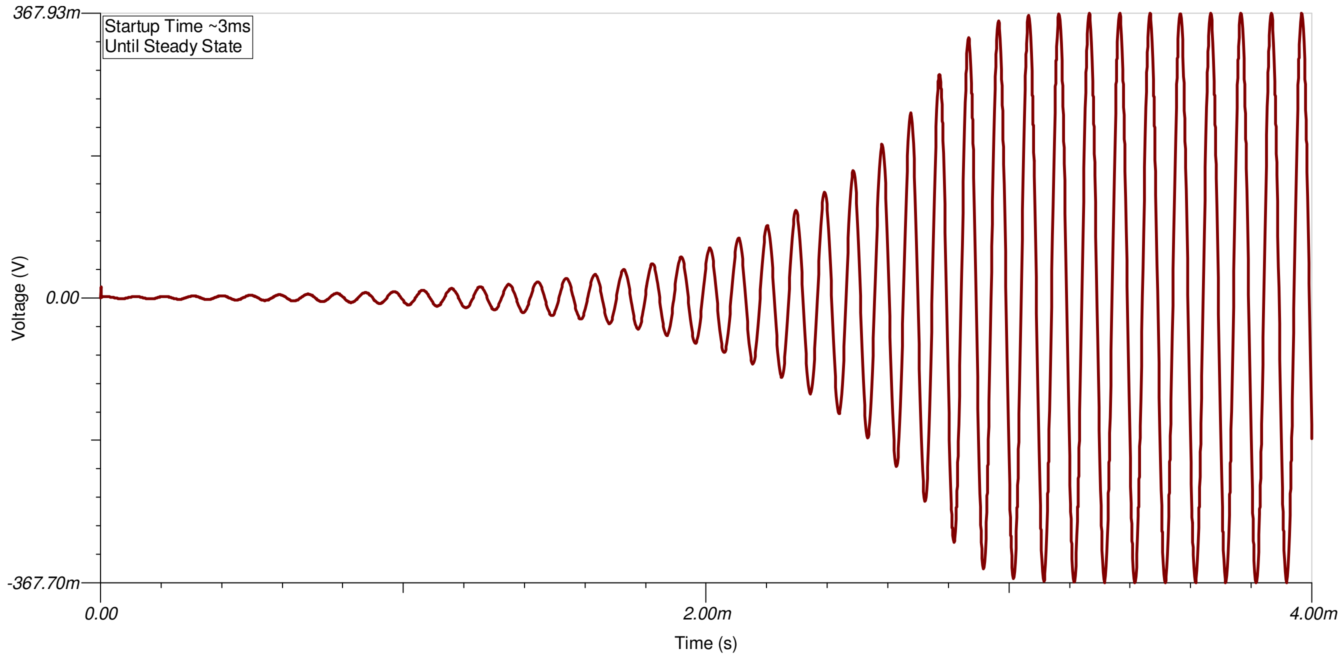
   $$SR_{req} < SR_{TLV9064}$$

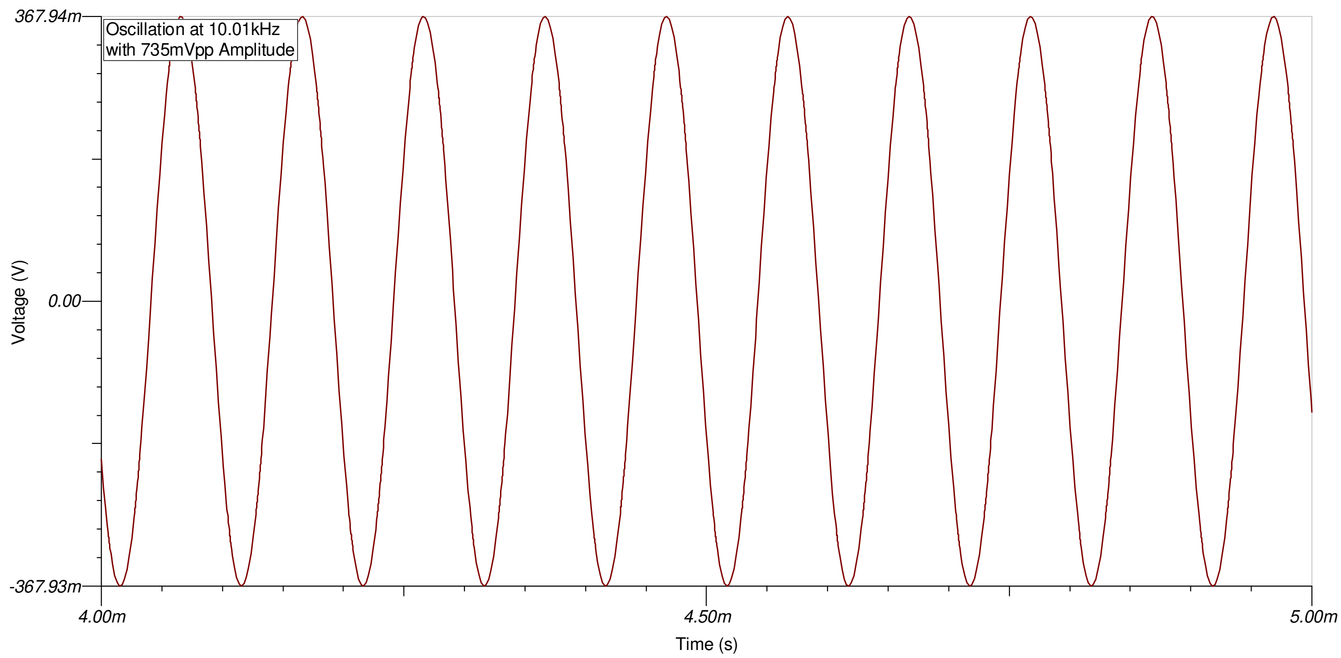
   $$0.157\ \frac{V}{\mu s} < 6.5\frac{V}{\mu s}$$

Design Simulations

The resulting simulations demonstrate a sinusoidal oscillator that reaches steady state after about 3ms to a 10.01-kHz sine wave with a 735-mV_{pp} amplitude.

Transient Simulation Results





Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation File: SLOC355.
3. TI Precision Labs
4. *Sine-Wave Oscillator Application Report*
5. *Design of Op Amp Sine Wave Generators Application Report*

Design Featured Op Amp

TLV9064	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	300µV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9064	

Design Alternate Op Amps

	TLV9052	OPA4325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail–to–rail	Rail–to–rail
V_{out}	Rail–to–rail	Rail–to–rail
V_{os}	330µV	40µV
I_q	330µA	650µA
I_b	2pA	0.2pA
UGBW	5MHz	10MHz
SR	15V/µs	5V/µs
#Channels	2	4
	www.ti.com/product/TLV9052	www.ti.com/product/OPA4325

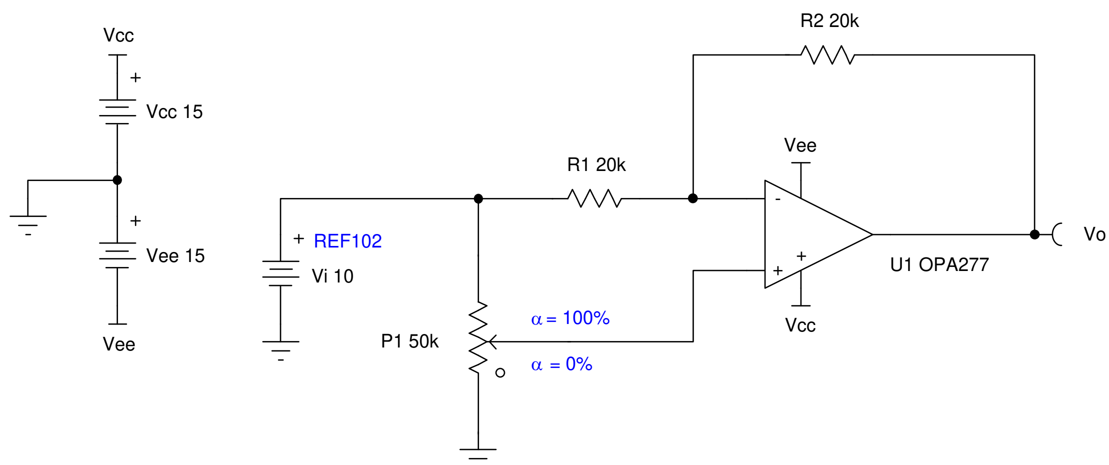
Adjustable Reference Voltage Circuit

Design Goals

Input	Output		Supply	
V_i	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
10 V	–10 V	10 V	15 V	–15 V

Design Description

This circuit combines an inverting and non-inverting amplifier to make a reference voltage adjustable from the negative of the input voltage up to the input voltage. Gain can be added to increase the maximum negative reference level.

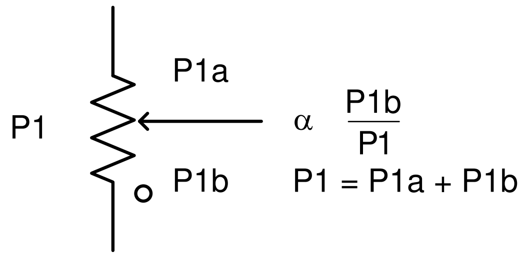


Design Notes

1. Observe the common-mode and output swing limitations of the op amp.
2. Mismatch in R_1 and R_2 results in a gain error. Selecting $R_2 > R_1$ increases the maximum negative voltage, and selecting $R_2 < R_1$ decreases the maximum negative voltage. In either case, the maximum positive voltage is always equal to the input voltage. This relationship is inverted if a negative input reference voltage is used.
3. Select the potentiometer based on the desired resolution of the reference. Generally, the potentiometers can be set accurately to within one-eighth of a turn. For a 10-turn pot this means alpha (∝) may be off by as much as 1.25%.

Design Steps

Alpha represents the potentiometer setting relative to ground. This is the fraction of the input voltage that will be applied to the non-inverting terminal of the op amp and amplified by the non-inverting gain.



The transfer function of this circuit follows:

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1} + \alpha\left(1 + \frac{R_2}{R_1}\right)$$

1. If $R_2 = R_1 = 20\ k\Omega$, then the equation for V_o simplifies as the following shows:

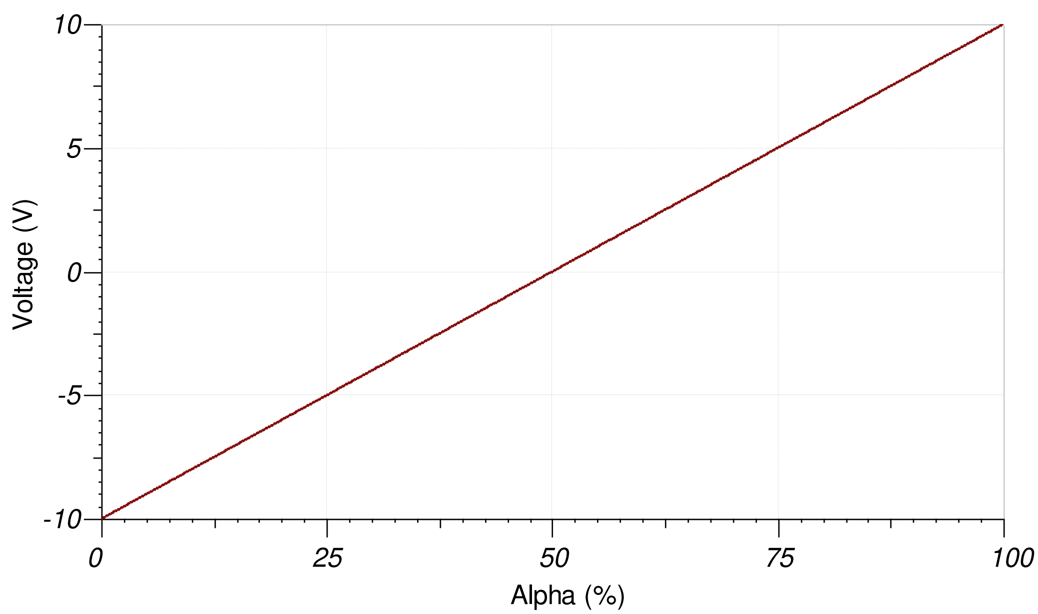
$$V_o = (2\alpha - 1) \times V_i$$

2. If V_i = 10V and ∝ = 0.75, the value of V_o can be determined.

$$V_o = (2 \times 0.75 - 1) \times 10 = 5V$$

Design Simulations

DC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the TINA-TI™ circuit simulation file, SBOMAU2.

See TI Precision Labs - Op Amps.

Design Featured Op Amp

OPA277	
V_{ss}	4 V to 36 V
V_{inCM}	V_{ee}+2 V to V_{cc}–2 V
V_{out}	V_{ee}+0.5 V to V_{cc}–1.2 V
V_{os}	10 µV
I_q	790 µA/Ch
I_b	500 pA
UGBW	1 MHz
SR	0.8 V/µs
#Channels	1, 2, and 4
OPA277	

Design Alternate Op Amp

OPA172	
V_{ss}	4.5 V to 36 V
V_{inCM}	V_{ee}–0.1 V to V_{cc}–2 V
V_{out}	Rail-to-rail
V_{os}	200 µV
I_q	1.6 mA/Ch
I_b	8 pA
UGBW	10 MHz
SR	10 V/µs
#Channels	1, 2, and 4
OPA172	

Voltage-to-current (V-I) converter circuit with BJT

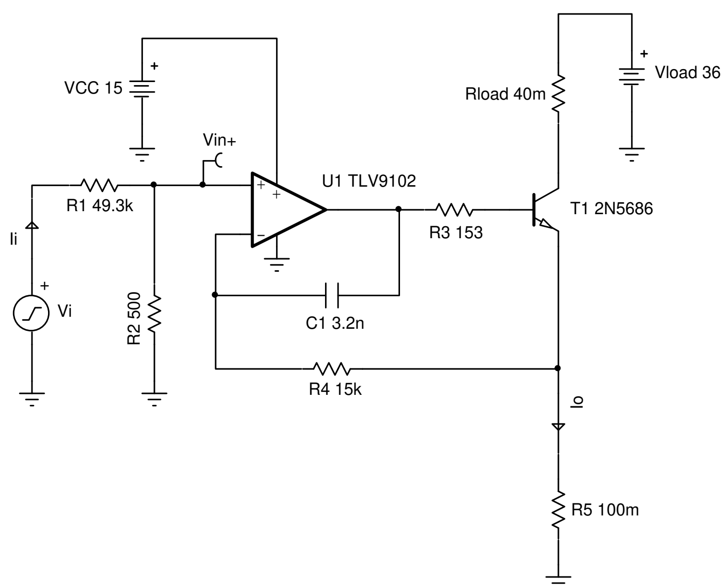
Amplifiers

Design Goals

Input			Output		Supply		
V_{iMin}	V_{iMax}	I_{iMax}	I_{oMin}	I_{oMax}	V_{cc}	V_{ee}	V_{load}
0V	10V	200µA	0A	1A	15V	0V	36V

Design Description

This low-side voltage-to-current (V-I) converter delivers a well-regulated current to a load which can be connected to a voltage greater than the op amp supply voltage. The circuit accepts an input voltage from 0V to 10V and converts it to a current from 0A and 1A. The current is accurately regulated by feeding back the voltage drop across a low-side current-sense resistor (R_5) to the op amp.



Design Notes

1. Resistor divider (R1 and R2) is implemented to limit the maximum voltage at the non-inverting input, V_{in+}, and sense resistor, R_5, at full-scale.
2. For an op amp that is not rail-to-rail input (RRI), a voltage divider may be needed to reduce the input voltage to be within the common-mode voltage of the op amp.
3. Use low resistance values for R_5 to maximize load compliance voltage and reduce the power dissipated at full-scale.
4. Using a high-gain BJT reduces the output current requirement for the op amp.
5. Feedback components R_3, R_4, and C_1 provide compensation to ensure stability. R_3 isolates the input capacitance of the bipolar junction transistor (BJT), R_4 provides a DC feedback path directly at the current-setting resistor (R_5), and C_1 provides a high-frequency feedback path that bypasses the BJT.
6. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions in the device data sheet.

Design Steps

The transfer function of the circuit is:

$$Io = \frac{R_2}{R_5 \times (R_1 + R_2)} \times Vi$$

1. Calculate the sense resistor, R_5. The sense resistor should be sized as small as possible to maximize the load compliance voltage and reduce power dissipation. Set the maximum voltage across the sense resistor to 100mV. Limiting the voltage drop to 100mV limits the power dissipated in the sense resistor to 100mW at full-scale output.

   $$\text{Let } V_{in\text{-}(max)} = 100\text{mV at } I_{oMax} = 1\text{A}$$

   $$R_5 = \frac{V_{in\text{-}(max)}}{I_{oMax}} = \frac{100\text{mV}}{1\text{A}} = 100\text{m}\Omega$$

2. Select resistors, R_1 and R_2, for the voltage divider at the input. At the maximum input voltage, the voltage divider should reduce the input voltage to the op amp, $V_{in+(max)}$, to the maximum voltage across the sense resistor, R_5. R_1 and R_2 should be chosen such that the maximum input current is not exceeded.

   $$V_{in\text{-}(max)} = V_{in+(max)} = I_{iMax} \times R_2 = 100\text{mV}$$

   $$R_2 = \frac{V_{in+(max)}}{I_{iMax}} = \frac{100\text{mV}}{200\mu\text{A}} = 500\Omega \sim 499\Omega \text{ (Standard value)}$$

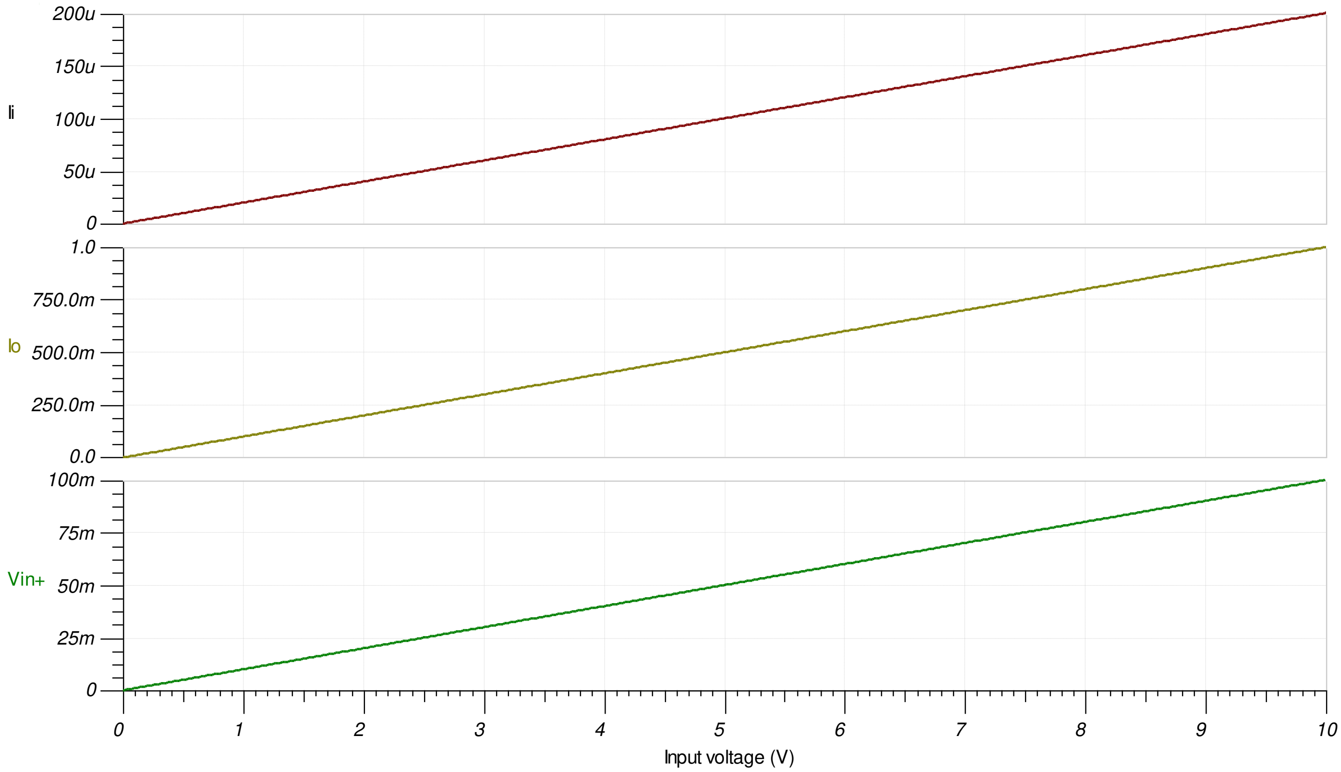
   $$V_{in+(max)} = V_{iMax} \times \left(\frac{R_2}{R_1 + R_2}\right)$$

   $$R_1 = 49.5\text{k}\Omega \sim 49.3\text{k}\Omega \text{ (Standard value)}$$

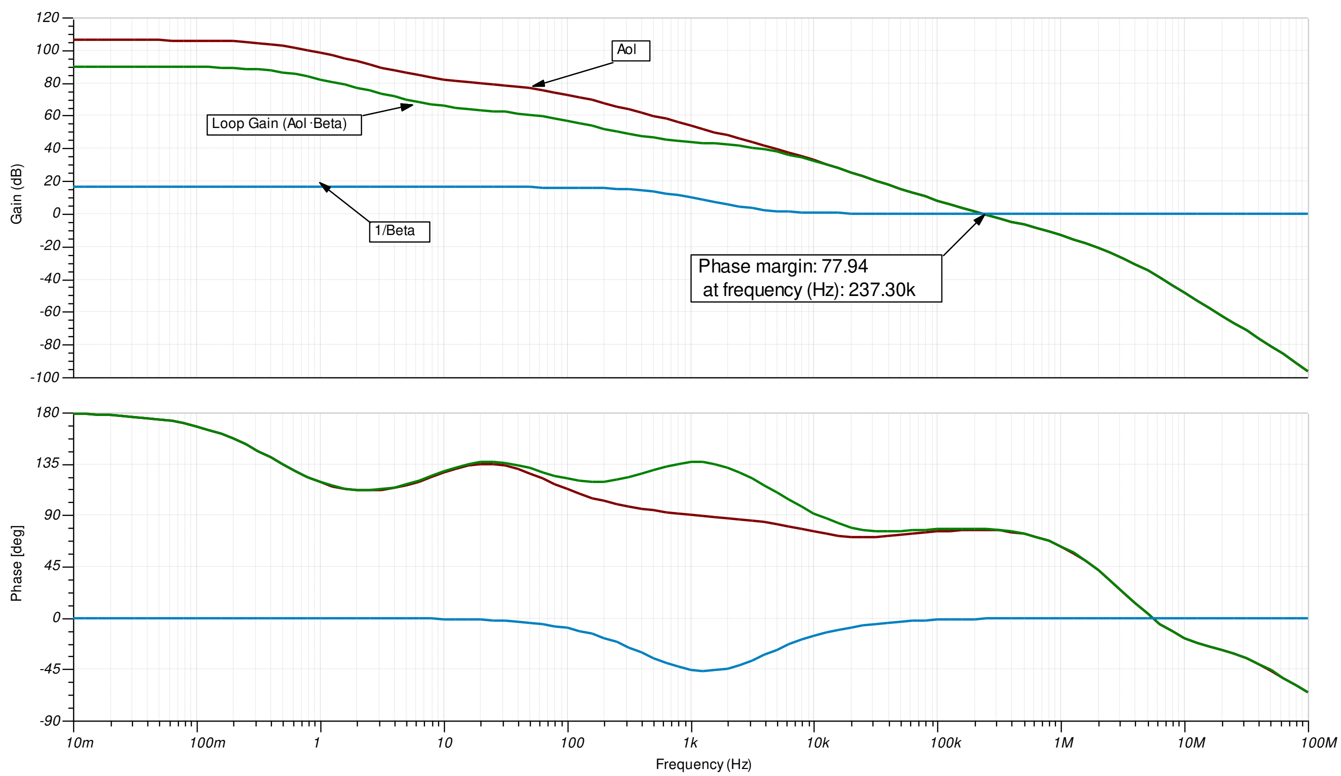
3. See the Design References section [3] for the design procedure on how to properly size the compensation components, R_3, R_4, and C_1.

Design Simulations

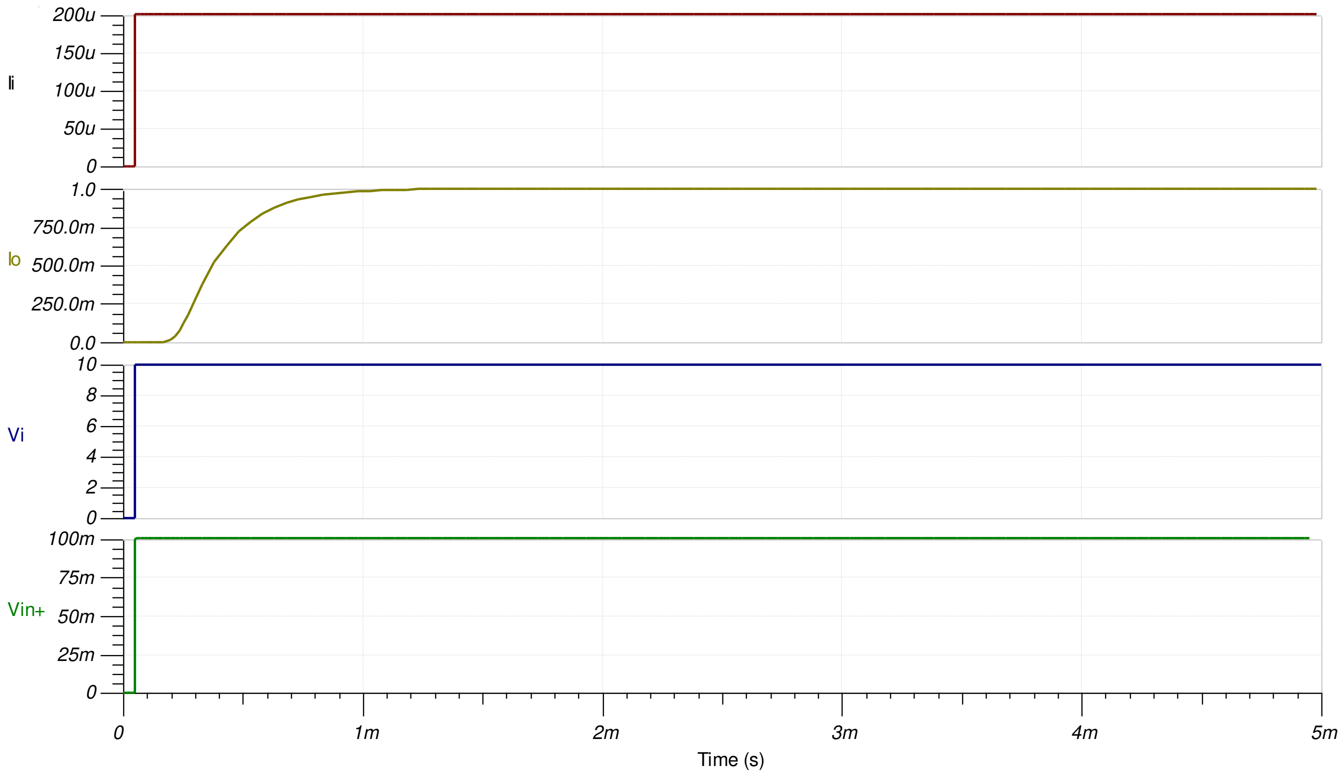
DC Simulation Results



AC Simulation Results



Transient Simulation Results



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation File: SBOMB58.
3. TI Precision Labs

Design Featured Op Amp

TLV9102	
V_{ss}	±1.35V to ±8V, 2.7V to 16V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	120µA
I_b	10pA
UGBW	1.1MHz
SR	4.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9102	

Design Alternate Op Amp

TLV9152	
V_{ss}	±1.35V to ±8V, 2.7V to 16V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	125µV
I_q	560µA
I_b	10pA
UGBW	4.5MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9152	

Voltage-to-current (V-I) converter circuit with MOSFET

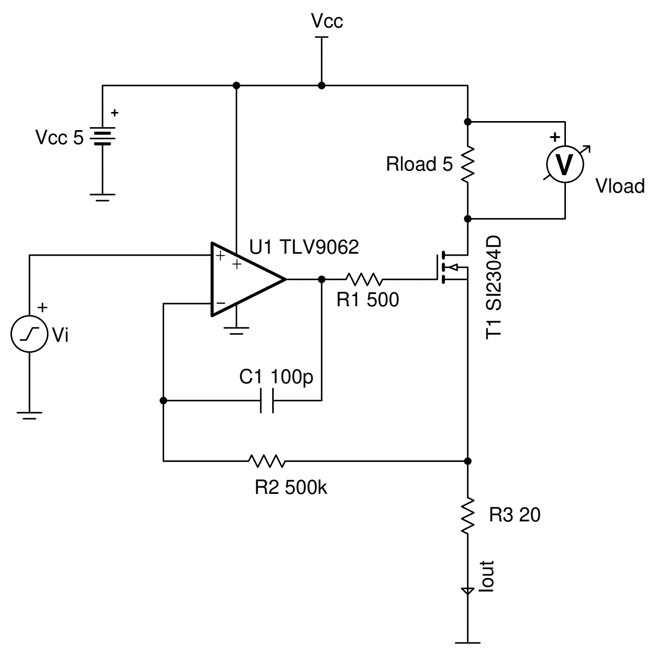
Amplifiers

Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	I_{oMin}	I_{oMax}	Vcc	Vee
0V	2V	0mA	100mA	5V	0V

Design Description

This single-supply, low-side, V-I converter delivers a well-regulated current to a load which can be connected to a voltage greater than the op-amp supply voltage. The circuit accepts an input voltage between 0V and 2V and converts it to a current between 0mA and 100mA. The current is accurately regulated by feeding back the voltage drop across a low-side current-sense resistor, R_3, to the inverting input of the op amp.



Design Notes

1. A device with a rail-to-rail input (RRI) or common-mode voltage that extends to GND is required.
2. R_1 helps isolate the amplifier from the capacitive load of the MOSFET gate.
3. Feedback components R_2 and C_1 provide compensation to ensure stability during input or load transients, which also helps reduce noise. R_2 provides a DC feedback path directly at the current setting resistor (R_3) and C_1 provides a high-frequency feedback path that bypasses the MOSFET.
4. The input bias current will flow through R_2, which will cause a DC error. Therefore, ensure that this error is minimal compared to the offset voltage of the op amp.
5. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions provided in the op amp data sheet.

Design Steps

1. Determine the transfer function.

$$I_o = \frac{V_i}{R_3}$$

2. Calculate the sense resistor, R_3.

$$R_3 = \frac{V_{iMax} - V_{iMin}}{I_{oMax} - I_{oMin}} = \frac{2V - 0V}{100mA - 0mA} = 20\Omega$$

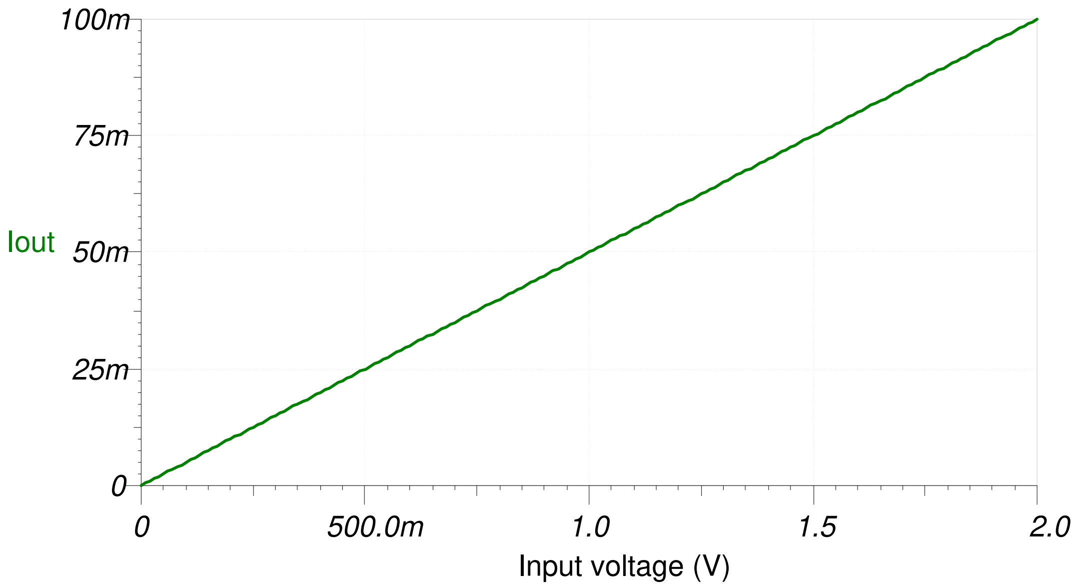
3. Calculate the maximum power dissipated into the sense resistor, R_3, to ensure the resistor power ratings are not exceeded.

$$P_{R_3} = \frac{{V_{iMax}}^2}{R_3} = \frac{2V^2}{20\Omega} = 0.2W$$

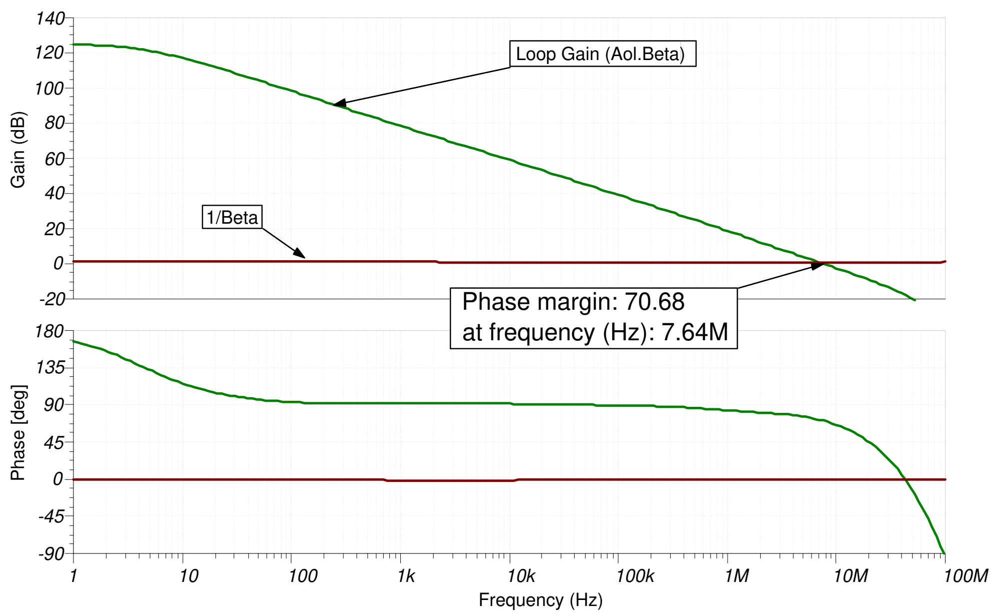
4. See the Design References section, [2] for the design procedure on how to properly size the compensation components, R_1, R_2, and C_1.

Design Simulations

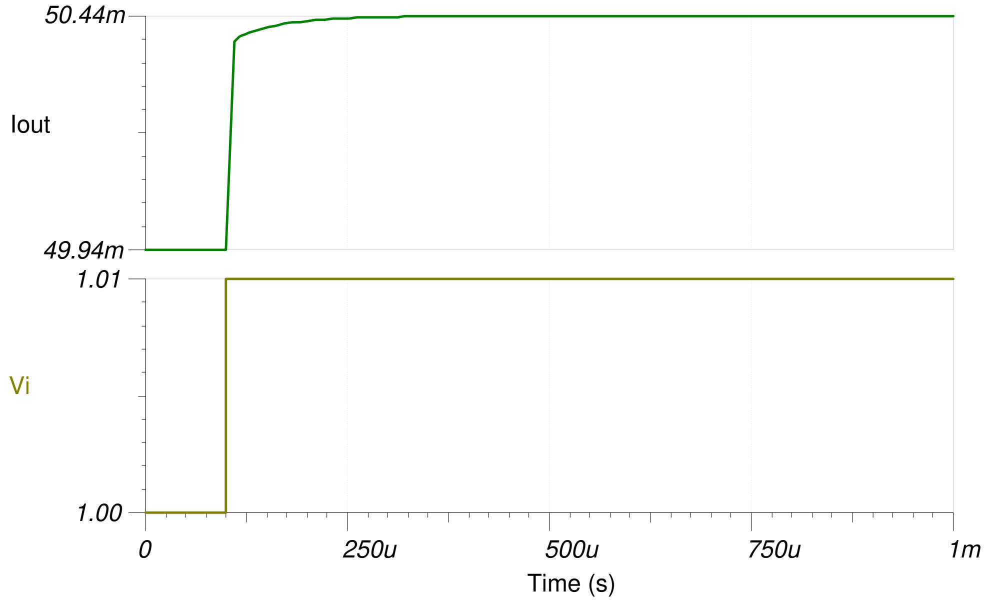
DC Simulation Results



Loop Stability Simulation Results

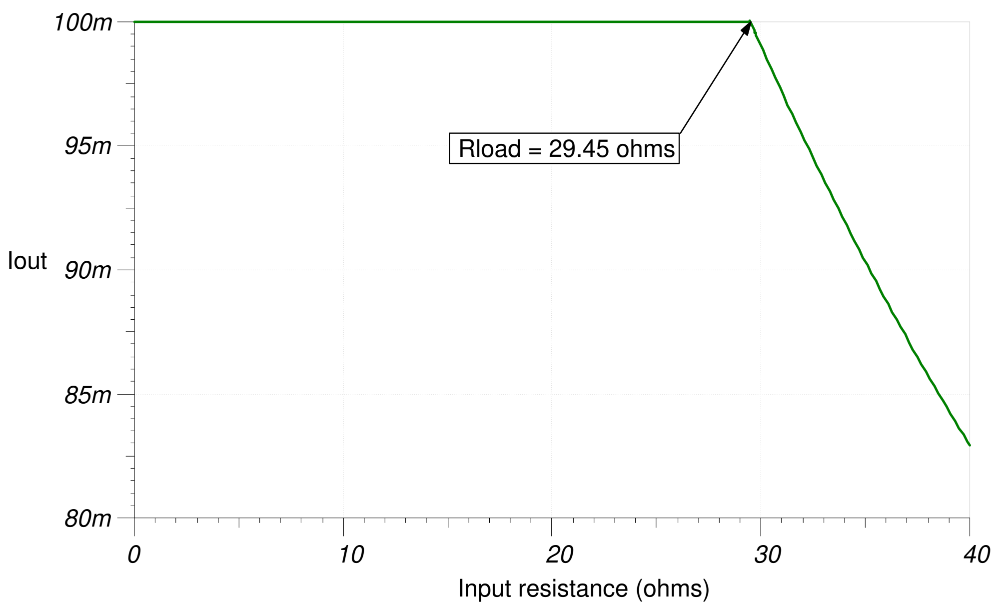


Step Response



Compliance Voltage

Set output to full-scale (100 mA) and test the maximum load resistance.



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. TI Precision Labs

Design Featured Op Amp

TLV9062	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	(V_{cc} + 60mV) to (Vee – 60mV) at R_L = 2kΩ
V_{os}	1.6mV
I_q	0.538mA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV9042	OPA2182
V_{ss}	1.2V to 5.5V	4.5V to 36V
V_{inCM}	Rail-to-rail	(V_{ee} – 0.1V) to (V_{cc} – 2.5V)
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	±0.6mV	±0.45µV
I_q	0.01mA	0.85mA
I_b	±1pA	±50pA
UGBW	350kHz	5MHz
SR	0.2V/µs	10V/µS
#Channels	1,2,4	2
	www.ti.com/product/TLV9042	www.ti.com/product/OPA2182

"Improved" Howland current pump circuit

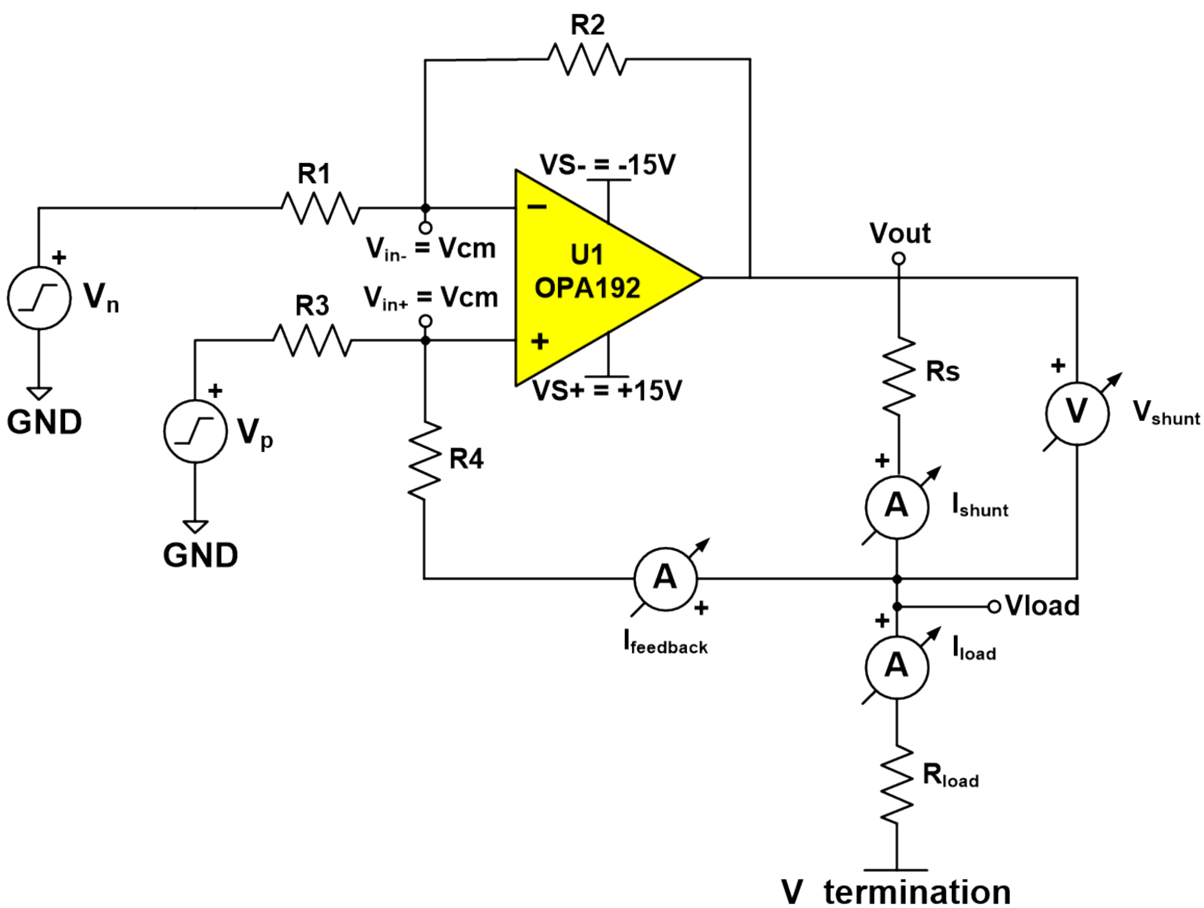
TEXAS INSTRUMENTS

Design Goals

Input V_{in} ($V_p - V_n$)		Output		Supply		
V_{inMin}	V_{inMax}	I_{Min}	I_{Min}	VS+	VS-	V_{ref}
–5V	5V	–25mA	25mA	15V	–15V	0V

Design Description

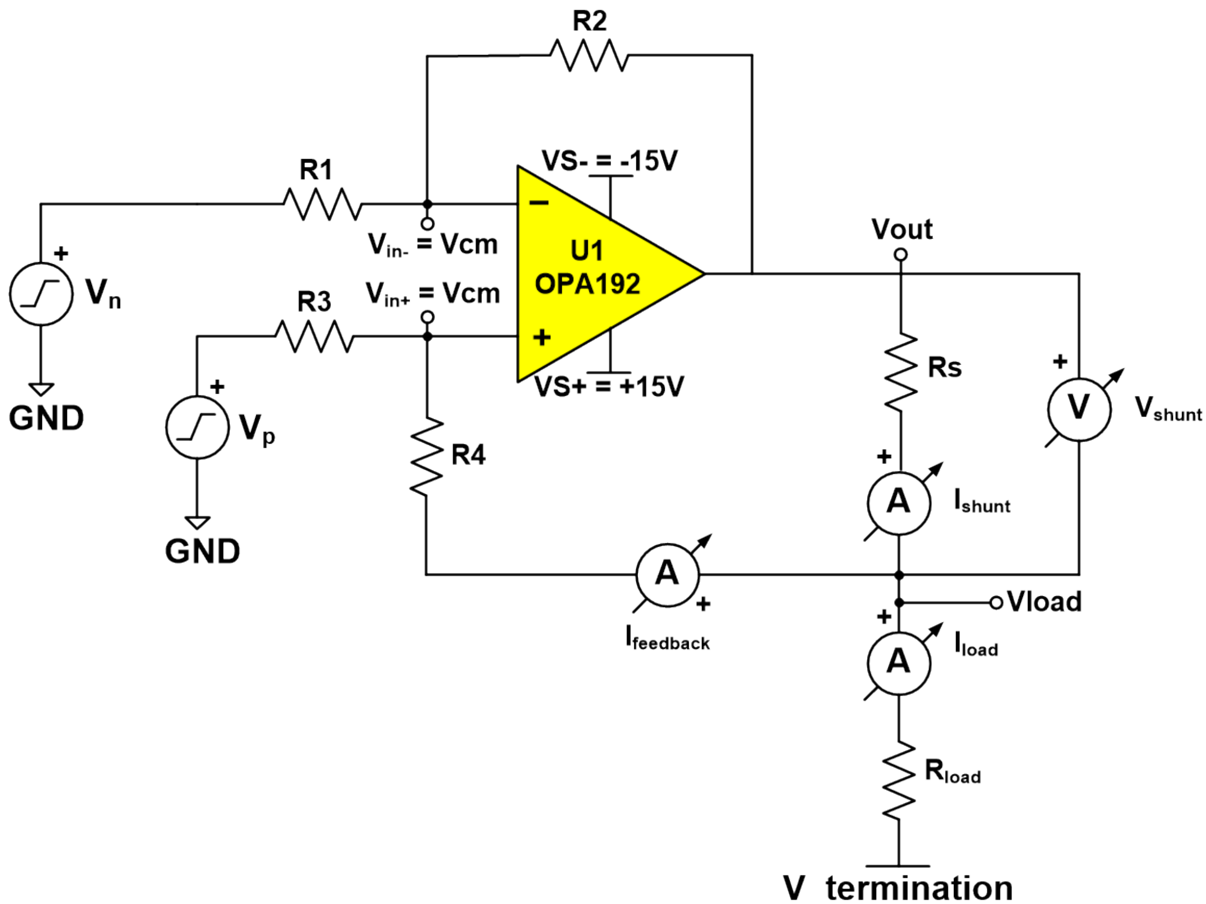
The "Improved" Howland current pump is a circuit that uses a difference amplifier to impose a voltage across a shunt resistor (Rs), creating a voltage-controlled bipolar (source or sink) current source capable of driving a wide range of load resistance. See the *AN-1515 A Comprehensive Study of the Howland Current Pump Application Report* for more information on the functionality of the "Improved" Howland current pump.



Design Notes

1. Ensure common-mode voltages at the inputs (V_{cm} nodes) of the op amp are within the V_{cm} range listed under Electrical Characteristics in the data sheet of the op amp.
2. Refer to the typical "Output Voltage Swing vs. Output Current" graphs in the data sheet of the op amp to account for output swing from rails (V_{out} node).
3. Resistor mismatch will contribute gain error and degrade CMRR of the circuit.
4. Error in final results can be expected due to $I_{feedback}$ current. Placing high-value resistors will limit the effect of this current, but will add thermal noise to the circuit. Possible bandwidth limitations and stability issues caused by large resistances and parasitic capacitances in the circuit also become more prevalent.
5. In an ideal "Improved" Howland current pump, resistor R4 is usually set equal to R2-Rs, which slightly alters the feedback network but results in the expected I_{load} value. Accuracy of these resistors will limit the effectiveness of the technique at reducing errors.
6. Special precautions should be taken when driving reactive loads.
7. A typical design procedure first calculates the gain for a known output current and shunt resistor; then sets R1 and scales R2 through R4 accordingly. This can be an iterative process.

Design Steps



- Calculating gain (G) for a given I_{load} and shunt resistor:

$$G(V/V) = \frac{I_{load} \times R_S}{V_p - V_n}$$

$$G(V/V) = \frac{R2}{R1}, \quad \frac{R2}{R1} = \frac{R4 + R_S}{R3}$$

- Ensure V_{out} is within the voltage output swing from rails (V_{out_Min}, V_{out_Max}) of the op amp at a specific output current specified in the data sheet of the op amp:

$$V_{out\_Min} < V_{out} < V_{out\_Max}$$

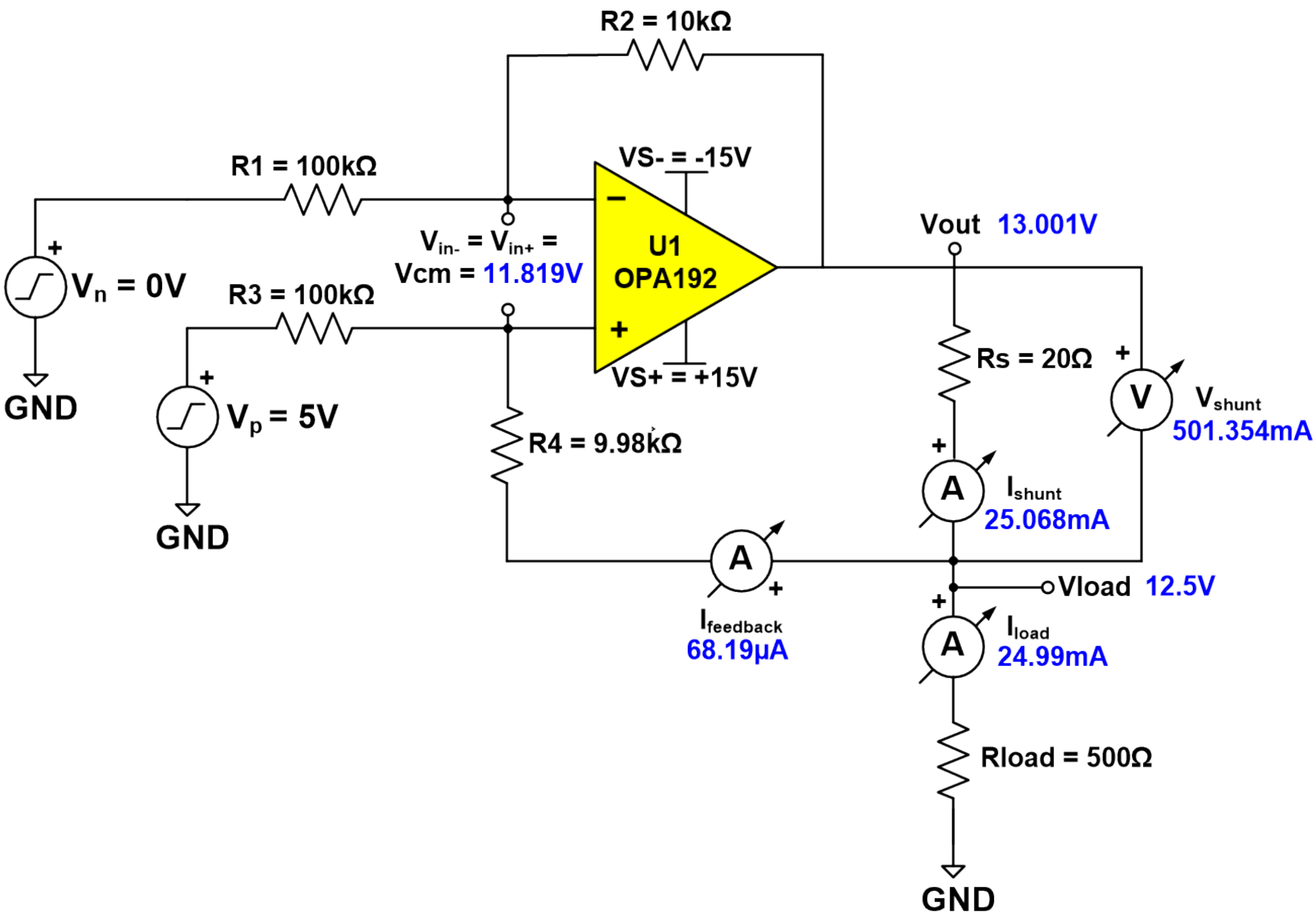
$$U1\_V_{out} = V_{termination} + (I_{load} \times R_{load}) + V_{shunt}$$

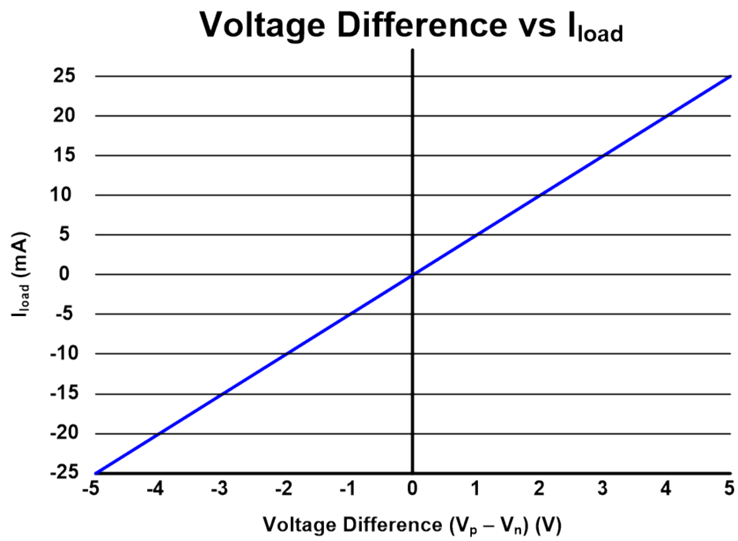
Design Simulations

A design goal of ±25mA of output current from an input voltage difference of ±5V and a 500-Ω load results in a V_{load} value of ±12.5V assuming a $V_{termination}$ voltage of 0V. The remaining ±2.5 volts must accommodate the selected output swing-to-rail of the op amp as well as the maximum voltage across the shunt. For these reasons, a 20-Ω shunt resistor and a gain of 1/10 (V/V) was chosen.

A DC input voltage difference sweep is simulated with a fixed Vn input of 0V and the Vp input swept from –5V to 5V. As the following image shows, the input common-mode range, output swing-to-rail, and output current are within the specifications of the selected op amp. The configuration and results are seen in the following images.

DC Simulation Results




Voltage Difference vs I_{load}
25
20
15
10
5
0
-5
-10
-15
-20
-25
I_{load} (mA)
-5
-4
-3
-2
-1
0
1
2
3
4
5
Voltage Difference (V_p – V_n) (V)

Design References

See the Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See the *AN-1515 A Comprehensive Study of the Howland Current Pump Application Report* for more information on the functionality of the "Improved" Howland current pump resource.

The TI E2E support forum on *Difference Amplifiers* contains information on the importance of matching difference amplifier resistors.

Design Featured Op Amp

OPA192	
V_{ss}	4.5V–36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1
www.ti.com/product/OPA192	

Design Alternate Op Amp

OPA990	
V_{ss}	2.7V–40V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	130µA
I_b	10pA
UGBW	1.1MHz
SR	4.5V/µs
#Channels	1
www.ti.com/product/OPA990	

Analog Engineer's Circuit

Voltage-to-current (V-I) converter circuit with a Darlington transistor

TEXAS INSTRUMENTS

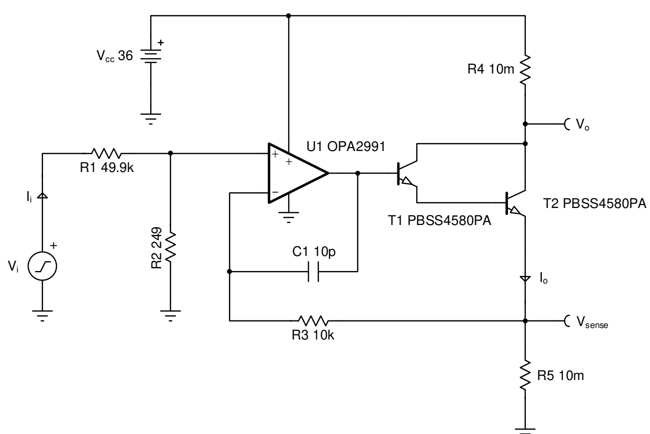
Amplifiers

Design Goals

Input			Output			Supply	
V_{iMin}	V_{iMax}	I_{iMax}	I_{oMin}	I_{oMax}	P_{R5Max}	V_{cc}	V_{ee}
0V	10V	200µA	0A	5A	0.25W	36V	0V

Design Description

This high-side voltage-to-current (V-I) converter delivers a well-regulated current to a load, R_4. The circuit accepts an input voltage from 0V to 10V and converts it to an output current from 0A to 5A. The current is regulated by feeding the voltage across a low-side, current-sense resistor back to the op amp. The output Darlington pair allows for higher current gain than when using a single, discrete transistor.



Design Notes

1. A resistor divider, formed by R_1 and R_2, is implemented at the input to limit the full-scale voltage at the non-inverting terminal of the amplifier and the output sense resistor (R_5).
2. The high current gain of the Darlington pair reduces the demand on the output current of the op amp.
3. Smaller values of R_4 and R_5 lead to an increased load compliance voltage and a reduction in power dissipated in the full-scale, output state.
4. Feedback components R_3 and C_1 provide frequency compensation to ensure the stability of the circuit during transients. They also help reduce noise. R_3 provides a DC feedback path directly at the current setting resistor, R_5, and C_1 provides a high-frequency feedback path that bypasses the NPN pair.
5. The input bias current will flow through R_3, which will cause a DC error. Therefore, ensure that this error is minimal compared to the offset voltage of the op amp.
6. Select an op amp whose linear output voltage swing includes at least $2 \times V_{be}+V_{sense}$. The output voltage of the op amp will be greater than the voltage at the sense resistor by approximaly double the base-to-emitter voltage, V_{be}.
7. Use the op amp in its linear operating region, specified under the A_{OL} test conditions of the data sheet.
8. If needed, an isolation resistor may be placed between the high-frequency feedback path and the base of T1 for stability.

Design Steps

The transfer function of this circuit is provided in the following steps:

$$I_o = V_i \times \frac{R_2}{R_5 \times (R_1 + R_2)}$$

1. Using the specifications for the maximum output power dissipation and the maximum output current, determine the maximum value of V_{sense}.

$$\mathrm{V_{R5Max}} = \mathrm{V_{senseMax}} = \frac{\mathrm{P_{R5Max}}}{\mathrm{I_{oMax}}} = \frac{0\ .25\ \mathrm{W}}{5\mathrm{A}} = 50\mathrm{mV}$$

2. Calculate the sense resistance, R_5.

$$R_5 = \frac{V_{\mathrm{senseMax}}}{I_{\mathrm{oMax}}} = \frac{50\mathrm{mV}}{5\mathrm{A}} = 10\mathrm{m\Omega}$$

3. Select values for R_1 and R_2 based on the maximum allowable input current, I_{iMax}, and the desired $V_{senseMax}$ voltage.

$$R_1 = \frac{V_{\mathrm{senseMax}}}{I_{\mathrm{iMax}}} = \frac{50\mathrm{mV}}{200\mu\mathrm{A}} = 250\Omega \approx 249\Omega(\text{Standard Value})$$

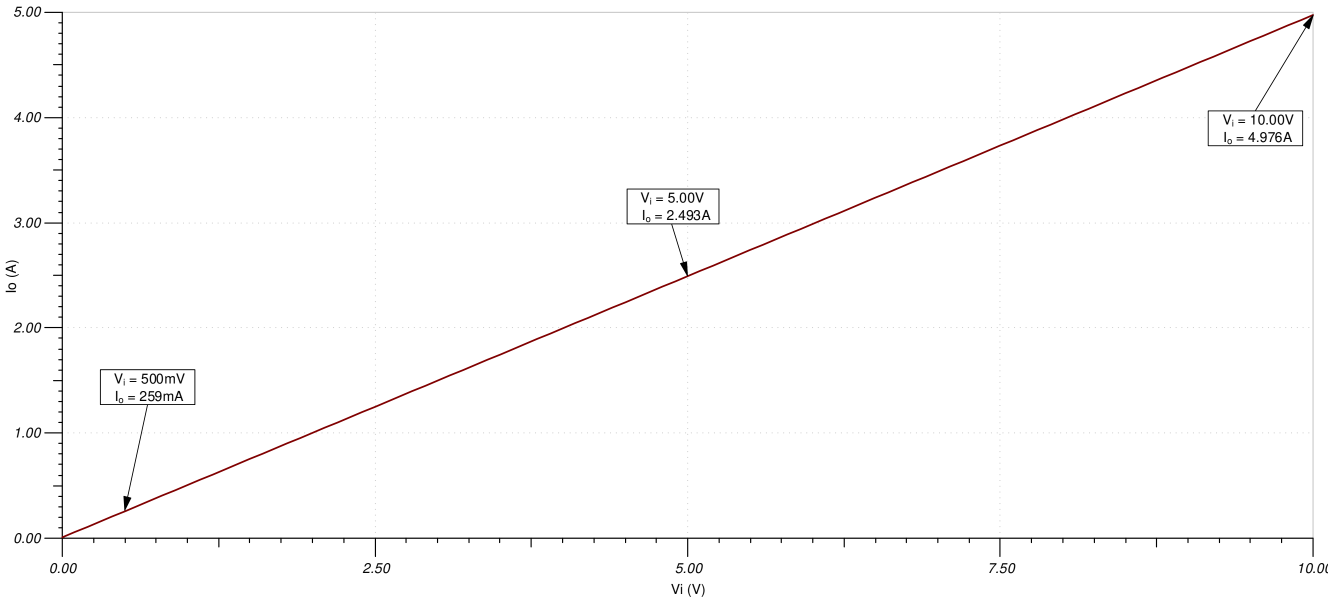
$$V_{\mathrm{senseMax}} = V_{\mathrm{iMax}} \times \left(\frac{R_2}{R_1 + R_2}\right)$$

$$R_2 = 49.6\mathrm{k\Omega} \approx 49.9\mathrm{k\Omega}\ (\text{Standard Value})$$

4. See the Design References section [2] for the design procedure on how to properly size the compensation components, R_3 and C_1.

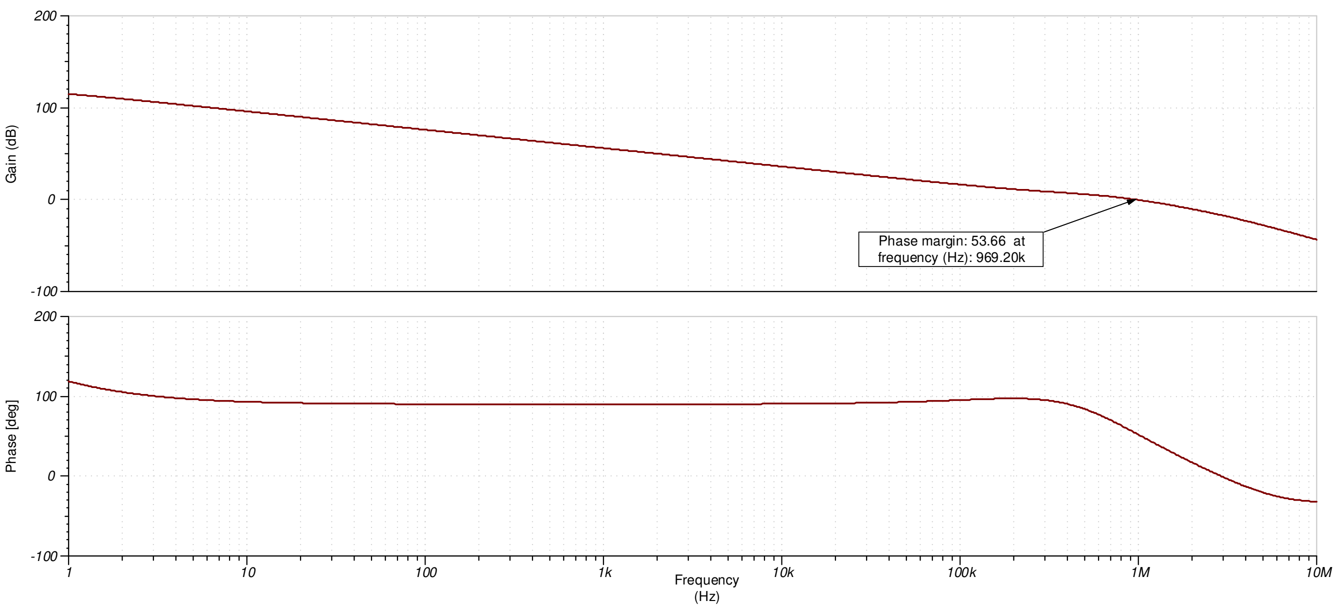
Design Simulations

DC Simulation Results

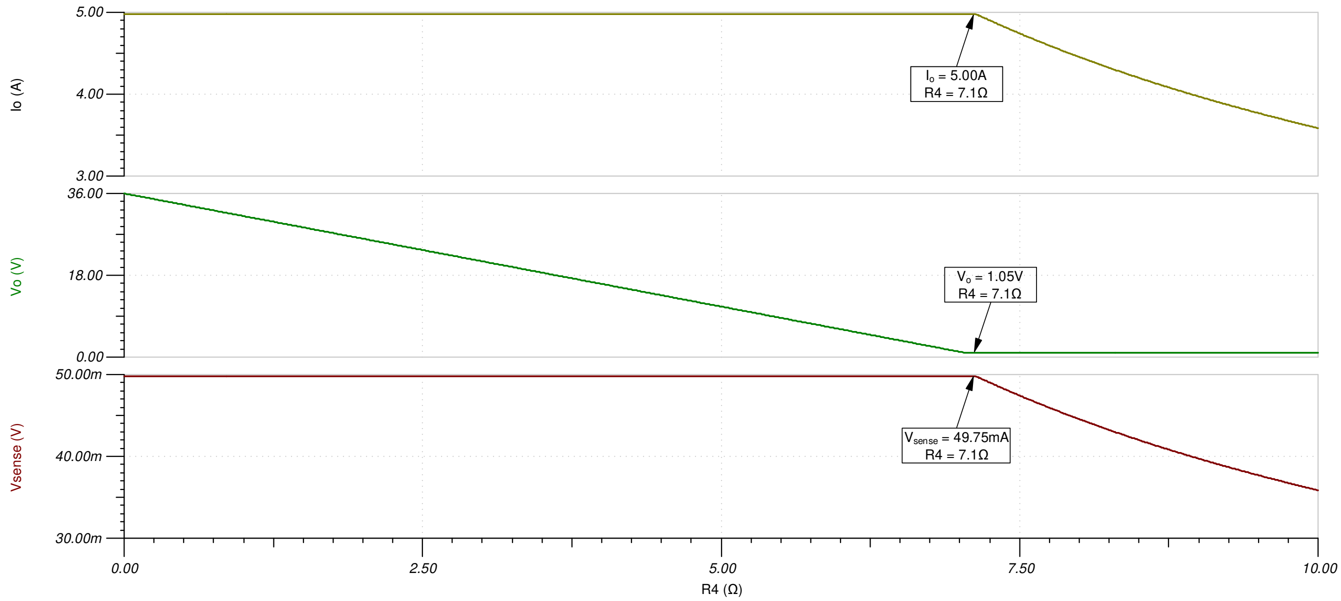


Loop Stability Simulation Results

Loop gain phase is 53 degrees.



Compliance Voltage Simulation Results



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. TI Precision Labs

Design Featured Op Amp

OPA2991	
V_{ss}	2.7V to 40V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	125µV
I_q	560µA
I_b	10pA
UGBW	4.5MHz
SR	21V/µs
#Channels	1, 2, 4
www.ti.com/product/opa2991	

Design Alternate Op Amp

OPA197	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/opa197	

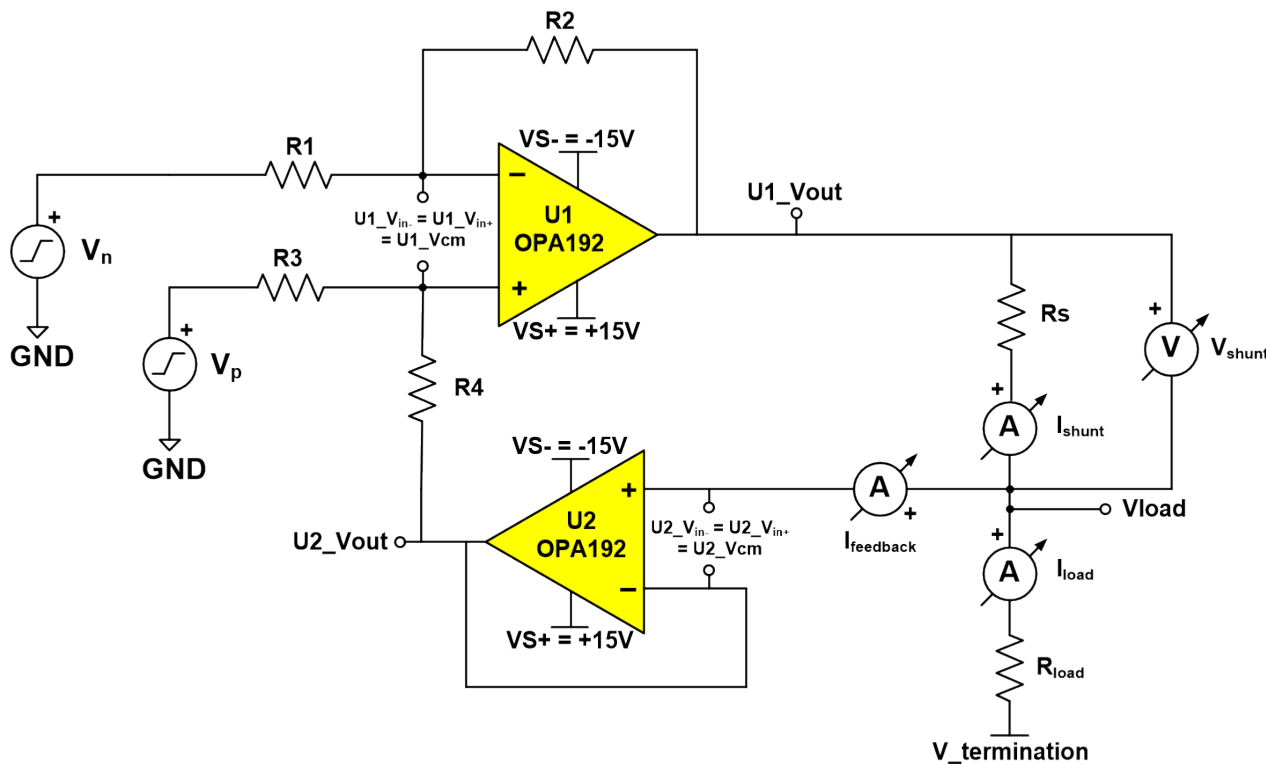
"Improved" Howland current pump with buffer circuit

Design Goals

Input V_{in} ($V_p - V_n$)		Output		Supply		
V_{inMin}	V_{inMax}	I_{Min}	I_{Max}	VS+	VS-	V_{ref}
–5V	5V	–25mA	25mA	15V	–15V	0V

Design Description

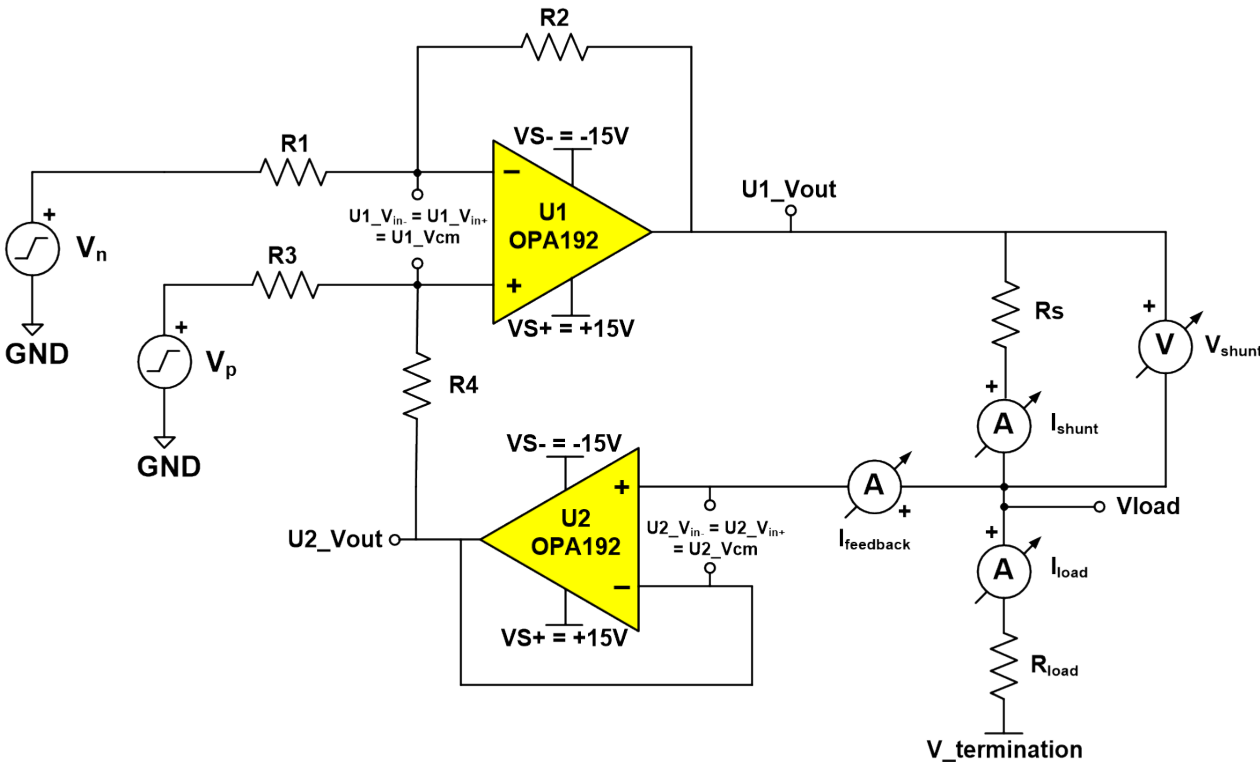
The "Improved" Howland current pump is a circuit that uses a difference amplifier to impose a voltage across a shunt resistor (Rs), creating a voltage-controlled bipolar (source or sink) current source capable of driving a wide range of load resistance. See the *AN-1515 A Comprehensive Study of the Howland Current Pump Application Report* for more information on the functionality of the "Improved" Howland current pump.



Design Notes

1. Ensure common-mode voltages at the inputs (V_{cm} nodes) of both op amps are within their V_{cm} range listed under Electrical Characteristics in the data sheet of the op amp.
2. Refer to the typical *Output Voltage Swing vs. Output Current* graphs in the data sheet to account for output swing from rails (V_{out} nodes) for both op amps.
3. Resistor mismatch will contribute gain error and degrade CMRR of the circuit.
4. The buffer offers improved output impedance of the current source nearly eliminating $I_{feedback}$ current. This allows the use of smaller resistor values for R1 through R4, reducing thermal noise. Possible bandwidth limitations and stability issues caused by large resistances and parasitic capacitances in the circuit are also reduced.
5. Special precautions should be taken when driving reactive loads.
6. A typical design procedure first calculates the gain for a known output current and shunt resistor; then sets R1 and scales R2 through R4 accordingly. This can be an iterative process.
7. The figures use two OPA192 op amps, but in practice a single chip OPA2192 can be used.

Design Steps



1. Calculating gain (G) for a given I_{load} and shunt resistor*:*

$$G(V/V) = \frac{I_{load} \times R_S}{V_p - V_n}$$

$$G(V/V) = \frac{R2}{R1}, \quad (R1 = R3, R2 = R4)$$

2. Ensure V_{out} for both op amps are within their voltage output swing from rails (V_{out_Min}, V_{out_Max}) at a specific output current specified in the data sheet.The following formula can be used to calculate U1_V_{out} for U1 OPA192. U2_V_{out} for U2 OPA192 will be V_{load}.

$$V_{out\_Min} < V_{out} < V_{out\_Max}$$

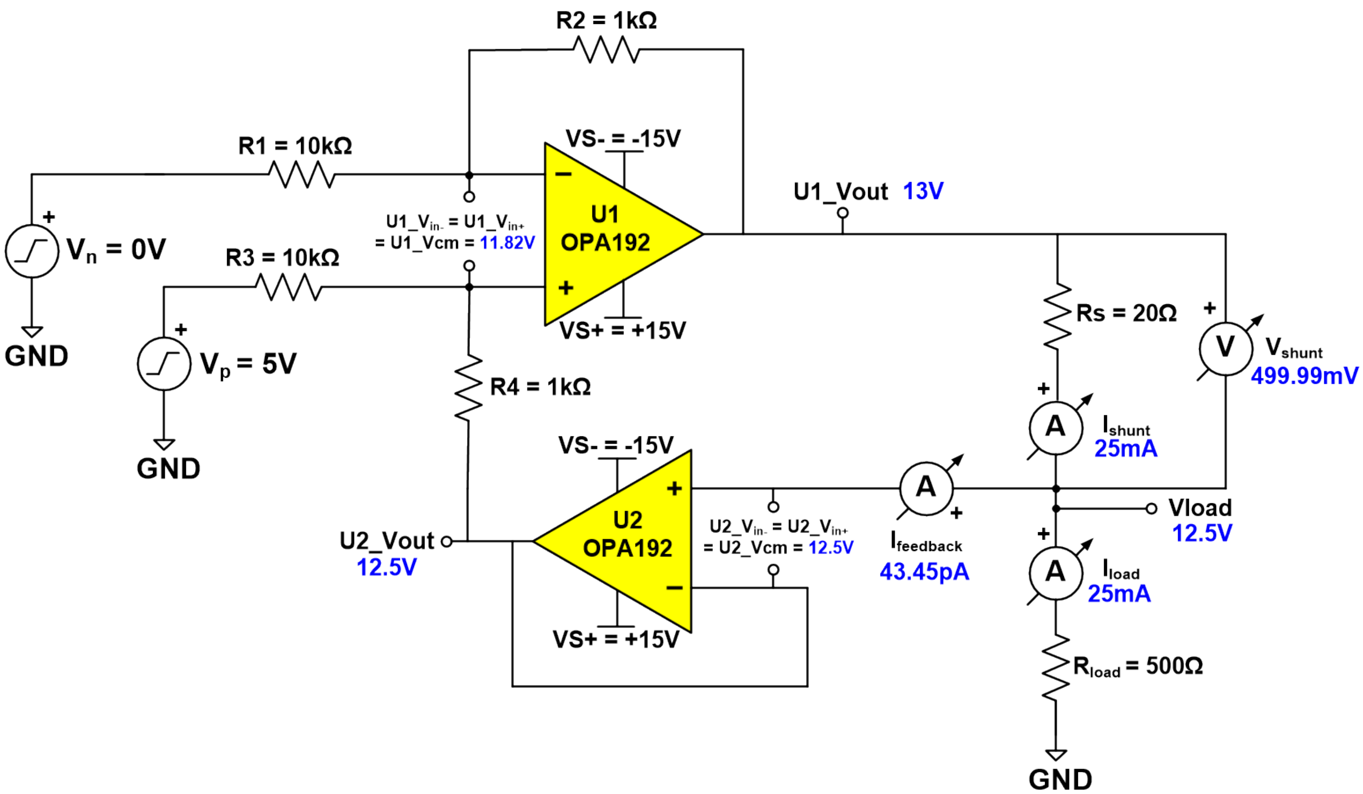
$$U1\_V_{out} = V_{termination} + (I_{load} \times R_{load}) + V_{shunt}$$

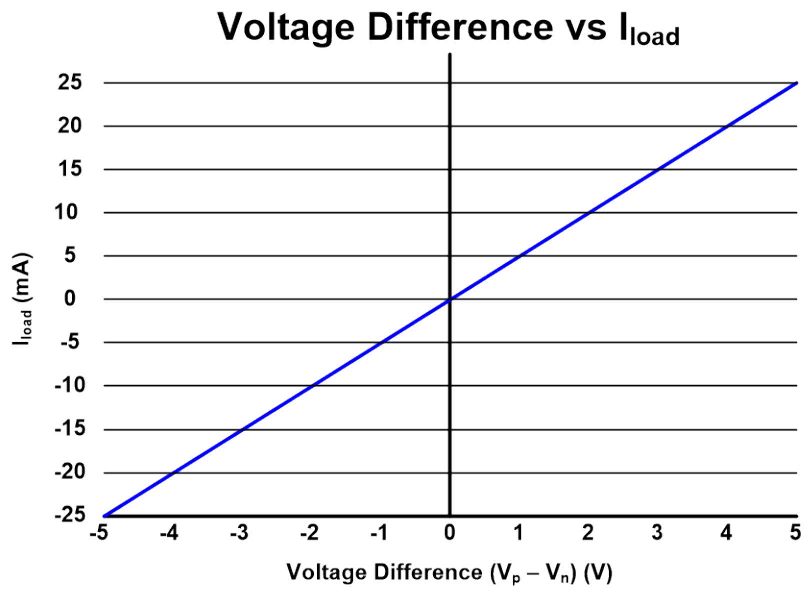
Design Simulations

A design goal of ±25mA of output current from an input voltage difference of ±5V and a 500-Ω load results in a V_{load} value of ±12.5V, assuming a $V_{termination}$ voltage of 0V. The remaining ±2.5 volts must accommodate the output swing-to-rail of the selected op amp as well as the maximum voltage across the shunt. For these reasons a 20-Ω shunt resistor and a gain of 1/10 (V/V) was chosen. This V_{load} value is also within the voltage compliance range of the buffer.

A DC input voltage difference sweep is simulated with a fixed Vn input of 0V and the Vp input swept from –5V to 5V. As the following image shows, the input common-mode range, output swing-to-rail, and output current are within the specifications of the selected op amps. The configuration and results follow.

DC Simulation Results




Voltage Difference vs I_load
25
20
15
10
5
0
-5
-10
-15
-20
-25
I_load (mA)
-5
-4
-3
-2
-1
0
1
2
3
4
5
Voltage Difference (Vp – Vn) (V)

Design References

See the Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See the *AN-1515 A Comprehensive Study of the Howland Current Pump Application Report* for more information on the functionality of the “Improved” Howland current pump resource.

The TI E2E support forum on *Difference Amplifiers* contains information on the importance of matching difference amplifier resistors.

Design Featured Op Amp

OPA2192	
V_{ss}	4.5V–36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	2
www.ti.com/product/OPA2192	

Design Alternate Op Amp

OPA2990	
V_{ss}	2.7V–40V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	120µA
I_b	10pA
UGBW	1.1MHz
SR	4.5V/µs
#Channels	2
www.ti.com/product/OPA2990	

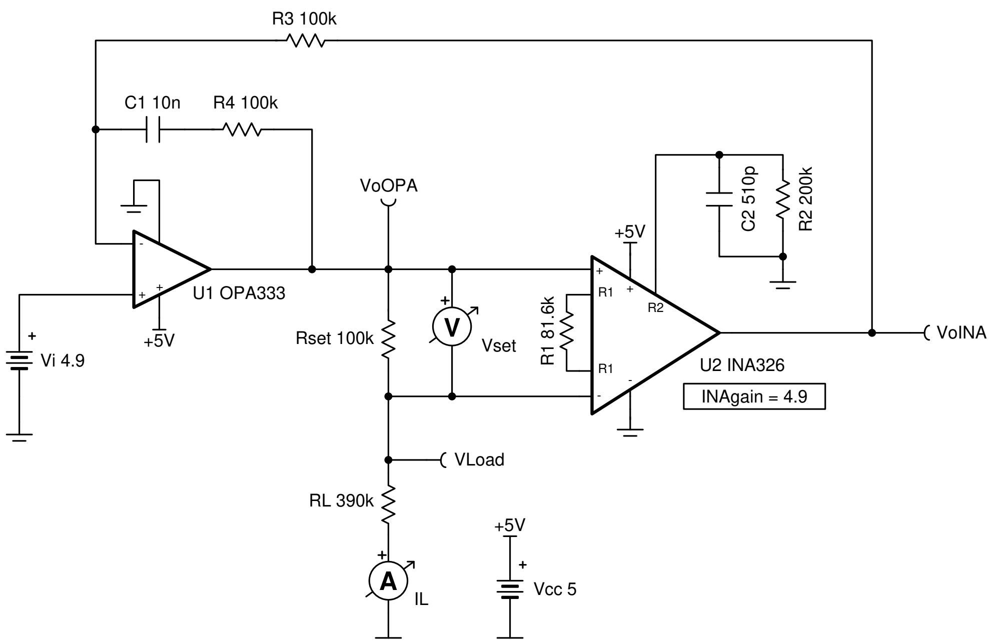
Low-Level Voltage-to-Current Converter Circuit

Design Goals

Input		Output		Supply		Load Resistance (R_L)	
V_{iMin}	V_{iMax}	I_{LMin}	I_{LMax}	V_{cc}	V_{ee}	R_{LMin}	R_{LMax}
0.49 V	4.9 V	1 µA	10 µA	5 V	0 V	0 Ω	390 kΩ

Design Description

This circuit delivers a precise low-level current, I_L, to a load, R_L. The design operates on a single 5 V supply and uses one precision low-drift op amp and one instrumentation amplifier. Simple modifications can change the range and accuracy of the voltage-to-current (V-I) converter.



Design Notes

1. Voltage compliance is dominated by op amp linear output swing (see data sheet A_{OL} test conditions) and instrumentation amplifier linear output swing. See the *Common-Mode Input Range Calculator for Instrumentation Amplifiers* for more information.
2. Voltage compliance, along with R_{LMin}, R_{LMax}, and R_{set} bound the I_L range.
3. Check op amp and instrumentation amplifier input common-mode voltage range.
4. Stability analysis must be done to choose R_4 and C_1 for stable operation.
5. Loop stability analysis to select R_4 and C_1 will be different for each design. The compensation shown is only valid for the resistive load ranges used in this design. Other types of loads, op amps, or instrumentation amplifiers, or both will require different compensation. See the ***Design References*** section for more op amp stability resources.

Design Steps

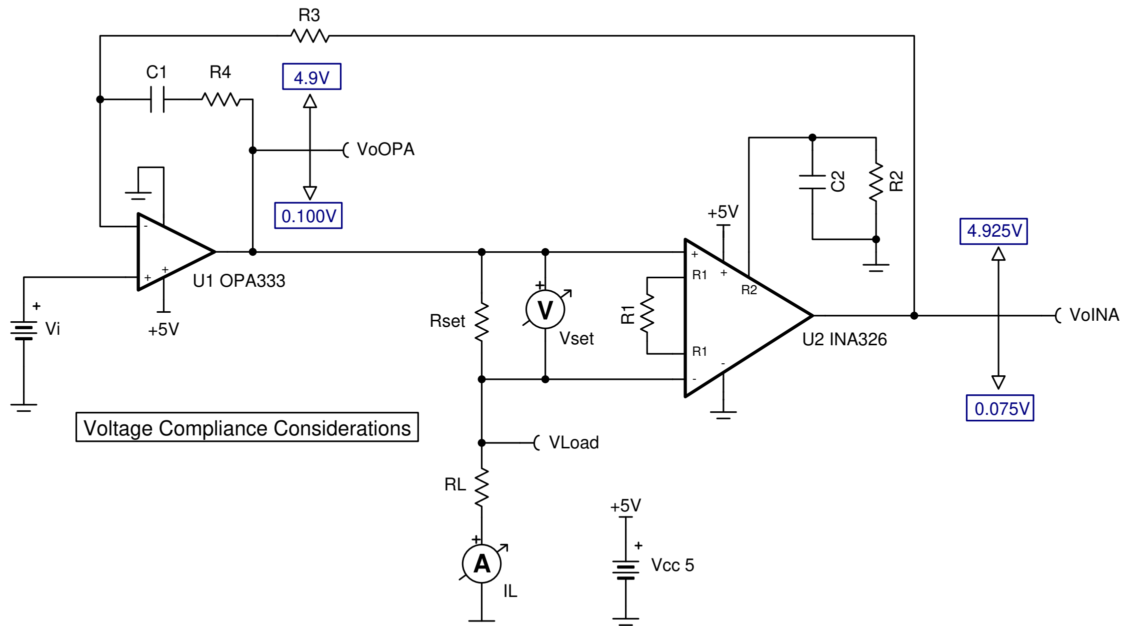
1. Select R_{set} and check I_{LMin} based on voltage compliance.

$$I_{LMax} = \frac{V_{oOPAMax}}{R_{set} + R_{LMax}}$$

$$10\mu A = \frac{4.9V}{R_{set} + 390k\Omega} \rightarrow R_{set} = 100k\Omega$$

$$I_{LMin} = \frac{V_{oOPAMin}}{R_{set} + R_{LMin}}$$

$$I_{LMin} = \frac{0.1V}{100k\Omega + 0\Omega} = 1\mu A$$



2. Compute instrumentation amplifier gain, G.

$$V_{setMin} = I_{LMin} \times R_{set} = 1\mu A \times 100k\Omega = 0.1V$$

$$V_{setMax} = I_{LMax} \times R_{set} = 10\mu A \times 100k\Omega = 1V$$

$$G = \frac{V_{iMax} - V_{iMin}}{V_{setMax} - V_{setMin}}$$

$$G = \frac{4.9V - 0.49V}{1V - 0.1V} = 4.9$$

3. Choose R_1 for INA326 instrumentation amplifier gain, G. Use data sheet recommended R_2 = 200 kΩ and C_2 = 510 pF.

$$G = 2 \times \left(\frac{R_2}{R_1}\right)$$

$$R_1 = \frac{2 \times R_2}{G}$$

$$R_1 = \left(\frac{2 \times 200k\Omega}{4.9}\right) = 81.6327k\Omega \approx 81.6k\Omega$$

4. The final transfer function of the circuit follows:

$$I_L = \frac{V_i}{G \times R_{set}}$$

$$I_L = \frac{V_i}{4.9 \times 100k\Omega} = \frac{V_i}{490k\Omega}$$

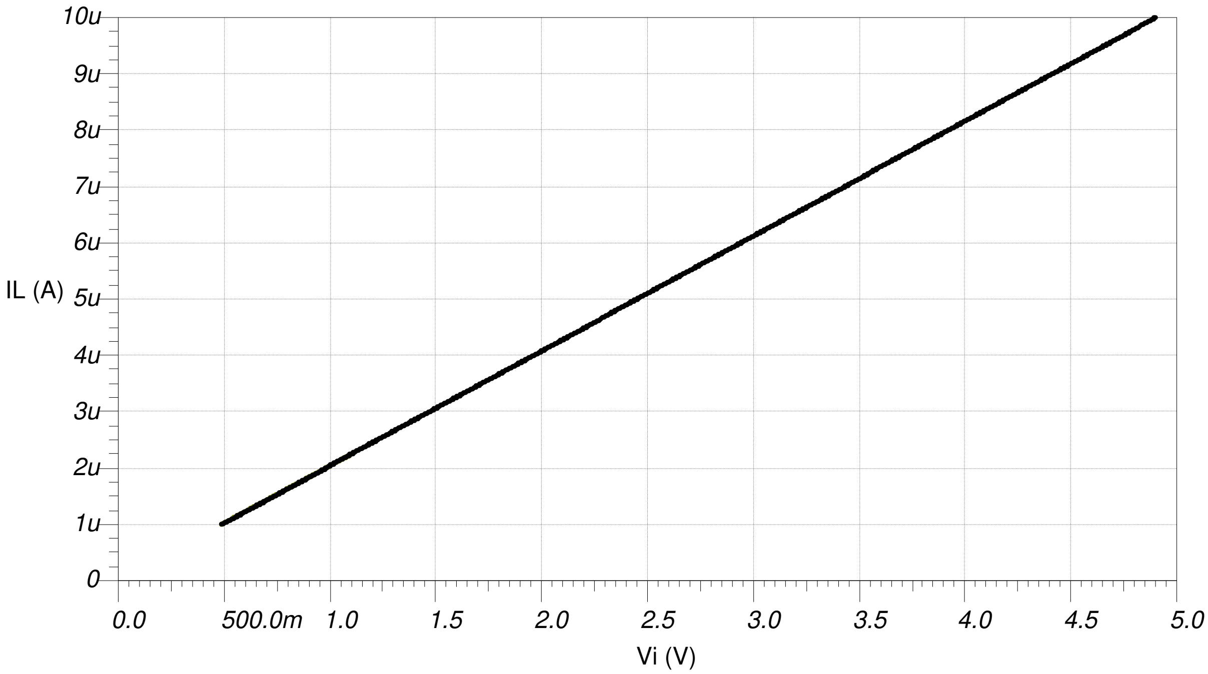
$$V_i = 0.49V \rightarrow I_L = 1\mu A$$

$$V_i = 4.9V \rightarrow I_L = 10\mu A$$

Design Simulations

DC Simulation Results

V_i	R_L	I_L	V_{oOPA}	V_{oOPA} Compliance	V_{oINA}	V_{oINA} Compliance
0.49 V	0 Ω	0.999627 µA	99.982723 mV	100 mV to 4.9 V	490.013346 mV	75 mV to 4.925 V
0.49 V	390 kΩ	0.999627 µA	489.837228 mV	100 mV to 4.9 V	490.013233 mV	75 mV to 4.925 V
4.9 V	0 Ω	9.996034 µA	999.623352 mV	100 mV to 4.9 V	4.900016 V	75 mV to 4.925 V
4.9 V	390 kΩ	9.996031 µA	4.898075 V	100 mV to 4.9 V	4.900015 V	75 mV to 4.925 V



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the TINA-TI™ circuit simulation file, SBOMAT8.

See TIPD107.

See Solving Op Amp Stability Issues - E2E FAQ.

See TI Precision Labs - Op Amps.

Design Featured Op Amp

OPA333	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2 µV
I_q	17 µA/Ch
I_b	70 pA
UGBW	350 kHz
SR	0.16 V/µs
#Channels	1 and 2
OPA333	

Design Featured Instrumentation Amplifier

INA326	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	20 µV
I_q	2.4 mA
I_b	0.2 nA
UGBW	1 kHz (set by 1 kHz filter)
SR	0.012 V/µs (set by 1 kHz filter)
#Channels	1
INA326	

Analog Engineer's Circuit

Single-supply, 2nd-order, multiple feedback low-pass filter circuit

TEXAS INSTRUMENTS

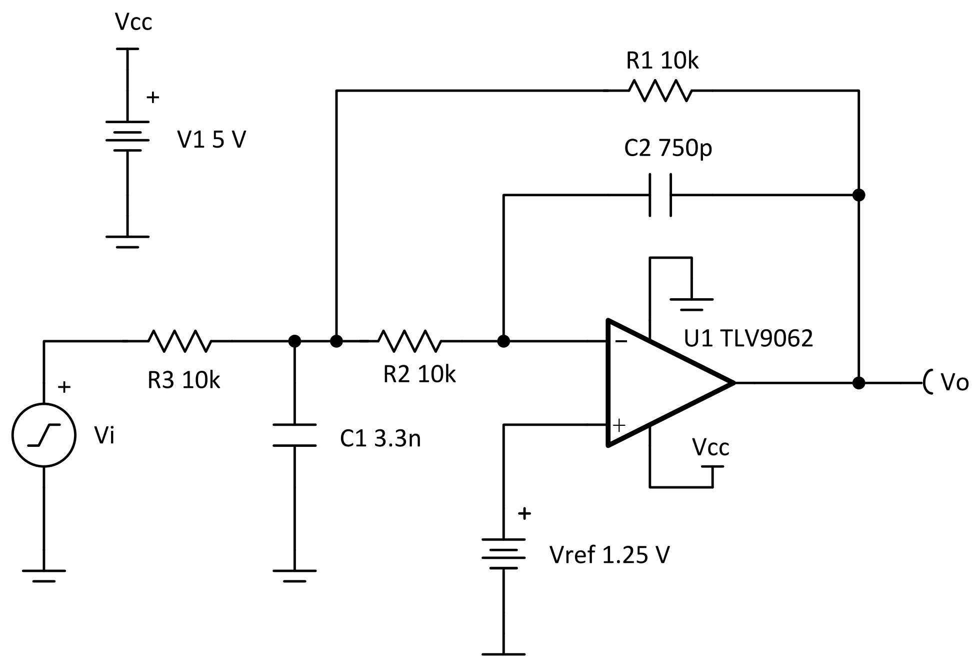
Amplifiers

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–2.45V	+2.45V	0.05V	4.95V	5V	0V

Gain	Cutoff Frequency (f_c)	V_{ref}
–1V/V	10kHz	1.25V

Design Description

The multiple-feedback (MFB) low-pass filter (LP filter) is a second-order active filter. V_{ref} provides a DC offset to accommodate for single-supply applications. This LP filter inverts the signal (Gain = –1V/V) for frequencies in the pass band. An MFB filter is preferable when the gain is high or when the Q-factor is large (for example, 3 or greater).



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_c.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).

Design Steps

The first step in design is to find component values for the normalized cutoff frequency of 1 radian/second. In the second step the cutoff frequency is scaled to the desired cutoff frequency with scaled component values.

The transfer function for a second-order MFB low-pass filter is given by:

$$H(s) = \frac{\frac{1}{R_2 \times R_3 \times C_1 \times C_2}}{s^2 + s \times \frac{1}{C_1}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right) + \frac{1}{R_1 \times R_2 \times C_1 \times C_2}}$$

$$H(s) = \frac{b_0}{s^2 + a_1 \times s + a_0}$$

$$\text{Here, } \; a_1 = \frac{1}{C_1}\left(\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right), \; a_0 = \frac{1}{R_1 \times R_2 \times C_1 \times C_2}$$

1. Set normalized values of R_1 and R_2 (R_{1n} and R_{2n}) and calculate normalized values of C_1 and C_2 (C_{1n} and C_{2n}) by setting w_c to 1 radian/sec (or fc = 1 / (2 × π) Hz). For a 2nd-order Butterworth filter, (see the *Butterworth Filter Table* in the *Active Low-Pass Filter Design Application Report*).

$$\omega_c = 1\,\frac{\text{radian}}{\text{second}} \rightarrow a_0 = 1,\, a_1 = \sqrt{2},\, \text{let } R_{1n} = R_{2n} = R_{3n} = 1$$

$$\text{Then } C_{1n} \times C_{2n} = 1 \text{ or } C_{2n} = \frac{1}{C_{1n}},\; a_1 = \frac{3}{C_{1n}} = \sqrt{2}$$

$$\therefore C_{1n} = \frac{3}{\sqrt{2}} = 2.1213\text{ F},\; C_{2n} = \frac{1}{C_{1n}} = 0.4714\text{ F}$$

2. Scale the component values and cutoff frequency. The resistor values are very small and capacitors values are unrealistic, hence these must be scaled. The cutoff frequency is scaled from 1 radian/second to w_0. If *m* is assumed to be the scaling factor, increase the resistors by *m* times, then the capacitor values have to decrease by 1/*m* times to keep the same cutoff frequency of 1 radian/second. If the cutoff frequency is scaled to be w_0, then the capacitor values have to be decreased by $1/w_o$. The component values for the design goals are calculated in steps 3 and 4.

$$R_1 = R_{1n} \times m,\; R_2 = R_{2n} \times m,\; R_3 = R_{3n} \times m$$

$$C_1 = \frac{C_{1n}}{m \times \omega_0} = \frac{2.1213}{m \times \omega_0}\text{F}$$

$$C_2 = \frac{C_{2n}}{m \times \omega_0} = \frac{0.4714}{m \times \omega_0}\text{F}$$

3. Set R_1, R_2, and R_3 to 10kΩ.

$$R_1 = R_{1n} \times m = 10k\Omega,\; R_2 = R_{2n} \times m = 10k\Omega,\; R_3 = R_{3n} \times m = 10k\Omega$$

$$\text{Therefore, } m = 10000$$

4. Calculate C_1 and C_2 based on *m* and w_0.

$$C_1 = \frac{2.1213}{m \times \omega_0}\ \mathrm{F} = \frac{2.1213}{10\mathrm{k} \times 2 \times \pi \times 10\mathrm{kHz}} = 3.376\mathrm{nF} \approx 3.3\mathrm{nF}\ (\mathrm{Standard\ Value})$$

$$C_2 = \frac{0.4714}{m \times \omega_0}\ \mathrm{F} = \frac{0.4714}{10\mathrm{k} \times 2 \times \pi \times 10\mathrm{kHz}} = 0.75\mathrm{nF} \approx 0.75\mathrm{nF}\ (\mathrm{Standard\ Value})$$

5. Calculate the minimum required GBW and SR for f_c. Be sure to use the noise gain for GBW calculations. Do not use the signal gain of –1V/V.

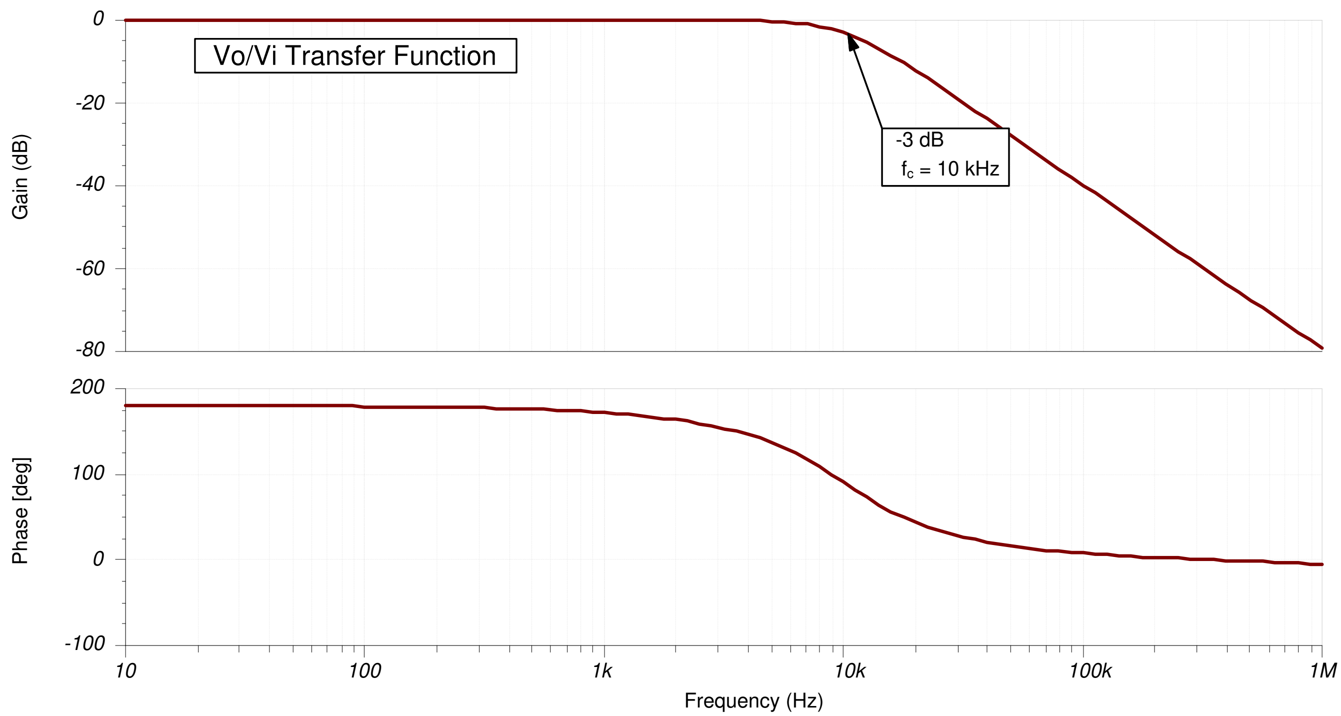
$$\mathrm{GBW} = 100 \times \mathrm{Noise\ Gain} \times f_c = 100 \times 2 \times 10\mathrm{kHz} = 2\mathrm{MHz}$$

$$\mathrm{SR} = 2 \times \pi \times f_c \times V_{\mathrm{iMax}} = 2 \times \pi \times 10\mathrm{kHz} \times 2.45\mathrm{V} = 0.154\frac{\mathrm{V}}{\mu\mathrm{s}}$$

The TLV9062 device has GBW of 10MHz and SR of 6.5 V/µs, so the requirements are met.

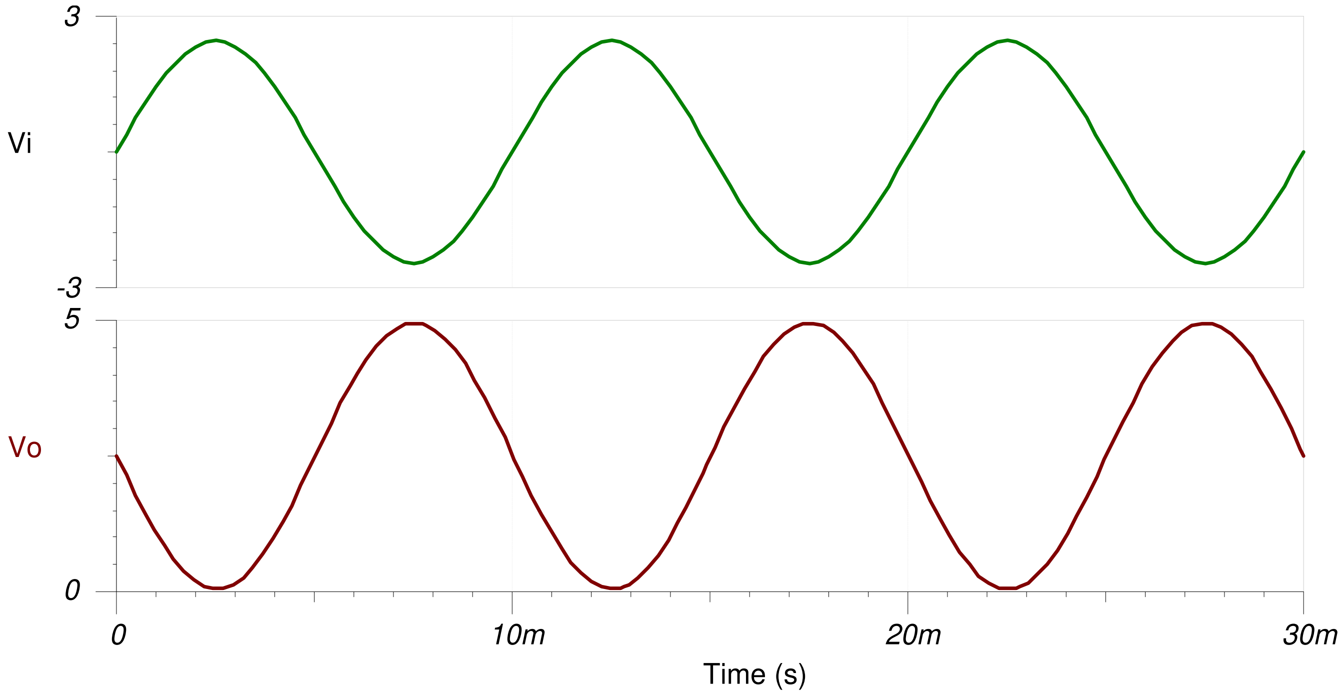
Design Simulations

AC Simulation Results

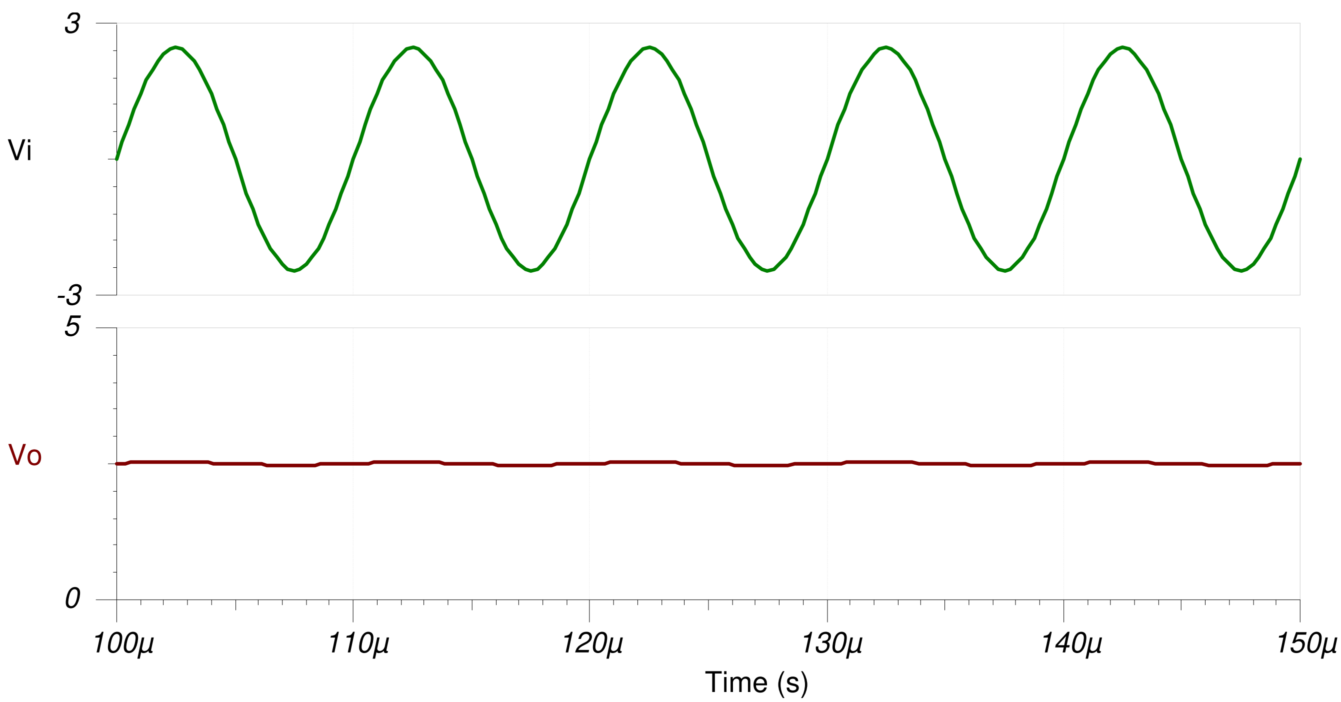


Transient Simulation Results

The following image shows the filter output in response to a 5-V_{pp}, 100-Hz input signal (gain = –1V/V).



The following image shows the filter output in response to a 5-V_{pp}, 10-kHz input signal (gain = –0.01V/V).



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation File SBOC597
3. TI Precision Labs.
4. *Active Low-Pass Filter Design Application Report*

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
Vout	Rail-to-Rail
V_{os}	0.3mV
Iq	538µA
Ib	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
Vout	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
Iq	400µA	650µA
Ib	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Analog Engineer's Circuit

Single-supply, 2nd-order, Sallen-Key low-pass filter circuit

TEXAS INSTRUMENTS

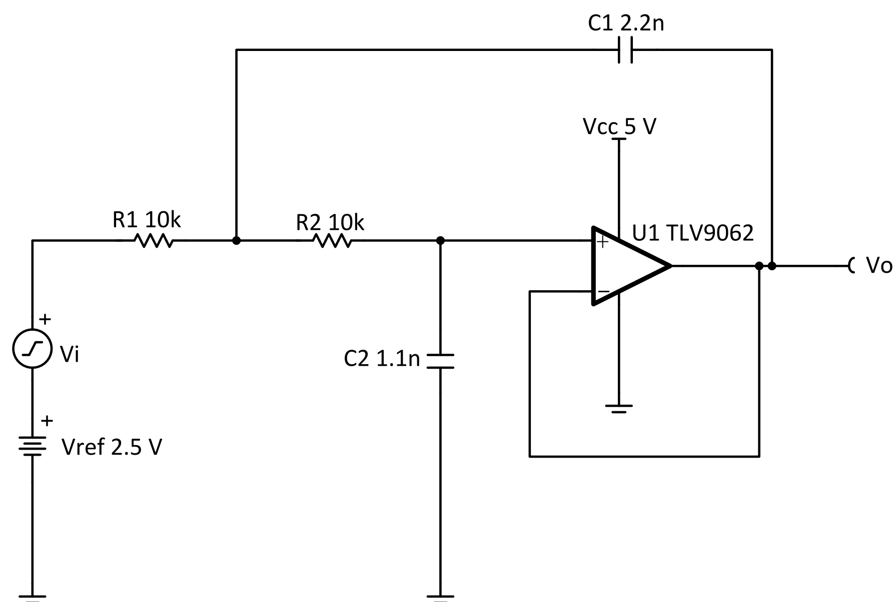
Amplifiers

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–2.45V	+2.45V	0.05V	4.95V	5V	0V

Gain	Cutoff Frequency (f_c)	V_{ref}
1V/V	10kHz	2.5V

Design Description

The Butterworth Sallen-Key low-pass filter is a second-order active filter. V_{ref} provides a DC offset to accommodate for single-supply applications. A Sallen-Key filter is usually preferred when small Q factor is desired, noise rejection is prioritized, and when a non-inverting gain of the filter stage is required. The Butterworth topology provides a maximally flat gain in the pass band.



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_c.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).

Design Steps

The first step is to find component values for the normalized cutoff frequency of 1 radian/second. In the second step the cutoff frequency is scaled to the desired cutoff frequency with scaled component values.

The transfer function for second order Sallen-Key low-pass filter is given by:

$$\mathrm{H}\ (\mathrm{s}) = \frac{\frac{1}{\mathrm{R_1 \times R_2 \times C_1 \times C_2}}}{\mathrm{s}^2 + \mathrm{s}\left(\frac{1}{\mathrm{R_1 \times C_1}} + \frac{1}{\mathrm{R_2 \times C_1}}\right) + \frac{1}{\mathrm{R_1 \times R_2 \times C_1 \times C_2}}}$$

$$\mathrm{H(s)} = \frac{\mathrm{a_0}}{\mathrm{s^2 + a_1 \times s + a_0}}$$

Here,

$$\mathrm{a_1} = \frac{1}{\mathrm{R_1 \times C_1}} + \frac{1}{\mathrm{R_2 \times C_1}},\ \mathrm{a_0} = \frac{1}{\mathrm{R_1 \times R_2 \times C_1 \times C_2}}$$

1. Set normalized values of R_1 and R_2 (R_{1n} and R_{2n}) and calculate normalized values of C_1 and C_2 (C_{1n} and C_{2n}) by setting w_c to 1 radian/sec (or f_c = 1 / (2 × π) Hz). For the second-order Butterworth filter, (see the *Butterworth Filter Table* in the *Active Low-Pass Filter Design Application Report*).

   $$\omega_c = 1\frac{\mathrm{radian}}{\mathrm{second}} \rightarrow \mathrm{a_0} = 1,\ \mathrm{a_1} = \sqrt{2},\ \text{let } \mathrm{R_{1n} = R_{2n}} = 1,\ \text{then } \mathrm{C_{1n} \times C_{2n}} = 1 \text{ or } \mathrm{C_{2n}} = \frac{1}{\mathrm{C_{1n}}},\ \mathrm{a_1} = \frac{2}{\mathrm{C_{1n}}} = \sqrt{2}$$

   $$\therefore \mathrm{C_{1n}} = \sqrt{2} = 1.414\ \mathrm{F},\ \mathrm{C_{2n}} = \frac{1}{\mathrm{C_{1n}}} = 0.707\ \mathrm{F}$$

2. Scale the component values and cutoff frequency. The resistor values are very small and capacitors values are unrealistic, hence these have to be scaled. The cutoff frequency is scaled from 1 radian/sec to w_0. If *m* is assumed to be the scaling factor, increase the resistors by *m* times, then the capacitor values have to decrease by 1/*m* times to keep the same cutoff frequency of 1 radian/sec. If the cutoff frequency is scaled to be w_0, then the capacitor values have to be decreased by 1 / w_o. The component values for the design goals are calculated in steps 3 and 4.

   $$R_1 = R_{1n} \times m,\ \ R_2 = R_{2n} \times m \tag{6}$$

   $$C_1 = \frac{\mathrm{C_{1n}}}{m \times \omega_0} = \frac{1.414}{m \times \omega_0}\mathrm{F} \tag{7}$$

   $$C_2 = \frac{\mathrm{C_{2n}}}{m \times \omega_0} = \frac{0.707}{m \times \omega_0}\mathrm{F} \tag{8}$$

3. Set R1 and R2 values:

   $$\mathrm{m} = 10000$$

   $$R_1 = (\mathrm{R_{1n}} \times m) = 10\mathrm{k\Omega} \tag{10}$$

   $$R_2 = (\mathrm{R_{2n}} \times m) = 10\mathrm{k\Omega} \tag{11}$$

4. Calculate C_1 and C_2 based on *m* and w_0.

   $$\text{Given } \omega_0 = 2 \times \pi \times f_c, \text{ where } f_c = 10\text{kHz and m} = 10000 = 10\text{ k}$$

   $$C_1 = \frac{1.414}{m \times \omega_0}\text{ F} = \frac{1.414}{10\text{ k} \times 2 \times \pi \times 10\text{kHz}} = 2.25\text{nF} \approx 2.2\text{nF (Standard Value)}$$

   $$C_2 = \frac{0.707}{m \times \omega_0}\text{ F} = \frac{0.707}{10\text{ k} \times 2 \times \pi \times 10\text{kHz}} = 1.125\text{nF} \approx 1.1\text{nF (Standard Value)}$$

5. Calculate the minimum required GBW and SR for f_c.

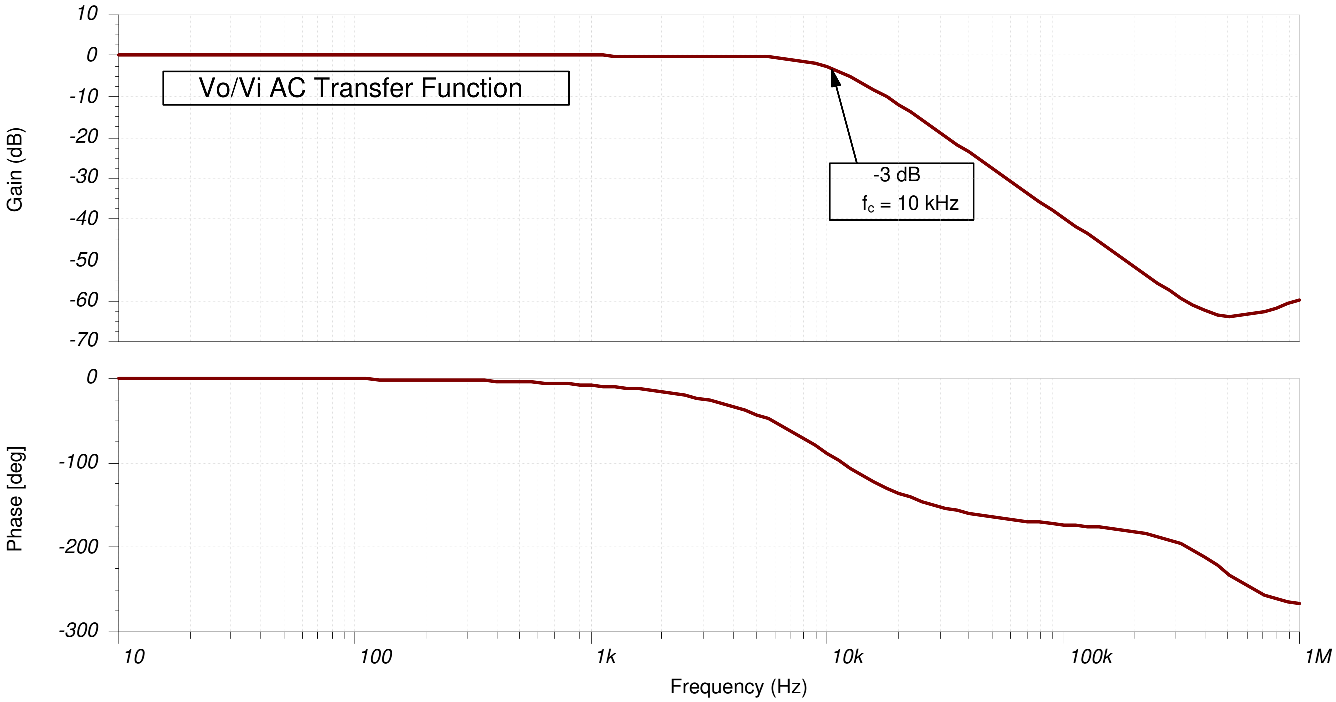
   $$\text{GBW} = 100 \times \text{Gain} \times f_c = 100 \times 1 \times 10\text{kHz} = 1\text{MHz}$$

   $$\text{SR} = 2 \times \pi \times f_c \times V_{ipeak} = 2 \times \pi \times 10\text{kHz} \times 2.45\text{V} = 0.154\frac{\text{V}}{\mu\text{s}}$$

   The TLV9062 device has a GBW of 10MHz and SR of 6.5V/µs, so the requirements are met.

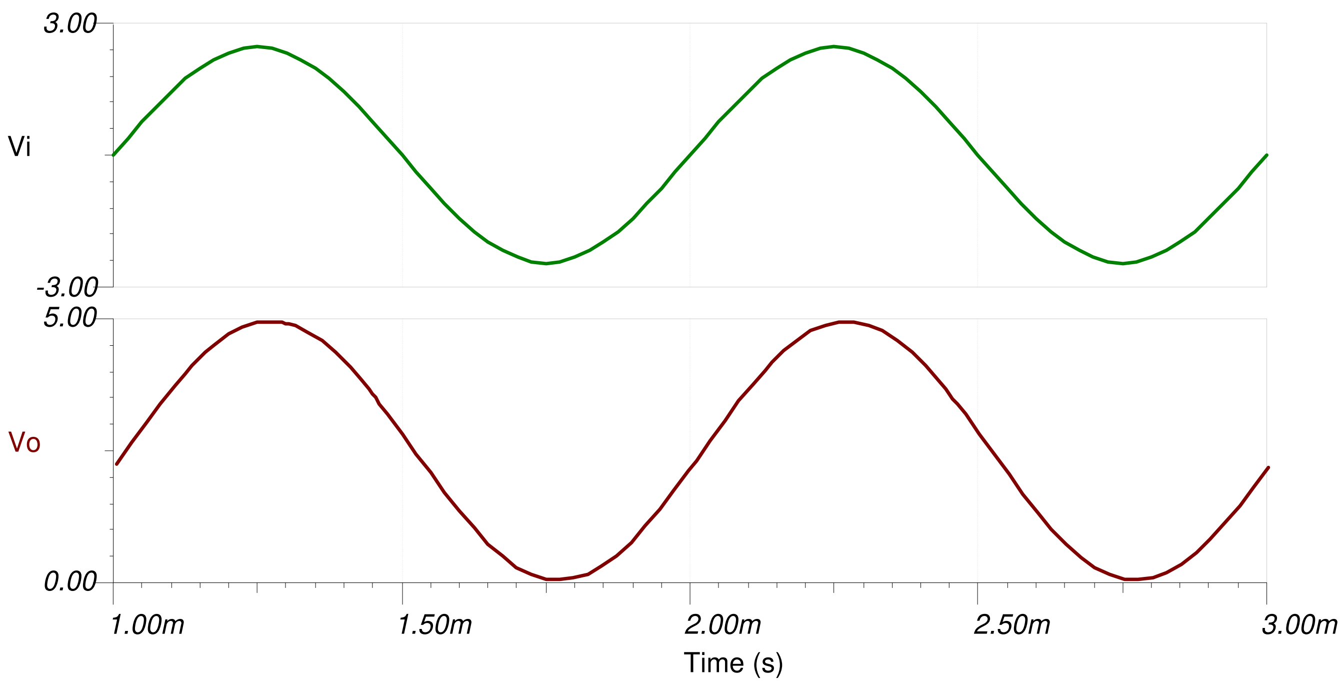
Design Simulations

AC Simulation Results

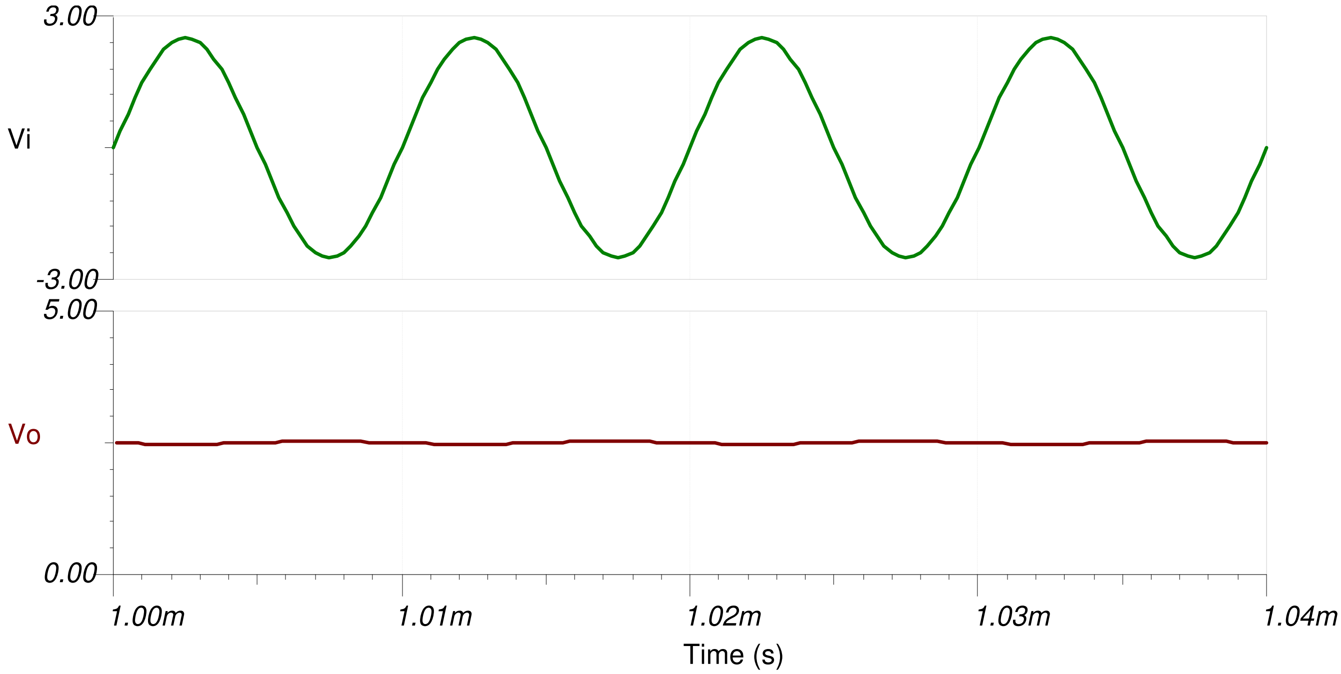


Transient Simulation Results

The following image shows the filter output in response to 5-Vpp, 1-kHz input signal (gain = 1V / V).



The following image shows the filter output in response to 5-Vpp, 100-kHz input signal (gain = 0.01 V/V).



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation File SBOC598.
3. TI Precision Labs.
4. *Active Low-Pass Filter Design Application Report*

Design Featured Op Amp

TLV9062	
Vss	1.8V to 5.5V
VinCM	Rail-to-Rail
Vout	Rail-to-Rail
Vos	0.3mV
Iq	538µA
Ib	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
Vss	1.8V to 5.5V	2.2V to 5.5V
VinCM	Rail-to-Rail	Rail-to-Rail
Vout	Rail-to-Rail	Rail-to-Rail
Vos	0.75mV	0.150mV
Iq	400µA	650µA
Ib	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Analog Engineer's Circuit Amplifiers

Low-Pass, Filtered, Inverting Amplifier Circuit

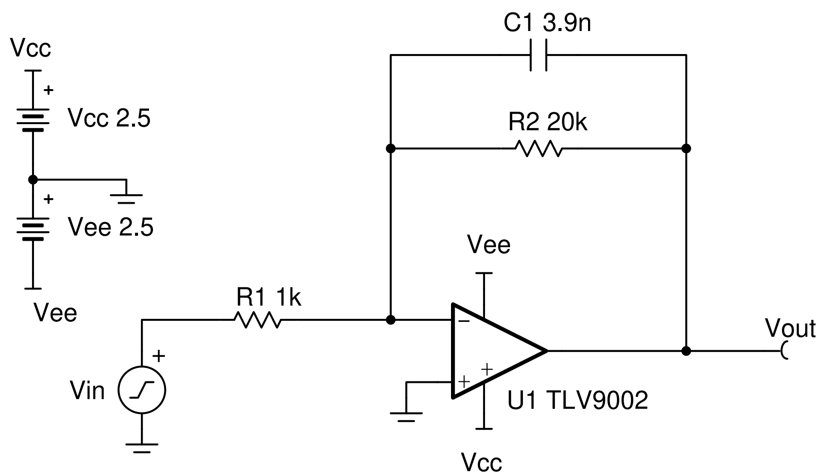
TEXAS INSTRUMENTS

Design Goals

Input		Output		BW	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{ee}	V_{cc}
–0.1V	0.1V	–2V	2V	2kHz	–2.5V	2.5V

Design Description

This tunable low–pass inverting amplifier circuit amplifies the signal level by 26dB or 20V/V. R_2 and C_1 set the cutoff frequency for this circuit. The frequency response of this circuit is the same as that of a passive RC filter, except that the output is amplified by the pass–band gain of the amplifier. Low–pass filters are often used in audio signal chains and are sometimes called bass–boost filters.



Design Notes

1. C_1 and R_2 set the low–pass filter cutoff frequency.
2. The common-mode voltage is set by the non–inverting input of the op amp, which in this case is mid–supply.
3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. R_2 and R_1 set the gain of the circuit.
5. The pole frequency f_p of 2kHz is selected for an audio bass–boost application.
6. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
7. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew–induced distortion.
8. For more information on op amp linear operation region, stability, slew–induced distortion, capacitive load drive, driving ADCs and bandwidth please see the design references section.

Design Steps

The DC transfer function of this circuit is given below.

$$V_o = V_i \times \left(-\frac{R_2}{R_1}\right)$$

1. Pick resistor values for given passband gain.

$$Gain = \frac{R_2}{R_1} = 20\ \frac{V}{V}\ (26\ dB)$$

$$R_1 = 1\ k\Omega$$

$$R_2 = Gain \times (R_1) = 20\frac{V}{V} \times 1\ k\Omega = 20\ k\Omega$$

2. Select low–pass filter pole frequency f_p

$$f_p = 2\ kHz$$

3. Calculate C_1 using R_2 to set the location of f_p.

$$f_p = \frac{1}{2 \times \pi \times R_2 \times C_1} = 2\ kHz$$

$$C_1 = \frac{1}{2 \times \pi \times R_2 \times f_p} = \frac{1}{2 \times \pi \times 20\ k\Omega\ \times 2\ kHz} = 3.98\ nF \approx 3.9\ nF\ (Standard\ Value)$$

4. Calculate the minimum slew rate required to minimize slew–induced distortion.

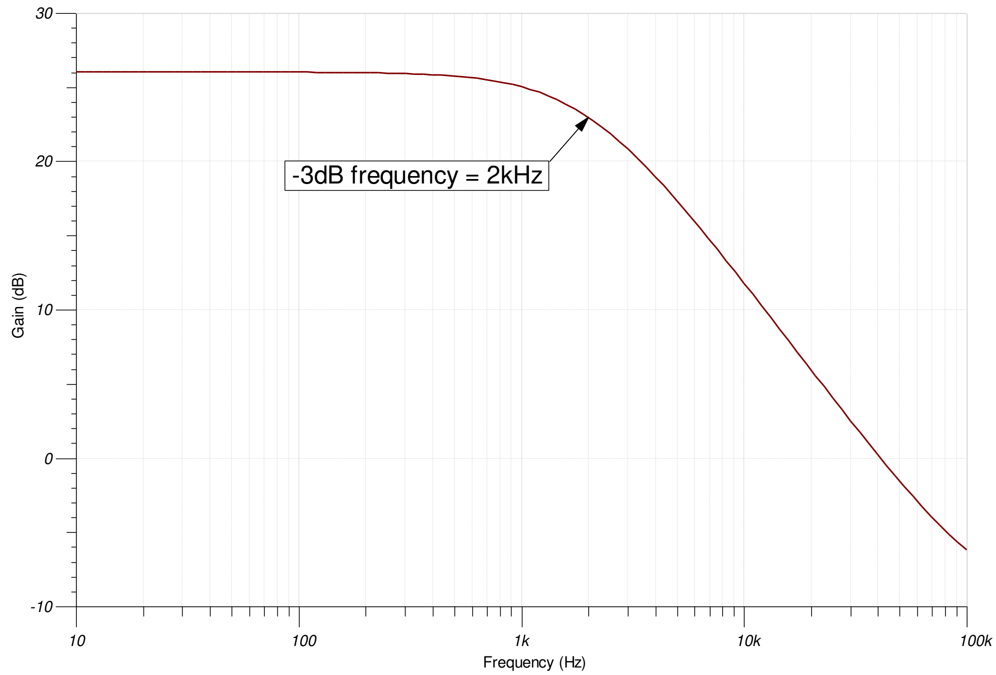
$$V_p = \frac{SR}{2 \times \pi \times f_p} \rightarrow SR > 2 \times \pi \times f_p \times V_p$$

$$SR > 2 \times \pi \times 2\ kHz \times 2\ V = 0.025\ \frac{V}{\mu s}$$

5. $SR_{TLV9002}$ = 2V/µs, therefore it meets this requirement

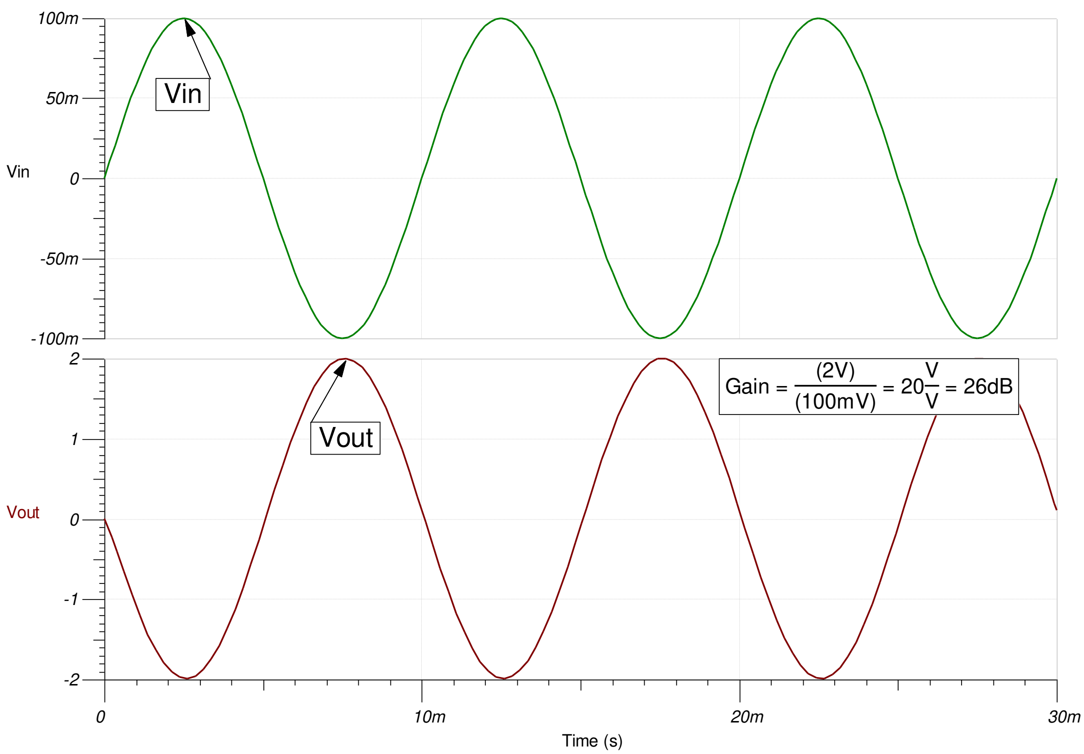
Design Simulations

AC Simulation Results

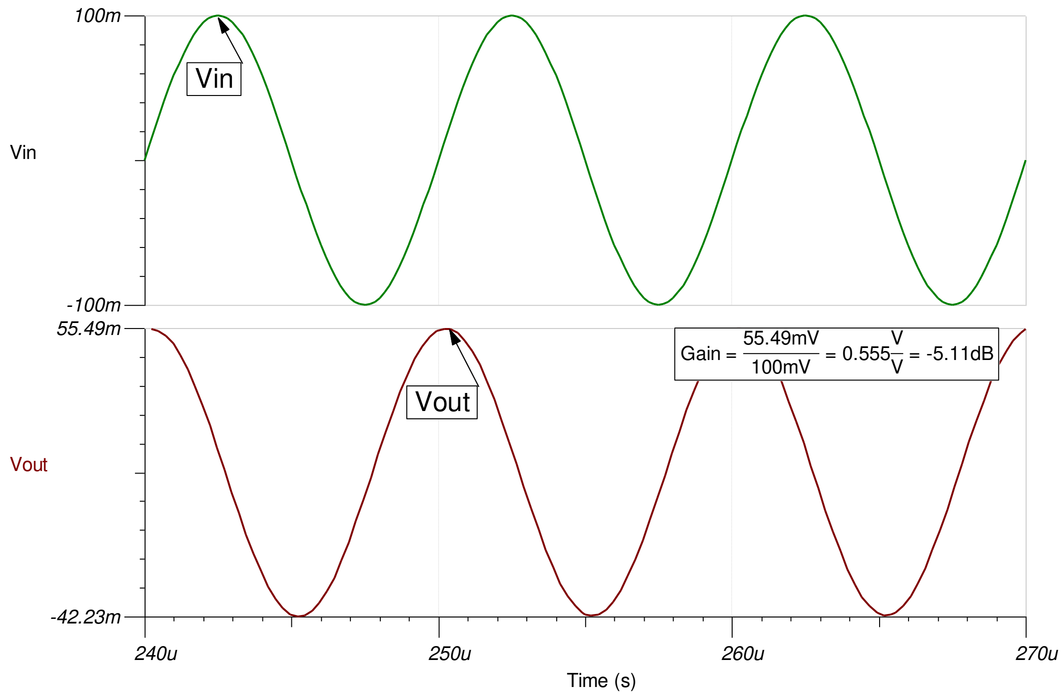


Transient Simulation Results

A 100 Hz, 0.2 V_{pp} sine wave yields a 4 V_{pp} output sine wave.



A 100 kHz, 0.2 V_{pp} sine wave yields a 0.1 V_{pp} output sine wave.



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOC523
3. TI Precision Designs TIPD185
4. TI Precision Labs

Design Featured Op Amp

TLV9002	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	0.4mV
I_q	60µA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1,2,4
www.ti.com/product/tlv9002	

Design Alternate Op Amp

OPA375	
V_{ss}	2.25V to 5.5V
V_{inCM}	V_{ee} to V_{cc} –1.2V
V_{out}	Rail–to–rail
V_{os}	0.15mV
I_q	890µA
I_b	10pA
UGBW	10MHz
SR	4.75V/µs
#Channels	1
www.ti.com/product/opa375	

Revision History

Revision	Date	Change
A	January 2021	Updated result in Design Step 4 from 0.25 to 0.025

Analog Engineer's Circuit

Single-supply, 2nd-order, Sallen-Key band-pass filter circuit

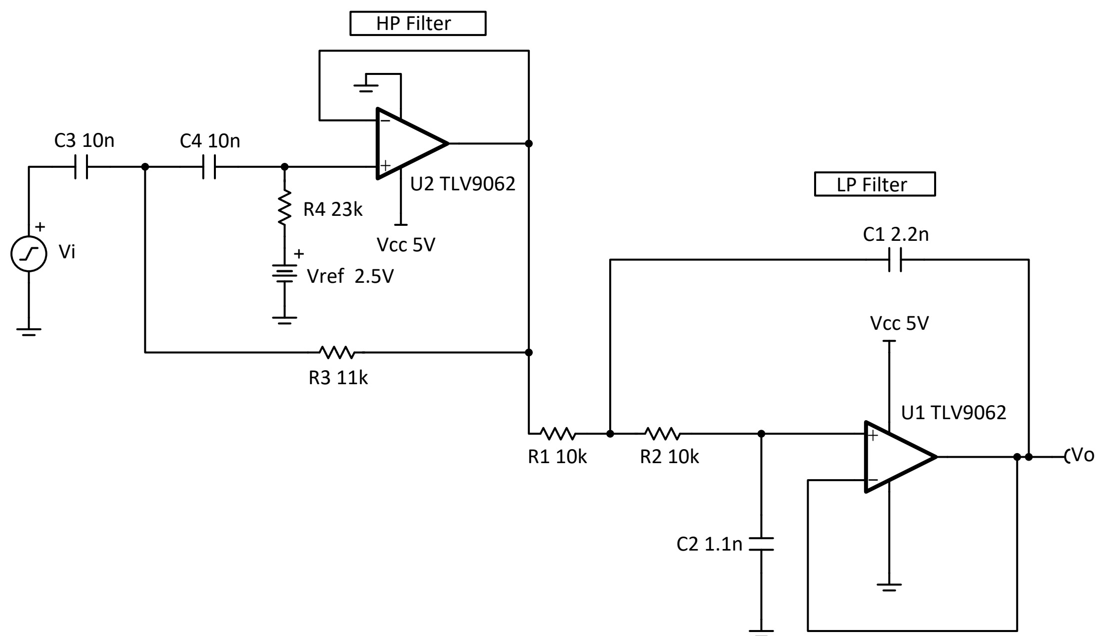
Amplifiers

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–2.45V	+2.45V	0.05V	4.95V	5V	0V

Gain	Low Cutoff Frequency (f_l)	High Cutoff Frequency (f_h)	V_{ref}
1V/V	1kHz	10kHz	2.5V

Design Description

This circuit is a single-supply, 2nd-order Sallen-Key (SK) band-pass (BP) filter. It is designed by cascading an SK low-pass filter and an SK high-pass filter. Vref provides a DC offset to accommodate for a single supply.



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_l and f_h.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).
5. For HP filters, the maximum frequency is set by the gain bandwidth (GBW) of the op amp. Therefore, be sure to select an op amp with sufficient GBW.

Design Steps

This BP filter design involves two cascaded filters, a low-pass (LP) filter and a high-pass (HP) filter. The lower cutoff frequency (f_l) of the BP filter is 1kHz and the higher cutoff frequency (f_h) is 10kHz. The design steps show an LP filter design with f_h of 10kHz and an HP filter design with f_l of 1kHz. See the SK LP filter design and SK HP filter design in the circuit cookbook for details on transfer function equations and calculations.

LP Filter Design

1. Use SK low-pass filter design to determine R_1 and R_2.

$$R_1 = 10\text{k}\Omega,$$
$$R_2 = 10\text{k}\Omega$$

2. Use SK low-pass filter design to determine C_1 and C_2.

$$C_1 = 2.2\text{nF} \;\; (\text{Standard Value}),$$
$$C_2 = 1.1\text{nF} \;\; (\text{Standard Value})$$

HP Filter Design

1. Use SK high-pass filter design to determine C_3 and C_4.

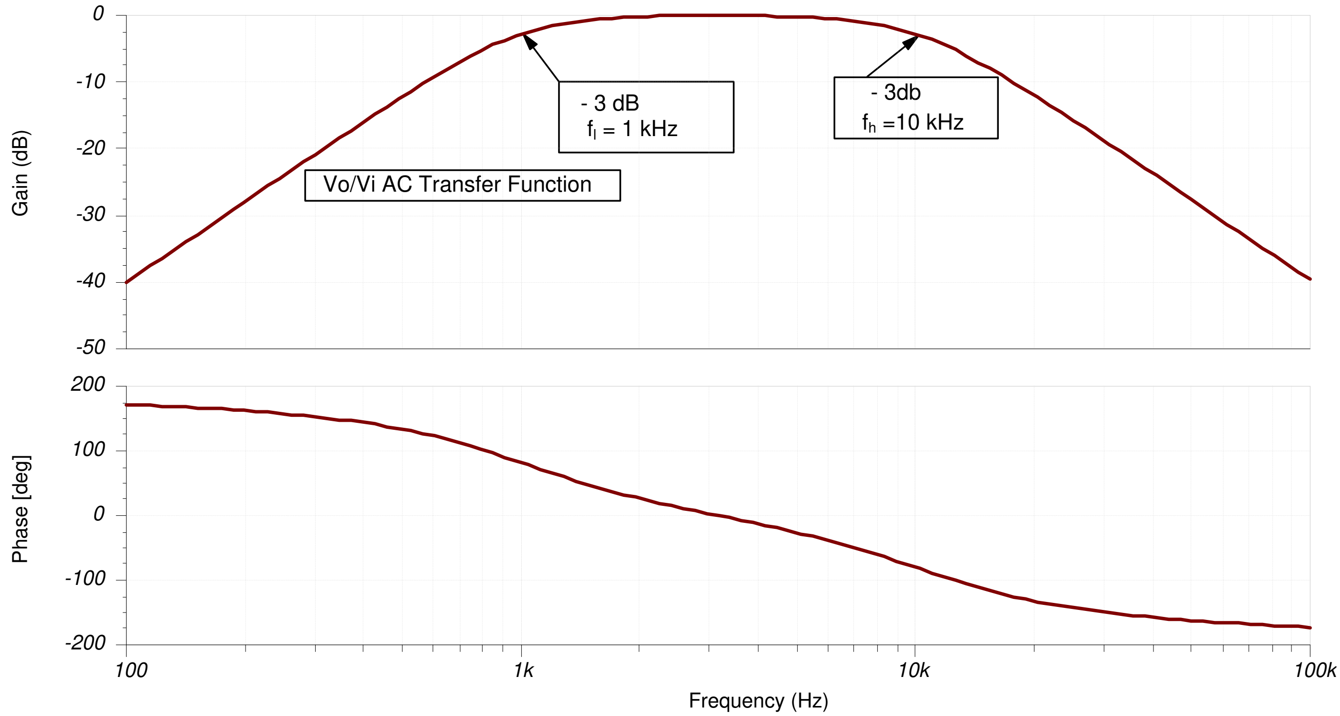
$$C_3 = 10\text{nF},$$
$$C_4 = 10\text{nF}$$

2. Use SK high-pass filter design to determine R_3 and R_4.

$$R_3 = 11\text{k}\Omega,$$
$$R_4 = 23\text{k}\Omega$$

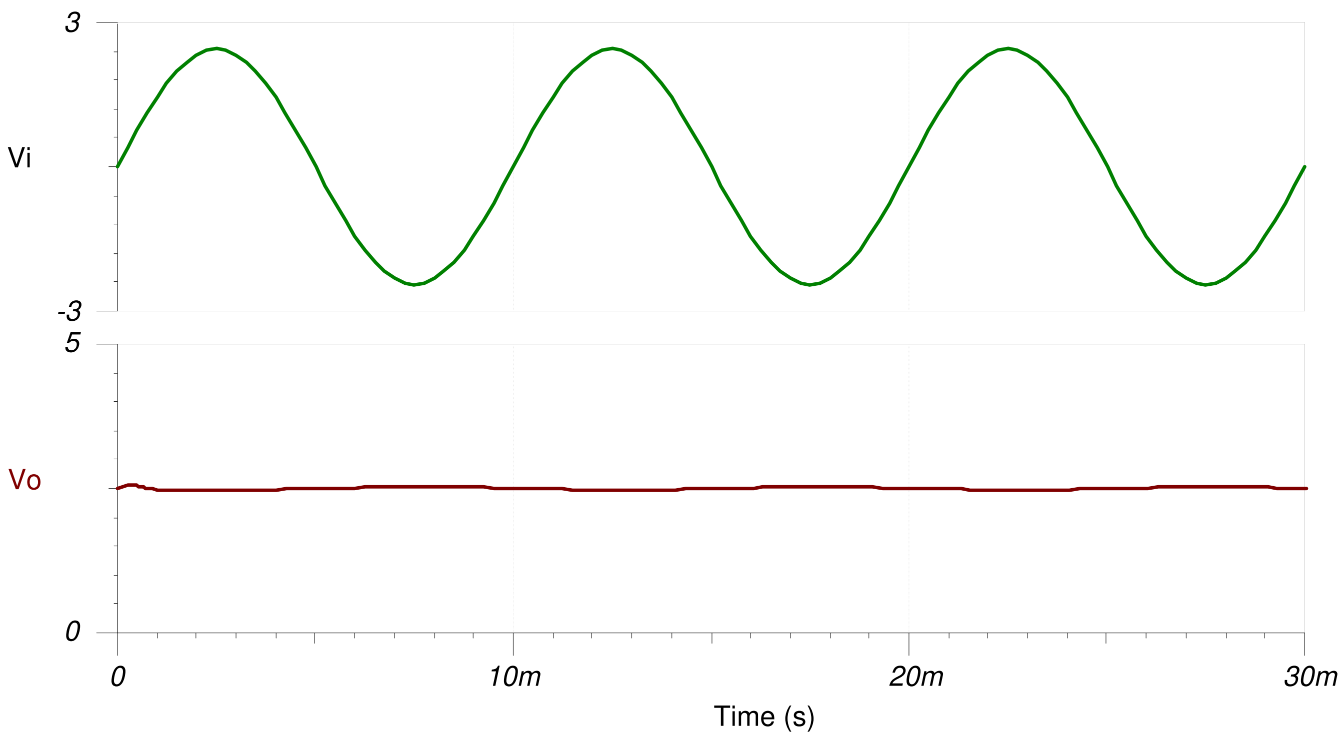
Design Simulations

AC Simulation Results

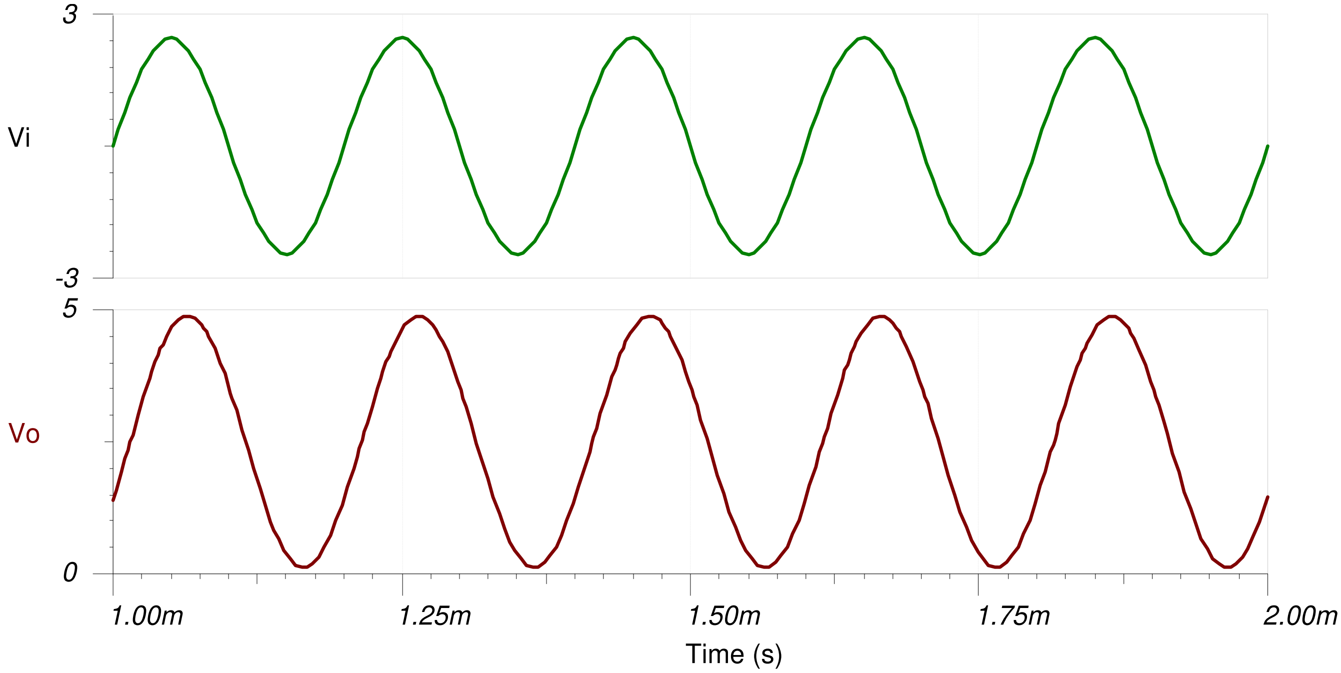


Transient Simulation Results

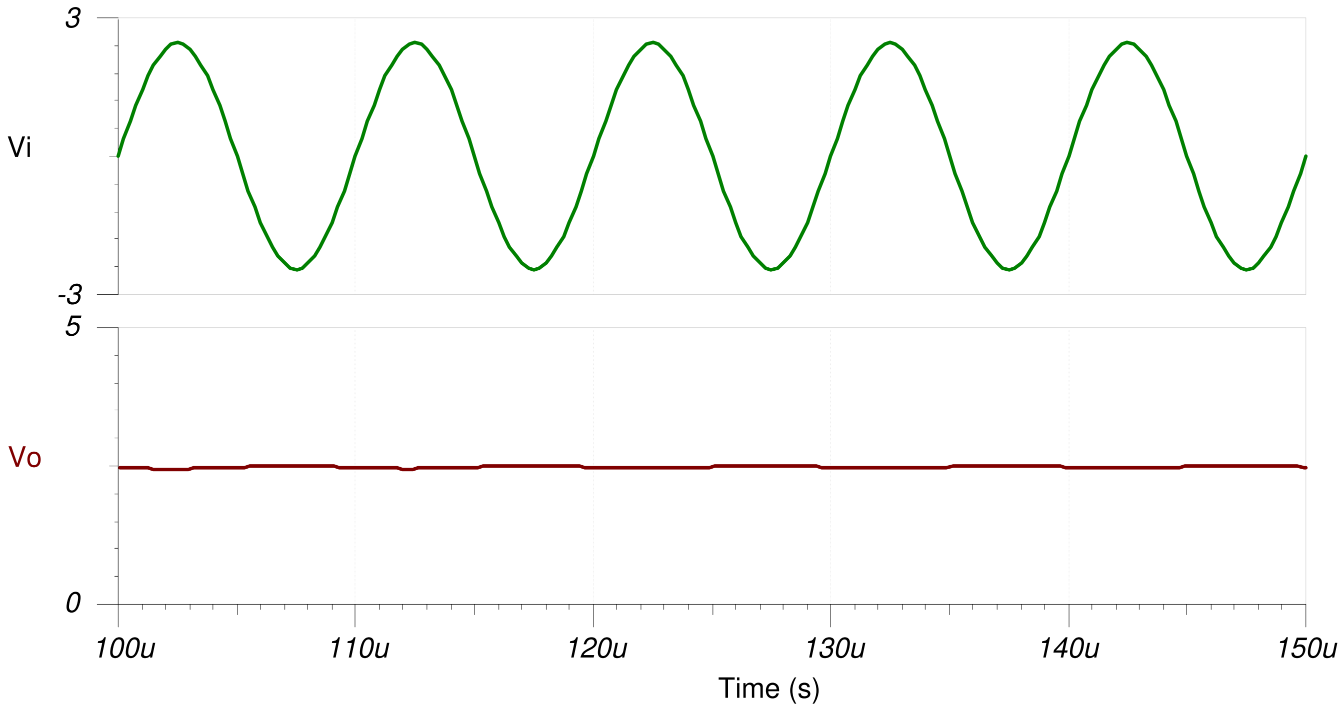
The following image shows a filter output in response to a 5-V_{pp}, 100-Hz input signal (gain = 0.01 V/V).



The following transient simulation result shows a filter output in response to a 5-V_{pp}, 5-kHz input signal (gain = 1V/V).



The following image shows a filter output in response to a 5-V_{pp}, 100-kHz input signal (gain = 0.01V/V).



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. TI Precision Labs.

Design Featured Op Amp

TLV9062	
Vss	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
Vout	Rail-to-Rail
Vos	0.3mV
Iq	538µA
Ib	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
Vout	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
Iq	400µA	650µA
Ib	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Analog Engineer's Circuit

AC Coupled (HPF) Non-Inverting Amplifier Circuit

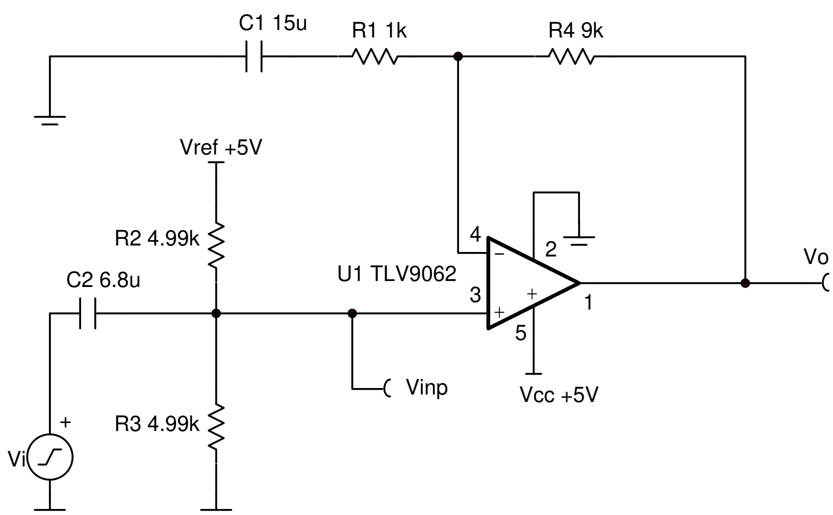
Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–240 mV	240 mV	0.1 V	4.9 V	5 V	0 V	5 V

Lower Cutoff Freq. (f_L)	Upper Cutoff Freq. (f_H)	AC Gain (G_{ac})
16 Hz	≥ 1 MHz	10 V/V

Design Description

This circuit amplifies an AC signal, and shifts the output signal so that it is centered at one-half the power supply voltage. Note that the input signal has zero DC offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.



Design Notes

1. The voltage at V_{inp} sets the input common-mode voltage.
2. R_2 and R_3 load the input signal for AC frequencies.
3. Use low feedback resistance for low noise.
4. Set the output range based on linear output swing (see A_{ol} specification of op amp).
5. The circuit has two real poles that determine the high-pass filter –3 dB frequency. Set them both to $f_L/1.557$ to achieve –3 dB at the lower cutoff frequency (f_L).

Design Steps

1. Select R_1 and R_4 to set the AC voltage gain.

$$R_1 = 1 \quad k\Omega \text{ (Standard Value)}$$

$$R_4 = R_1 \times (G_{ac} - 1) = 1 \quad k\Omega \times \left(10\frac{V}{V} - 1\right) = 9k\Omega \text{ (Standard Value)}$$

2. Select R_2 and R_3 to set the DC output voltage (V_{DC}) to 2.5 V, or mid–supply.

$$R_3 = 4.99k\Omega \text{ (Standard Value)}$$

$$R_2 = \frac{R_3 \times V_{ref}}{V_{DC}} - R_3 = \frac{4.99k\Omega \times 5V}{2.5V} - 4.99k\Omega = 4.99k\Omega$$

3. Select C_1 based on f_L and R_1.

$$f_L = 16Hz$$

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times \left(\frac{f_L}{1.557}\right)} = \frac{1}{2 \times \pi \times 1 \quad k\Omega \times 10.3Hz} = 15.5\mu F \approx 15\mu F \text{ (Standard Value)}$$

4. Select C_2 based on f_L, R_2, and R_3.

$$R_{div} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{4.99k\Omega \times 4.99k\Omega}{4.99k\Omega + 4.99k\Omega} = 2.495k\Omega$$

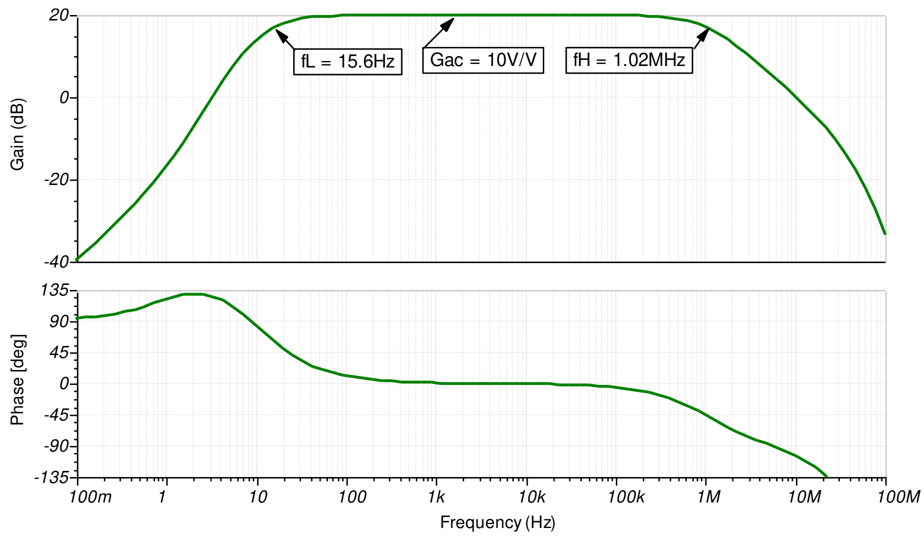
$$C_2 = \frac{1}{2 \times \pi \times R_{div} \times \left(\frac{f_L}{1.557}\right)} = \frac{1}{2 \times \pi \times 2.495k\Omega \times 10.3Hz} = 6.4\mu F \rightarrow 6.8\mu F\left(\text{StandardValue}\right)$$

5. The upper cutoff frequency (f_H) is set by the non-inverting gain of this circuit and the gain bandwidth (GBW) of the device (TLV9062).

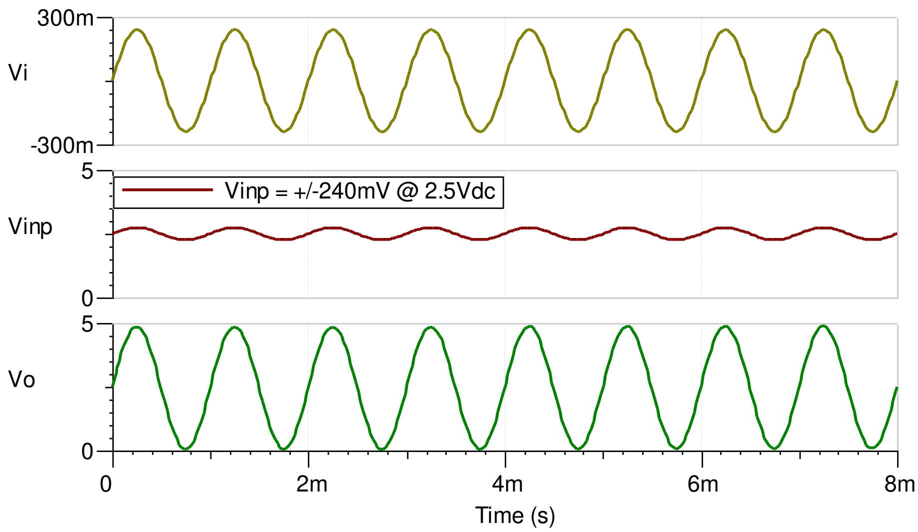
$$f_H = \frac{\text{GBW of TLV9062}}{G_{ac}} = \frac{10MHz}{10\frac{V}{V}} = 1 \quad MHz$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC505.

See TIPD185.

Design Featured Op Amp

TLV9062	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	300 µV
I_q	538 µA
I_b	0.5 pA
UGBW	10 MHz
SR	6.5 V/µs
#Channels	1, 2, and 4
TLV9062	

Design Alternate Op Amp

OPA192	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	1 mA/Ch
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA192	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 2, 2017 to February 1, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page............	1

Analog Engineer's Circuit

Single-supply, 2nd-order, Sallen-Key high-pass filter circuit

Amplifiers

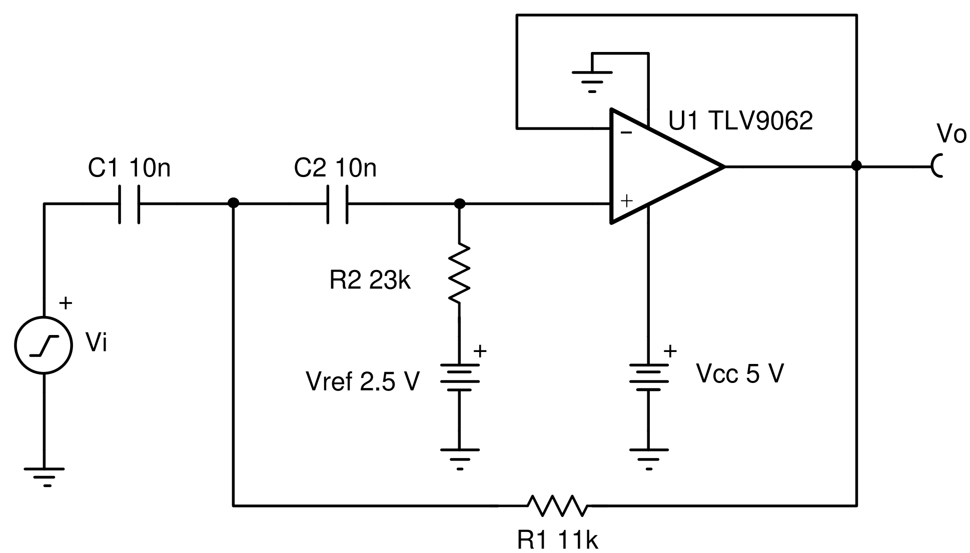
Input		**Output**		**Supply**	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–2.45V	+2.45V	0.05V	4.95V	5V	0V

Gain	**Cutoff Frequency (f_c)**	**Max Frequency (f_{max})**	**V_{ref}**
1V/V	1kHz	10kHz	2.5V

Design Description

The Butterworth Sallen-Key (SK) high-pass (HP) filter is a 2nd-order active filter. Vref provides a DC offset to accommodate for single-supply applications.

An SK filter is usually preferred when small Q factor is desired, noise rejection is prioritized, and when a non-inverting gain of the filter stage is required. The Butterworth topology provides a maximally flat gain in the pass band.



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_c.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).
5. For HP filters, the maximum frequency is set by the gain bandwidth (GBW) of the op amp. Therefore, be sure to select an op amp with sufficient GBW.

Design Steps

The first step is to find component values for the normalized cutoff frequency of 1 radian/second. In the second step the cutoff frequency is scaled to the desired cutoff frequency with scaled component values.

The transfer function for the second-order Sallen-Key high-pass filter is given by:

$$H(s) = \frac{s^2}{s^2 + s\left(\frac{1}{R_2 \times C_1} + \frac{1}{R_2 \times C_2}\right) + \frac{1}{R_1 \times R_2 \times C_1 \times C_2}}$$

$$H(s) = \frac{s^2}{s^2 + a_1 \times s + a_0}$$

where,

$$a_1 = \frac{1}{R_2 \times C_1} + \frac{1}{R_2 \times C_2},\ a_0 = \frac{1}{R_1 \times R_2 \times C_1 \times C_2}$$

1. Set normalized values of C_1 and C_2 (C_{1n} and C_{2n}) and calculate normalized values of R_1 and R_2 (R_{1n} and R_{2n}) by setting w_c to 1 radian/sec (or fc = 1 / (2 × π) Hz). For the second-order Butterworth filter, (see the *Butterworth Filter Table* in the *Active Low-Pass Filter Design Application Report*).

   $$a_0 = 1,\ a_1 = \sqrt{2},\ \text{let } C_{1n} = C_{2n} = 1\text{ F, then } R_{1n} \times R_{2n} = 1 \text{ or } R_{2n} = \frac{1}{R_{1n}},\ \ a_1 = \frac{2}{R_{2n}} = \sqrt{2}$$

   $$\therefore R_{2n} = \sqrt{2} = 1.414\Omega\ ,\ R_{1n} = \frac{1}{R_{2n}} = 0.707\Omega$$

2. Scale the component values and cutoff frequency. The resistor values are very small and capacitors values are unrealistic, hence these have to be scaled. The cutoff frequency is scaled from 1 radian/sec to w_0. If *m* is assumed to be the scaling factor, increase the resistors by *m* times, then the capacitor values have to decrease by 1/*m* times to keep the same cutoff frequency of 1 radian/sec. If the cutoff frequency is scaled to be w_0, then the capacitor values have to be decreased by 1 / w_0. The component values for the design goals are calculated in steps 3 and 4.

   $$R_1 = R_{1n} \times m,\ R_2 = R_{2n} \times m$$

   $$C_1 = C_2 = \frac{C_{1n}}{m \times w_0}\text{F}$$

3. Set C_1 and C_2 to 10nF, then calculate *m*.

   $$w_0 = 2 \times \pi \times 1\text{kHz},\ m = 15915.5$$

4. Select R_1 and R_2 based on *m*.

   $$R_1 = 0.707 \times 15915 = 11252\Omega \approx 11\text{k}\Omega\ (\text{Standard Value})$$

   $$R_2 = 1.414 \times 15915 = 22504\Omega \approx 23\text{k}\Omega\ (\text{Standard Value})$$

5. Calculate the minimum required GBW and SR for f_{max}.

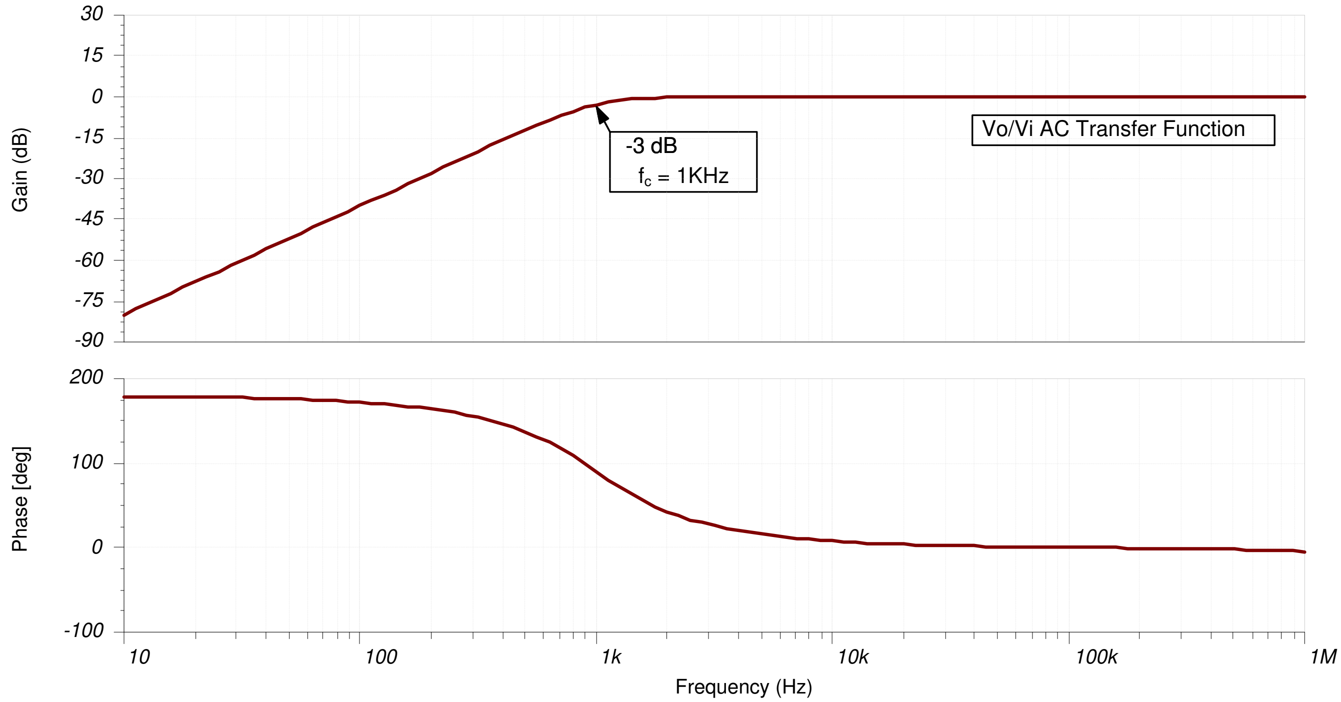
   $$\text{GBW} = 100 \times \text{Gain} \times f_{max} = 100 \times 1 \times 10\text{kHz} = 1\text{MHz}$$

   $$\text{SR} = 2 \times \pi \times f_{max} \times V_{ipeak} = 2 \times \pi \times 10\text{kHz} \times 2.45\text{V} = 0.154\frac{\text{V}}{\mu\text{s}}$$

   The TLV9062 device has a GBW of 10MHz and SR of 6.5V/µs, so it meets these requirements.

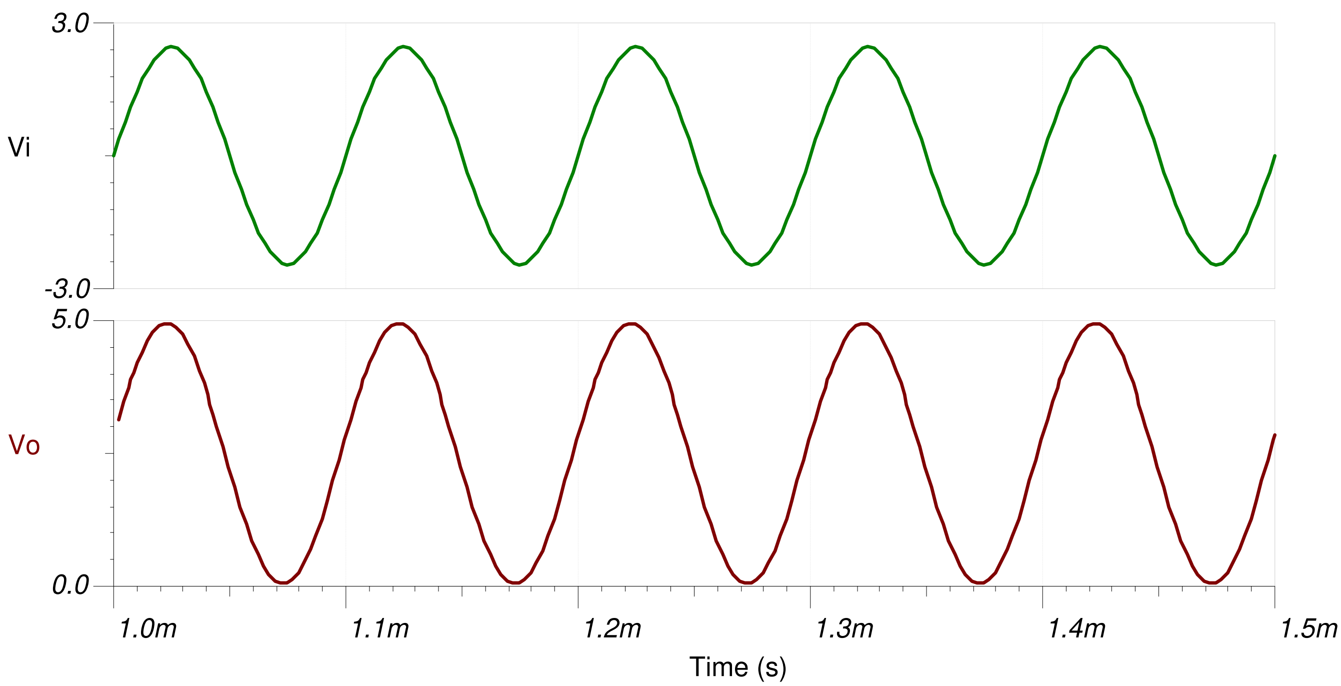
Design Simulations

AC Simulation Results

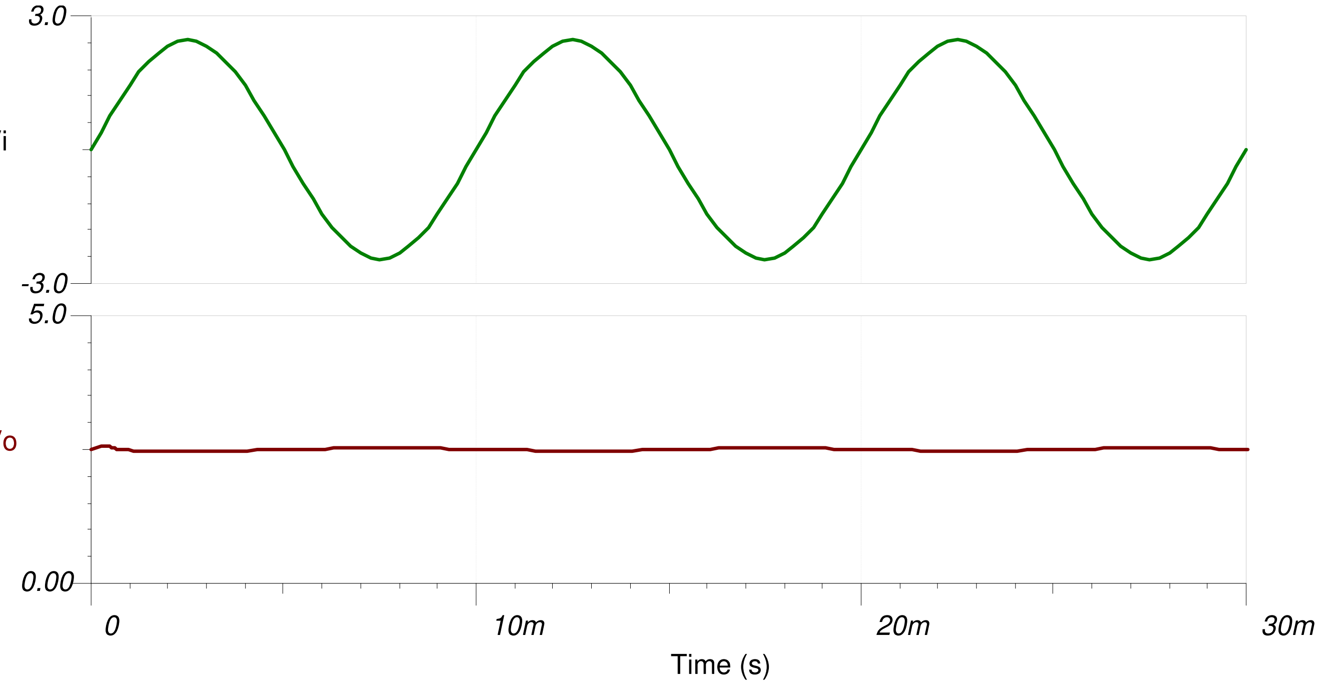


Transient Simulation Results

The following image shows the filter output in response to a ± 2.5-V, 10-kHz input signal (gain is 1V / V).



The following image shows the filter output in response to a ± 2.5-V, 10-Hz input signal (gain is 0.014V / V).



Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation File - SBOMB38.
3. TI Precision Labs

Design Featured Op Amp

TLV9062	
Vss	1.8V to 5.5V
VinCM	Rail-to-Rail
Vout	Rail-to-Rail
Vos	0.3mV
Iq	538µA
Ib	0.5pA
UGBW	10MHz
SR	6.5V / µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
Vss	1.8V to 5.5V	2.2V to 5.5V
VinCM	Rail-to-Rail	Rail-to-Rail
Vout	Rail-to-Rail	Rail-to-Rail
Vos	0.75mV	0.150mV
Iq	400µA	650µA
Ib	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V / µs	5V / µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/OPA316	www.ti.com/product/OPA325

Analog Engineer's Circuit

Single-supply, 2nd-order, multiple feedback high-pass filter circuit

TEXAS INSTRUMENTS

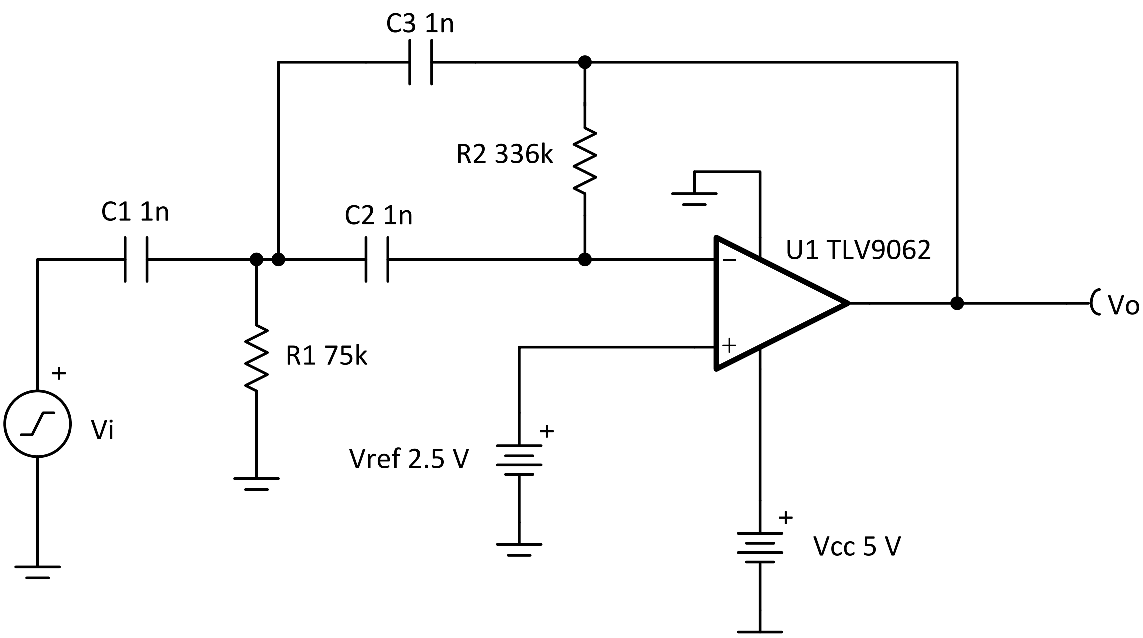
Amplifiers

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–2.45V	+2.45V	0.05V	4.95V	5V	0V

Gain	Cutoff Frequency (f_c)	Max Frequency (f_{max})	V_{ref}
–1V/V	1kHz	10kHz	2.5V

Design Description

The multiple-feedback (MFB) high-pass (HP) filter is a 2nd-order active filter. V_{ref} provides a DC offset to accommodate for single-supply applications. This HP filter inverts the signal (Gain = –1V/V) for frequencies in the pass band. An MFB filter is preferable when the gain is high or when the Q-factor is large (for example, 3 or greater).



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_c.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).
5. For HP filters, the maximum frequency is set by the gain bandwidth (GBW) of the op amp. Therefore, be sure to select an op amp with sufficient GBW.

Design Steps

The first step in design is to find component values for the normalized cutoff frequency of 1 radian/second. In the second step, the cutoff frequency is scaled to the desired cutoff frequency with scaled component values.

The transfer function for a 2nd-order MFB high pass filter is given by:

$$H(s) = \frac{-s^2\frac{C_1}{C_3}}{s^2 + s\frac{C_1 + C_2 + C_3}{R_2 \times C_2 \times C_3} + \frac{1}{R_1 \times R_2 \times C_2 \times C_3}}$$

$$H(s) = \frac{-s^2\frac{C_1}{C_3}}{s^2 + a_1 \times s + a_0}$$

$$\text{Here,}\ \ a_1 = \frac{C_1 + C_2 + C_3}{R_2 \times C_2 \times C_3},\ \ a_0 = \frac{1}{R_1 \times R_2 \times C_2 \times C_3} \tag{3}$$

1. Set normalized values of C_1, C_2, and C_3 (C_{1n}, C_{2n}, and C_{3n}) and calculate normalized values of R_1 and R_2 (R_{1n} and R_{2n}) by setting w_c to 1radian/sec (or f_c = 1 / (2 × π)Hz). For a 2nd-order Butterworth filter, (see the *Butterworth Filter Table* in the *Active Low-Pass Filter Design Application Report*).

   $$\omega_c = 1\frac{\text{radian}}{\text{second}} \rightarrow a_0 = 1, a_1 = \sqrt{2}, \text{let } C_{1n} = C_{2n} = C_{3n} = 1\text{ F}$$

   $$\text{Then } R_{1n} \times R_{2n} = 1 \text{ or } R_{2n} = \frac{1}{R_{1n}},\ a_1 = \frac{3}{R_{2n}} = \sqrt{2}$$

   $$\therefore R_{2n} = 2.1213,\ \ R_{1n} = \frac{1}{R_{2n}} = 0.4714$$

2. Scale the component values and cutoff frequency. The resistor values are very small and capacitors values are unrealistic, hence these have to be scaled. The cutoff frequency is scaled from 1 radian/sec to w_0. If we assume *m* to be the scaling factor, increase the resistors by *m* times, then the capacitor values have to decrease by 1/*m* times to keep the same cutoff frequency of 1 radian/sec. If we scale the cutoff frequency to be w_0 then the capacitor values have to be decreased by $1/w_0$. The component values for the design goals are calculated in step 3 and 4.

   $$R_1 = R_{1n} \times m = (0.4714 \times m),\ \ R_2 = R_{2n} \times m = (2.1213 \times m)$$

   $$C_1 = \frac{C_{1n}}{m \times \omega_0} = \frac{1}{m \times \omega_0}\text{F}$$

   $$C_2 = \frac{C_{2n}}{m \times \omega_0} = \frac{1}{m \times \omega_0}\text{F}$$

   $$C_3 = \frac{C_{3n}}{m \times \omega_0} = \frac{1}{m \times \omega_0}\text{F}$$

3. Set C_1, C_2, and C_3 to 1nF and calculate m.

   Given $\omega_0 = 2 \times \pi \times f_c$, where $f_c = 1\text{kHz}$,

   $$C_1 = C_2 = C_3 = \frac{1}{m \times \omega_0}\,\text{F} = \frac{1}{m \times 2 \times \pi \times 1\text{kHz}}$$

   So, $m = 159155$

4. Calculate R_1 and R_2 based on *m*.

   $$R_1 = R_{1n} \times m = 0.4714 \times 159155 \approx 75\text{k}\Omega \text{ (Standard Value)}$$

   $$R_2 = R_{2n} \times m = 2.1213 \times 159155 \approx 336\text{k}\Omega \text{ (Standard Value)}$$

5. Calculate minimum required GBW and SR for f_{max}. Be sure to use the noise gain for GBW calculations. Do not use the signal gain of –1V/V.

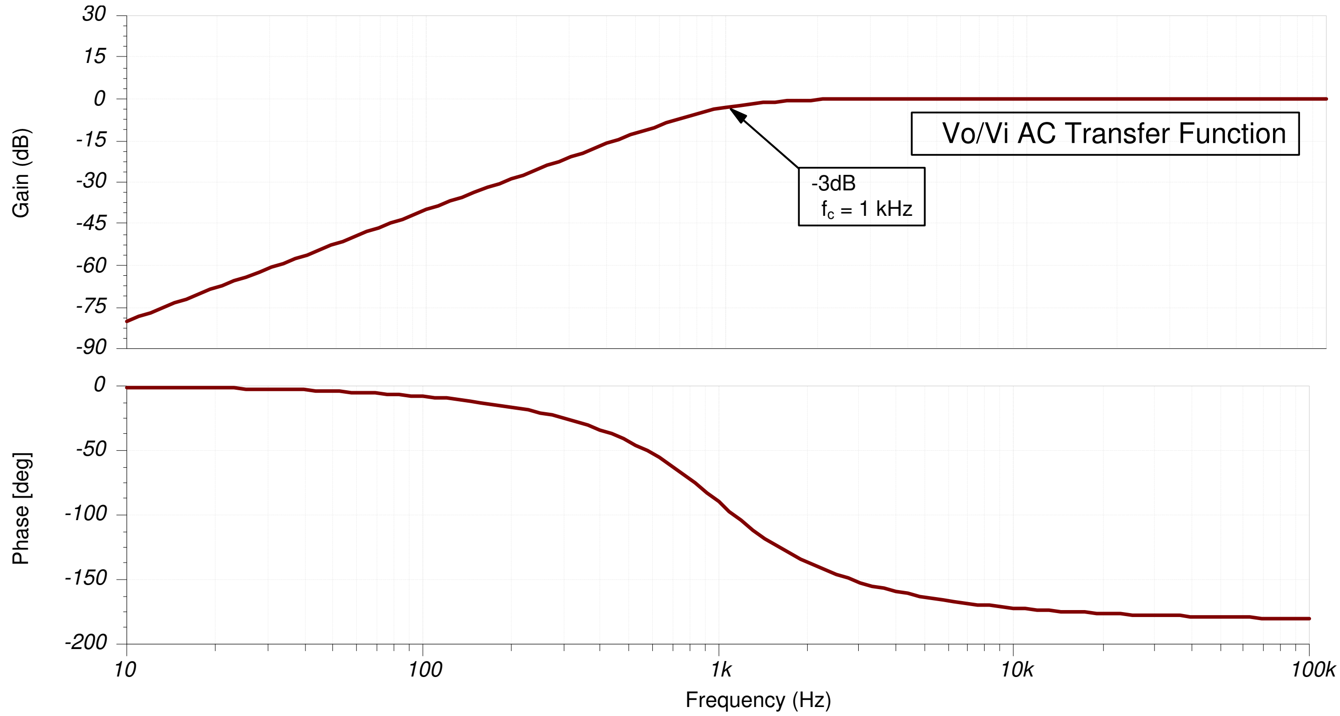
   $$\text{GBW} = 100 \times \text{Noise Gain} \times f_{max} = 100 \times 2 \times 10\text{kHz} = 2\text{MHz}$$

   $$\text{SR} = 2 \times \pi \times f_{max} \times V_{iMax} = 2 \times \pi \times 10\text{kHz} \times 2.45\text{V} = 0.154\frac{\text{V}}{\mu\text{s}}$$

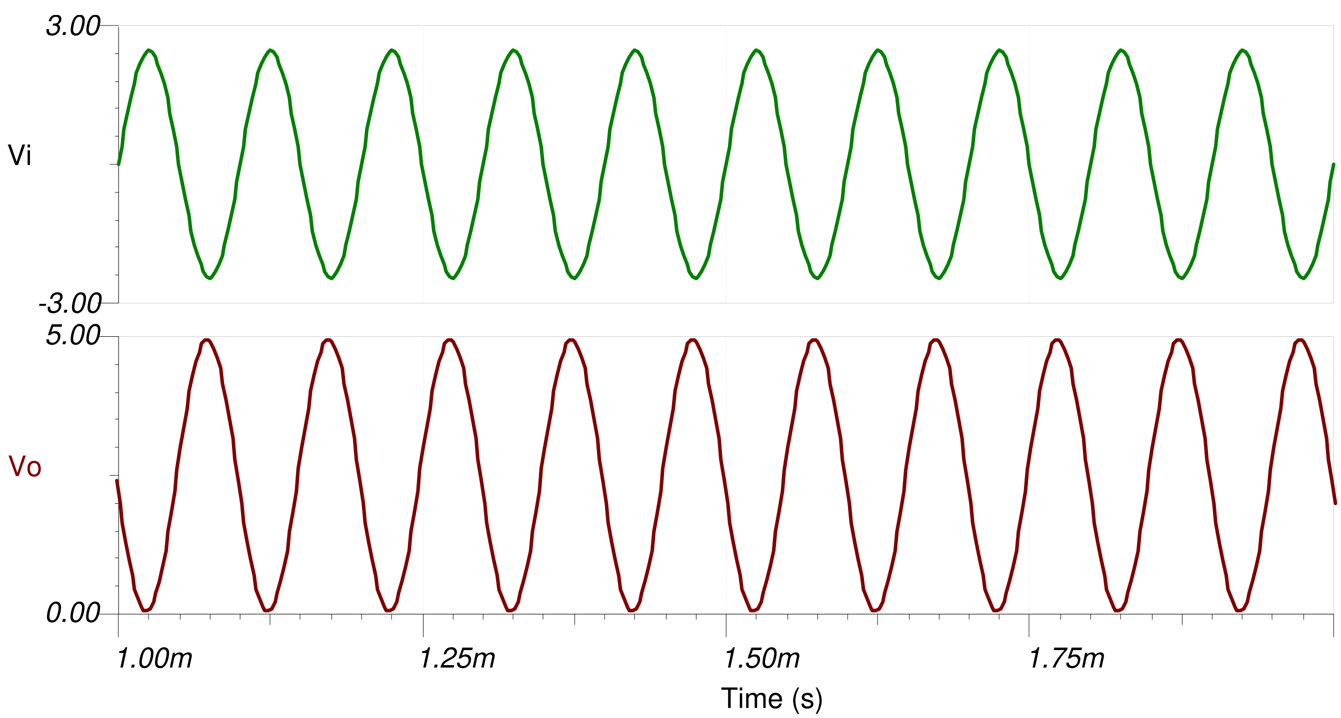
The TLV9062 device has GBW of 10MHz and SR of 6.5V/µs, so the requirements are met.

Design Simulations

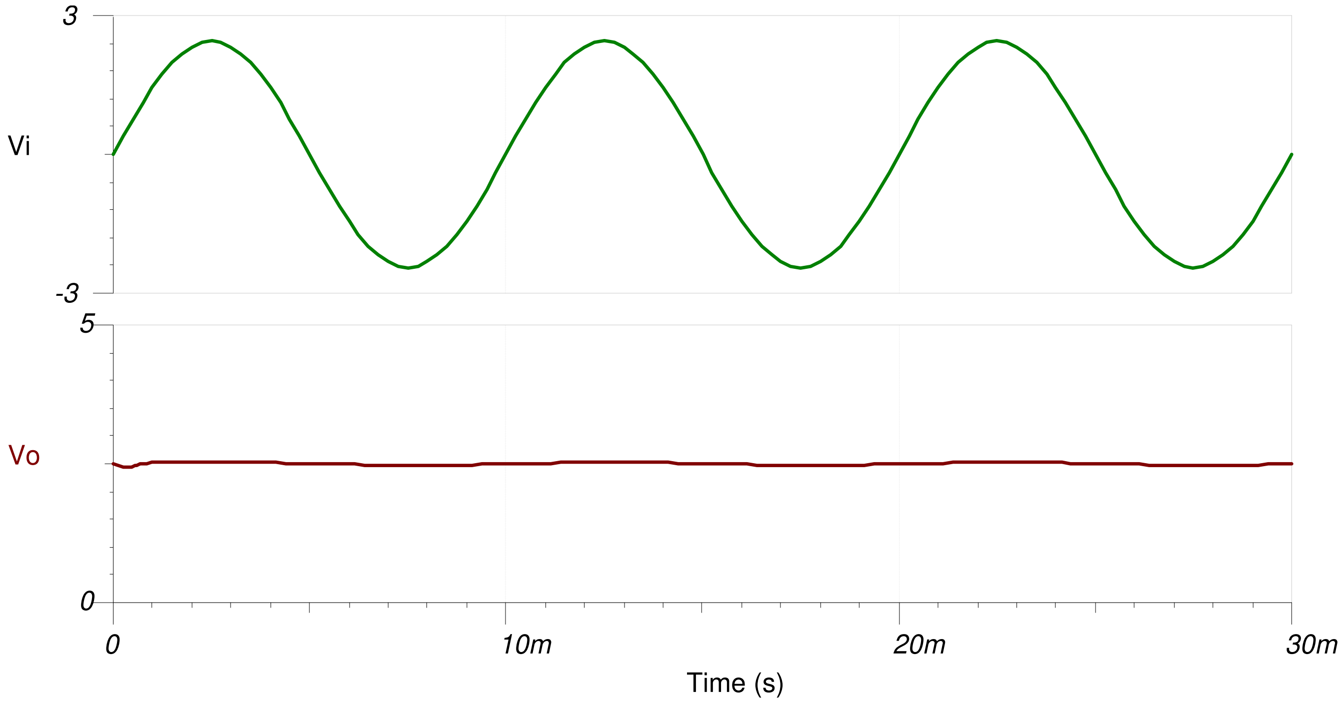
AC Simulation Results



Transient Simulation Results



Filter Output in Response to a 5-V_{pp}, 10-kHz Input-Signal (Gain = –1V/V).



Filter Output in Response to a 5-V_{pp}, 100-Hz Input-Signal (Gain = –0.01V/V)

Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation File: SBOC599.
3. TI Precision Labs.
4. *Active Low-Pass Filter Design Application Report*

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
Vout	Rail-to-Rail
Vos	0.3mV
Iq	538µA
Ib	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-Rail	Rail-to-Rail
Vout	Rail-to-Rail	Rail-to-Rail
V_{os}	0.75mV	0.150mV
Iq	400µA	650µA
Ib	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Analog Engineer's Circuit

Single-supply, 2nd-order, multiple feedback band-pass filter circuit

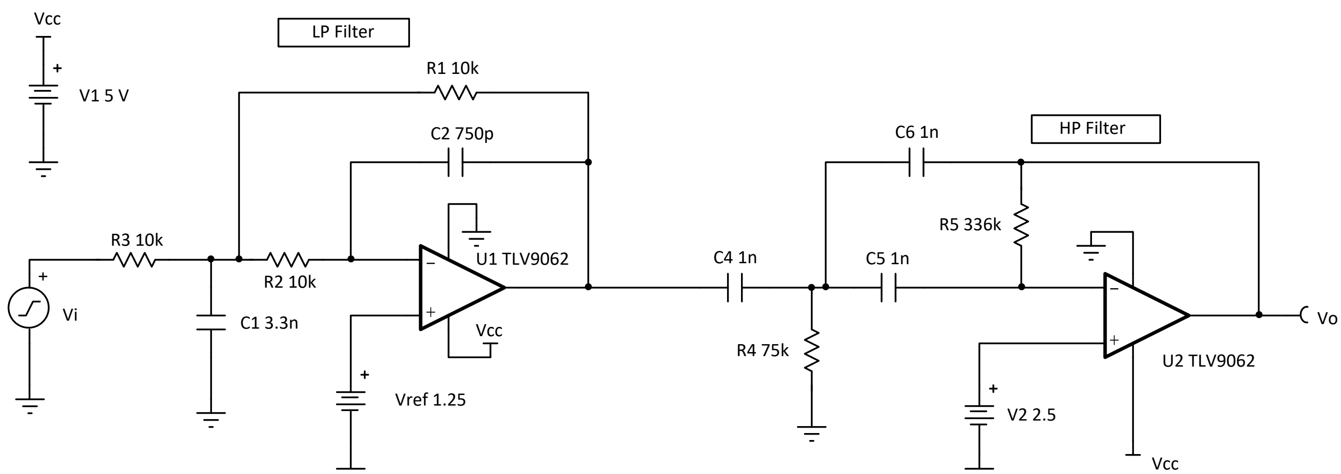
Amplifiers

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–2.45V	+2.45V	0.05V	4.95V	5V	0V

Gain	Low Cut-off Frequency (f_l)	High Cut-off Frequency (f_h)	V_{ref}
1V/V	1kHz	10kHz	1.25V and 2.5V

Design Description

This circuit is a 2nd-order multiple feedback (MFB) band-pass (BP) filter. This BP filter is created by cascading a low-pass and a high-pass filter. V_{ref} provides a DC offset to accommodate for single-supply applications.



Design Notes

1. Select an op amp with sufficient input common-mode range and output voltage swing.
2. Add V_{ref} to bias the input signal to meet the input common-mode range and output voltage swing.
3. Select the capacitor values first since standard capacitor values are more coarsely subdivided than the resistor values. Use high-precision, low-drift capacitor values to avoid errors in f_l and f_h.
4. To minimize the amount of slew-induced distortion, select an op amp with sufficient slew rate (SR).
5. For HP filters the maximum frequency is set by the gain bandwidth (GBW) of the op amp. Therefore, be sure to select an op amp with sufficient GBW.

Design Steps

This BP filter design involves two cascaded filters, a low-pass (LP) filter and a high-pass (HP) filter. The lower cutoff frequency (f_l) of the BP filter is 1kHz and the higher cutoff frequency (f_h) is 10kHz. The design steps show an LP filter design with f_h of 10kHz and a HP filter design with f_l of 1kHz. See MFB low-pass filter design and MFB high-pass filter design in the circuit cookbook for details on transfer function equations and calculations.

LP Filter Design

1. Use MFB low-pass filter design to determine R_1, R_2, and R_3.

$$R_1 = 10\text{k}\Omega,$$
$$R_2 = 10\text{k}\Omega,$$
$$R_3 = 10\text{k}\Omega$$

2. Use MFB low-pass filter design to determine C_1 and C_2.

$$C_1 = 3.3\text{nF (Standard Value)}, C_2 = 750\text{pF (Standard Value)}$$

HP Filter Design

1. Use MFB high-pass filter design to determine C_4, C_5, and C_6.

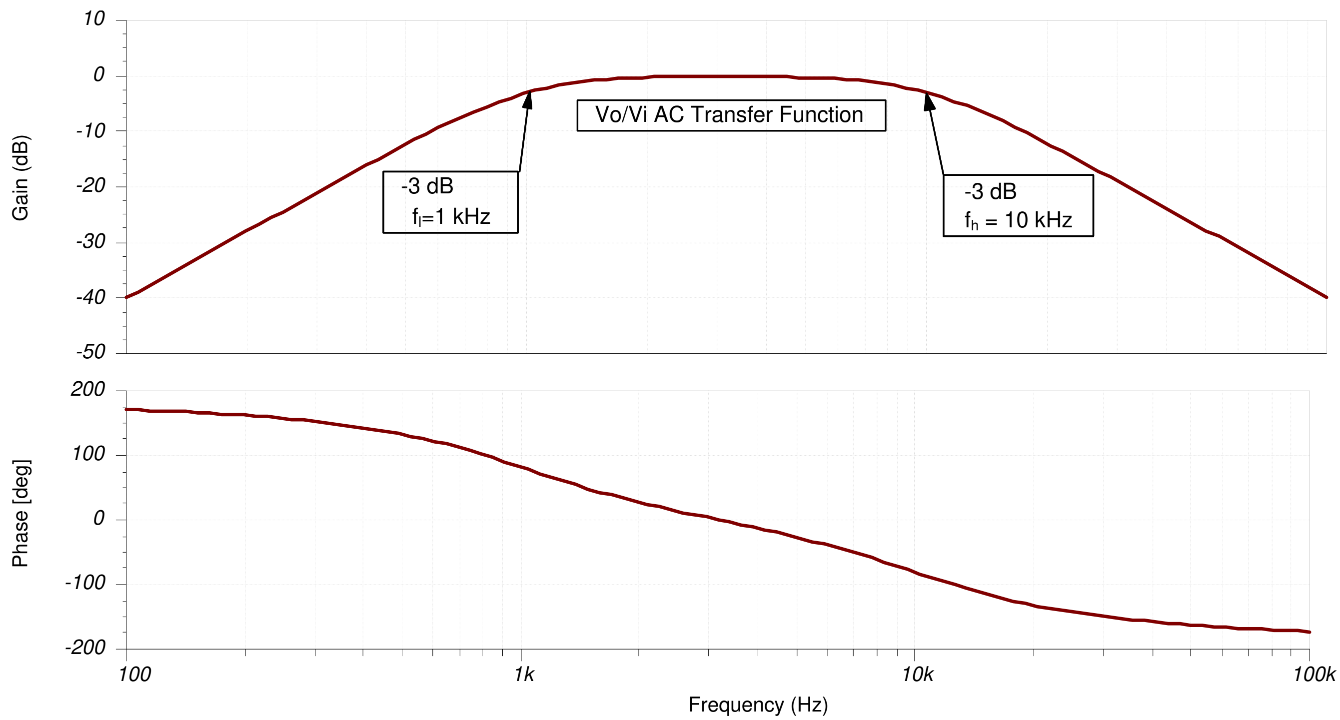
$$C_4 = 1\text{nF},$$
$$C_5 = 1\text{nF},$$
$$C_6 = 1\text{nF}$$

2. Use MFB high-pass filter design to determine R_4 and R_5.

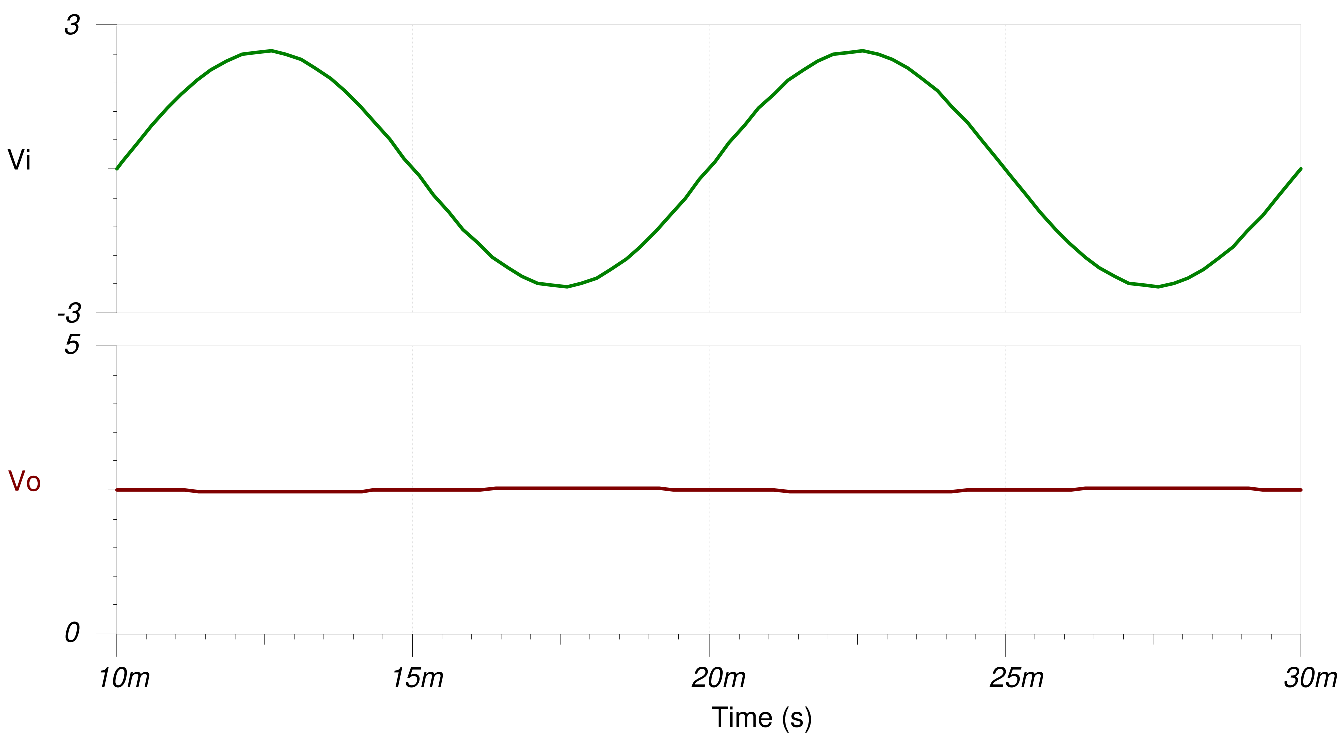
$$R_4 = 75\text{k}\Omega,$$
$$R_5 = 336\text{k}\Omega$$

Design Simulations

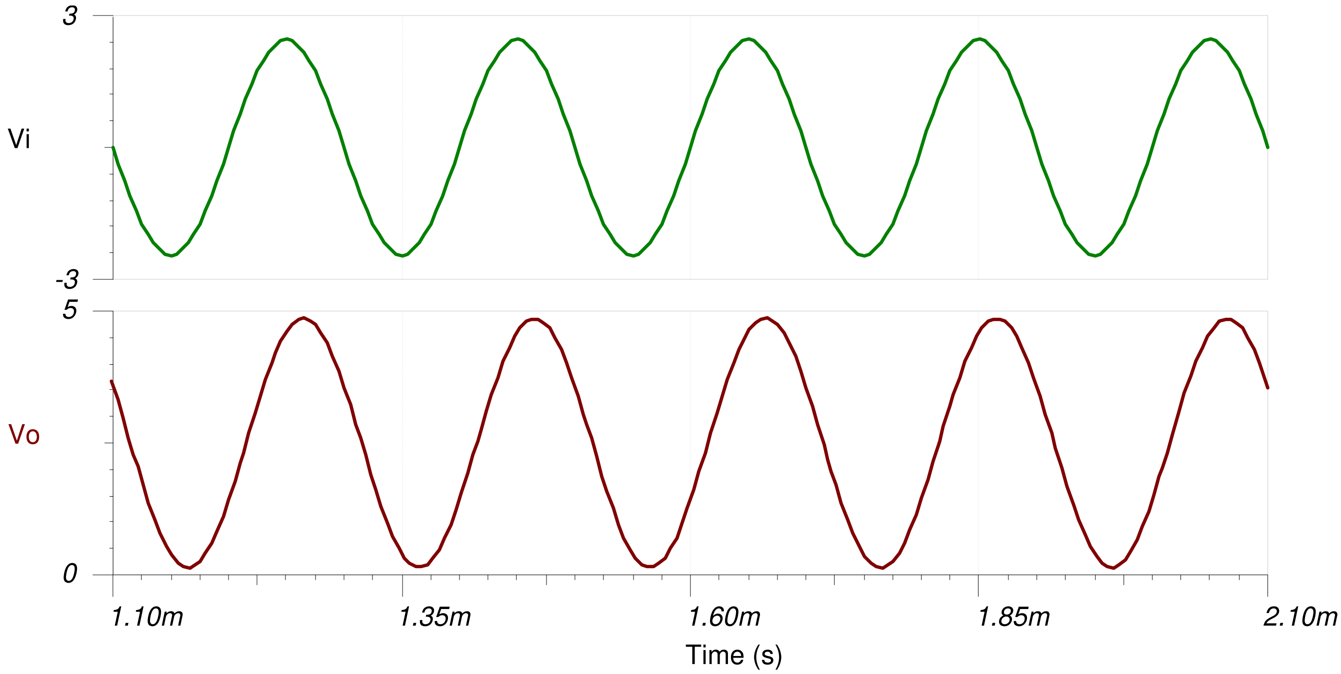
AC Simulation Results



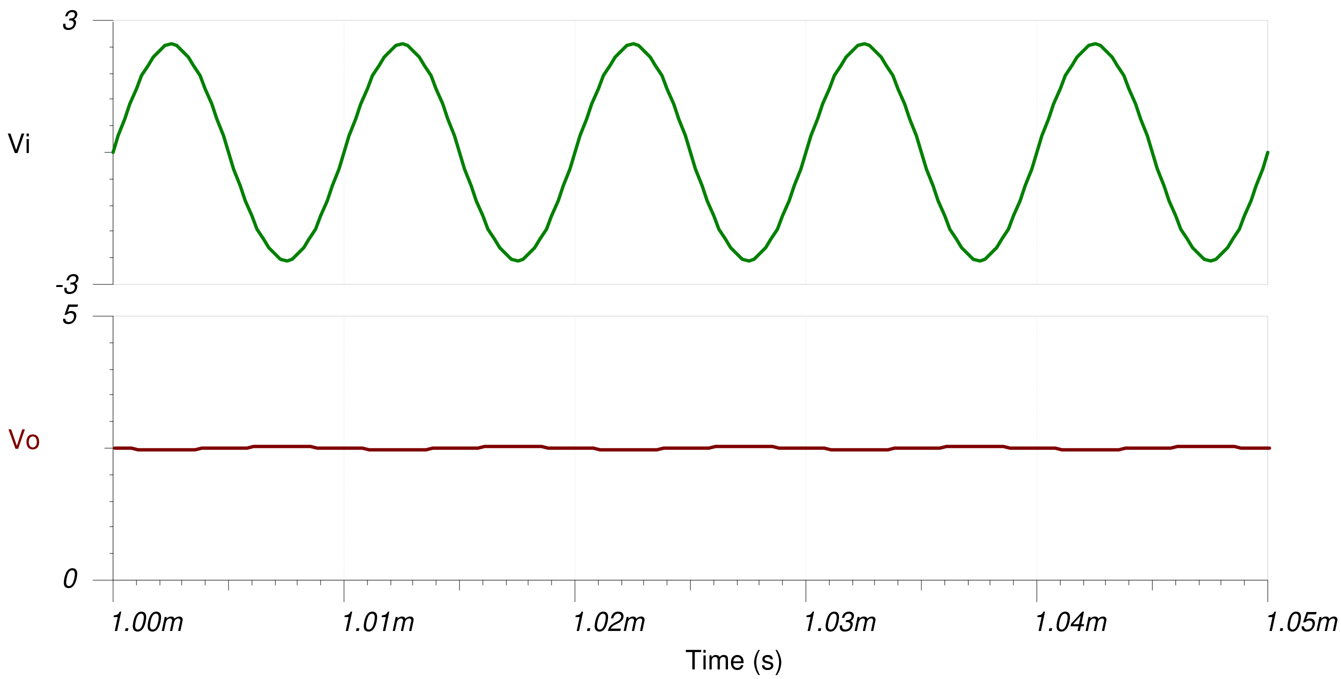
Transient Simulation Results



Filter Ouput in Response to a 5-Vpp, 100-Hz Input Signal (Gain = 0.01V/V)



Filter Ouput in Response to a 5-Vpp, 5-kHz Input Signal (Gain = 1V/V)



Filter Ouput in Response to a 5-Vpp, 100-kHz Input Signal (Gain = 0.01V/V)

Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation File: SBOC596.
3. TI Precision Labs.

Design Featured Op Amp

TLV9062	
Vss	1.8V to 5.5V
VinCM	Rail-to-Rail
Vout	Rail-to-Rail
Vos	0.3mV
Iq	538µA
Ib	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amp

	TLV316	OPA325
Vss	1.8V to 5.5V	2.2V to 5.5V
VinCM	Rail-to-Rail	Rail-to-Rail
Vout	Rail-to-Rail	Rail-to-Rail
Vos	0.75mV	0.150mV
Iq	400µA	650µA
Ib	10pA	0.2pA
UGBW	10MHz	10MHz
SR	6V/µs	5V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV316	www.ti.com/product/OPA325

Fast-Settling Low-Pass Filter Circuit

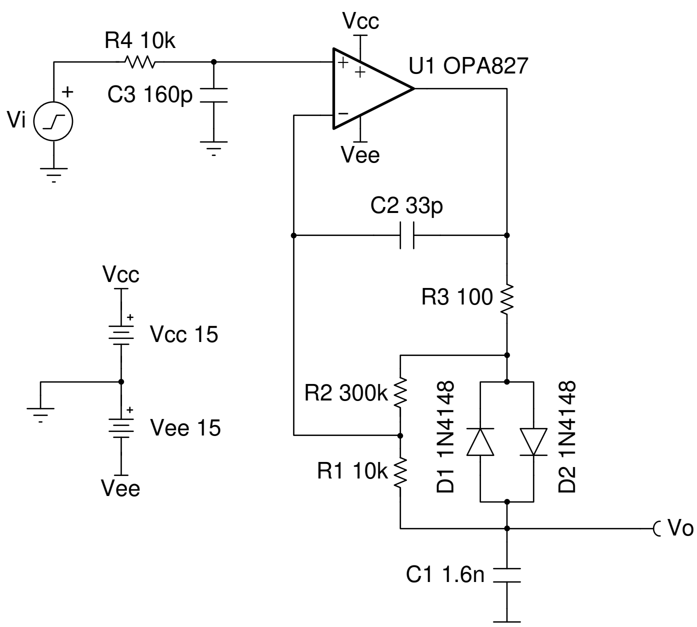
Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–12 V	12 V	–12 V	12 V	15 V	–15 V

Cutoff Frequency (f_c)	Diode Threshold Voltage (V_t)
10 kHz	20 mV

Design Description

This low-pass filter topology offers a significant improvement in settling time over the conventional single-pole RC filter. This is achieved through the use of diodes D_1 and D_2, that allow the filter capacitor to charge and discharge much faster when there is a large enough difference between the input and output voltages.



Design Notes

1. Observe the common-mode input limitations of the op amp.
2. Keeping C_1 small will ensure the op amp does not struggle to drive the capacitive load.
3. For the fastest settling time, use fast switching diodes.
4. The selected op amp should have sufficient output drive capability to charge C_1. R_3 limits the maximum charge current.

Design Steps

1. Select standard values for R_1 and C_1 based on f_C = 10kHz.

$$R_1 = 10k\Omega$$

$$C_1 = \frac{1}{2\pi \times f_C \times R_1} = \frac{1}{2\pi \times 10kHz \times 10k\Omega} = 1.6nF$$

2. Set the diode threshold voltage (V_t). This threshold is the minimum difference in voltage between the input and output that will result in diode conduction (fast capacitor charging and discharging).

$$V_t = \frac{V_f}{1 + \frac{R_2}{R_1}} \approx \frac{0.6V}{1 + \frac{R_2}{R_1}} = 20mV$$

$$R_2 = \left(\frac{0.6V}{20mV} - 1\right) \times R_1 = 290k\Omega \quad \approx \quad 300k\Omega \quad \text{(standard 5\% value)}$$

3. Select components for noise pre-filtering.

$$f_{c2} = 10 \times f_c = 100kHz$$

$$f_{c2} = \frac{1}{2\pi \times R_4 \times C_3}$$

$$\text{Select} \quad R_4 = R_1 = 10k\Omega$$

$$C_3 = \frac{C_1}{10} = 160pF$$

4. Add compensation components to stabilize U_1. R_3 limits the charge current into C_1 and also serves to isolate the capacitance from the op amp output when the diodes are conducting. Larger values will improve stability but increase C_1 charge time.

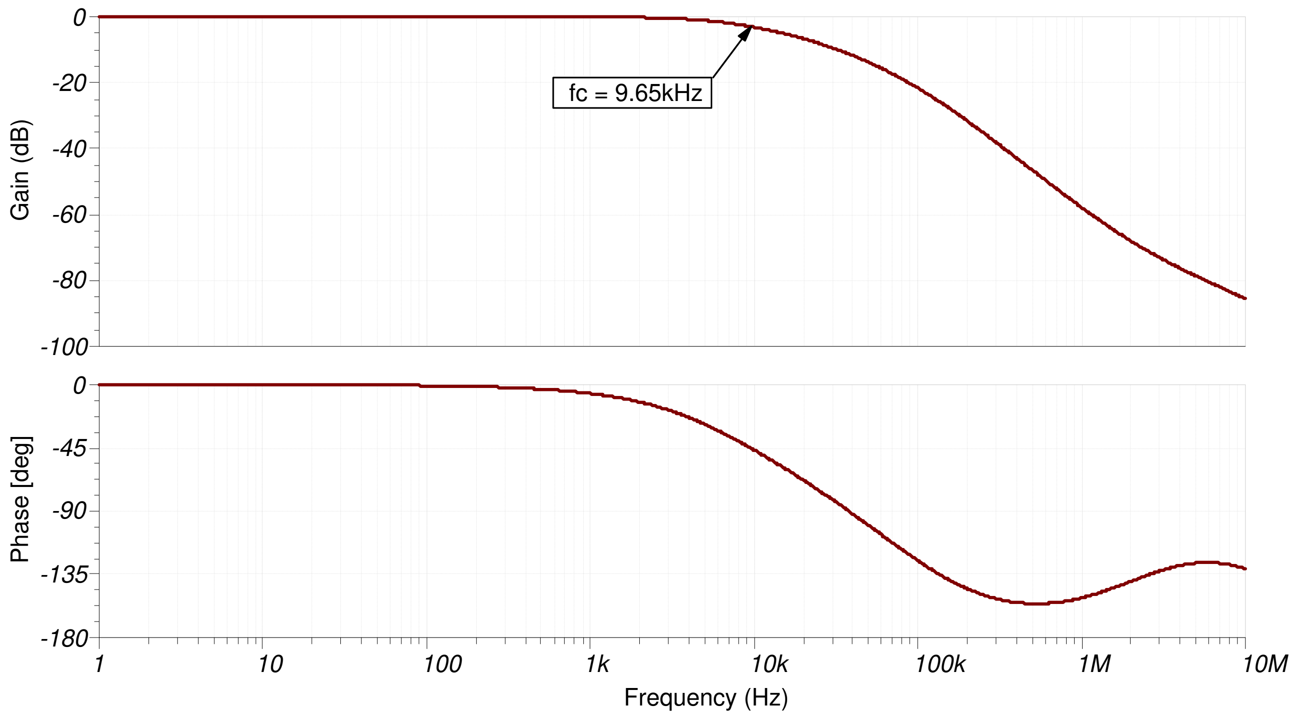
$$\text{Select} \quad R_3 = 100\Omega$$

5. C_2 provides local high frequency feedback to counteract the interaction between the input capacitance with the parallel combination of R_1 and R_2. To prevent interaction with C_1, select C_2 as the following shows:

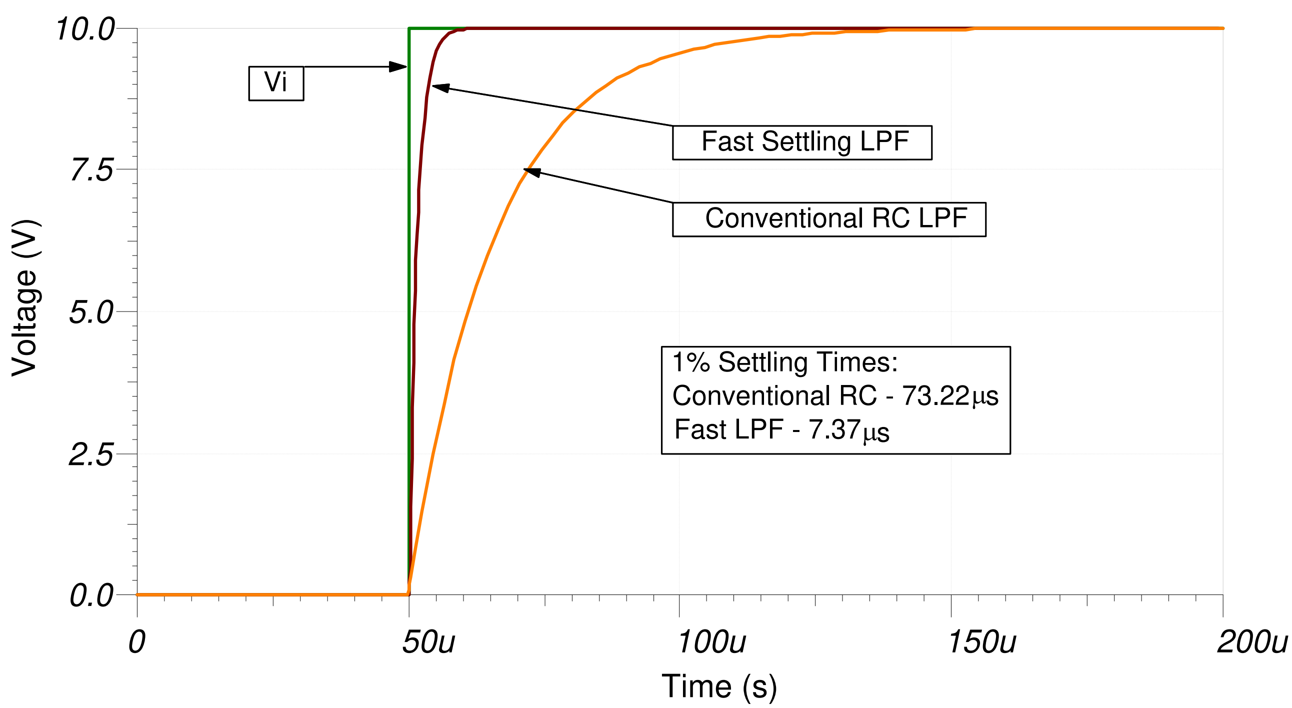
$$\text{Select} \quad C_2 = \frac{C_1}{50} = 32pF \approx 33pF \text{ (standard value)}$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, SBOMAU1.

For more information on many op amp topics including common-mode range, output swing, bandwidth, and how to drive an ADC, see *TI Precision Labs*.

Design Featured Op Amp

OPA827	
V_{ss}	8 V to 36 V
V_{inCM}	V_{ee}+3 V to V_{cc}–3 V
V_{out}	V_{ee}+3 V to V_{cc}–3 V
V_{os}	75 µV
I_q	4.8 mA
I_b	3 pA
UGBW	22 MHz
SR	28 V/µs
#Channels	1
OPA827	

Design Alternate Op Amp

TLC072	
V_{ss}	4.5 V to 16 V
V_{inCM}	V_{ee}+0.5 V to V_{cc}–0.8 V
V_{out}	V_{ee}+350 mV to V_{cc}–1 V
V_{os}	390 µV
I_q	2.1 mA/Ch
I_b	1.5 pA
UGBW	10 MHz
SR	16 V/µs
#Channels	1, 2, and 4
TLC072	

Analog Engineer's Circuit

AC Coupled (HPF) Inverting Amplifier Circuit

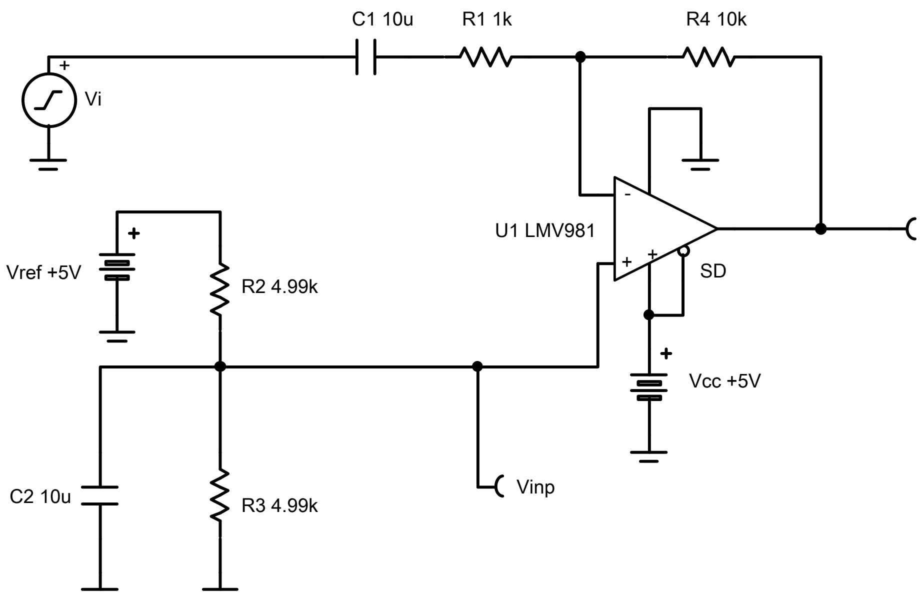
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–240 mV	240 mV	0.1 V	4.9 V	5 V	0 V	5 V

Design Description

This circuit amplifies an AC signal and shifts the output signal so that it is centered at half the power supply voltage. Note that the input signal has zero DC offset so it swings above and below ground. The key benefit of this circuit is that it accepts signals which swing below ground even though the amplifier does not have a negative power supply.



Design Notes

1. R_1 sets the AC input impedance. R_4 loads the op amp output.
2. Use low feedback resistances to reduce noise and minimize stability concerns.
3. Set the output range based on linear output swing (see A_{ol} specification).
4. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_4. Adding a capacitor in parallel with R_4 will also improve stability of the circuit if high-value resistors are used.

Design Steps

1. Select R_1 and R_4 to set the AC voltage gain.

$$R_1 = 1\ \ \text{k}\Omega\ (\text{Standard Value})$$

$$R_4 = R_1 \times |G_{ac}| = 1\ \ \text{k}\Omega \times \left|-10\frac{V}{V}\right| = 10\text{k}\Omega\ (\text{Standard Value})$$

2. Select R_2 and R_3 to set the DC output voltage to 2.5 V.

$$R_3 = 4.99\text{k}\Omega\ (\text{Standard Value})$$

$$R_2 = \frac{R_3 \times V_{ref}}{V_{DC}} - R_3 = \frac{4.99\text{k}\Omega \times 5\text{V}}{2.5\text{V}} - 4.99\text{k}\Omega = 4.99\text{k}\Omega$$

3. Choose a value for the lower cutoff frequency, f_l, then calculate C_1.

$$f_l = 16\text{Hz}$$

$$C_1 = \frac{1}{2 \times \pi \times R_1 \times f_l} = \frac{1}{2 \times \pi \times 1\ \ \text{k}\Omega \times 16\text{Hz}} = 9.94\mu\text{F} \approx 10\mu\text{F}\ (\text{Standard Value})$$

4. Choose a value for f_{div}, then calculate C_2.

$$f_{div} = 6.4\text{Hz}$$

$$R_{div} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{4.99\text{k}\Omega \times 4.99\text{k}\Omega}{4.99\text{k}\Omega + 4.99\text{k}\Omega} = 2.495\text{k}\Omega$$

$$C_2 = \frac{1}{2 \times \pi \times R_{div} \times f_{div}} = \frac{1}{2 \times \pi \times 2.495\text{k}\Omega \times 6.4\text{Hz}} = 9.96\mu\text{F} \approx 10\mu\text{F}\ (\text{Standard Value})$$

5. The upper cutoff frequency, f_h, is set by the noise gain of this circuit and the gain bandwidth (GBW) of the device (LMV981).

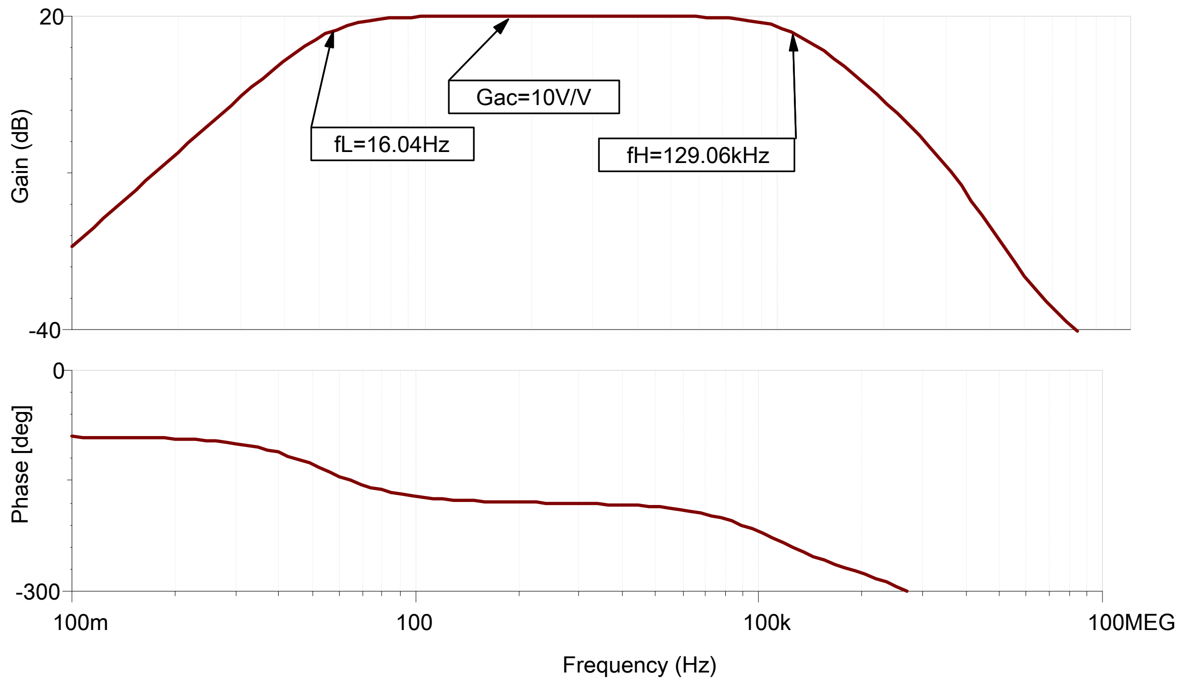
$$GBW = 1.5\text{MHz}$$

$$G_{noise} = 1 + \frac{R_4}{R_1} = 1 + \frac{10\text{k}\Omega}{1\ \ \text{k}\Omega} = 11\frac{V}{V}$$

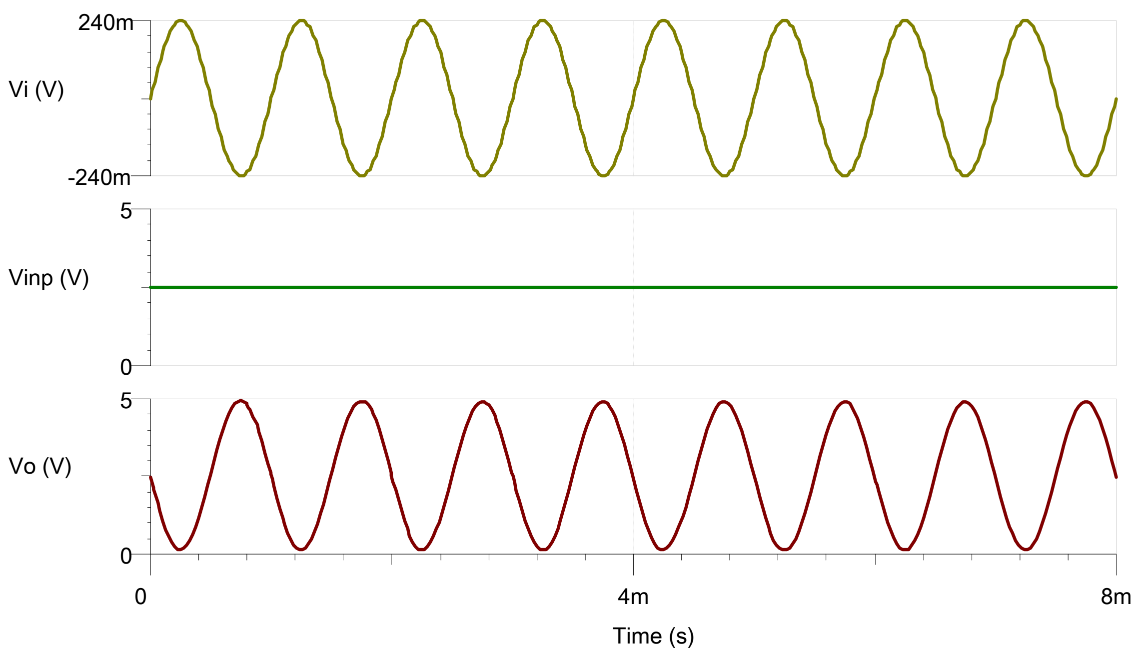
$$f_h = \frac{GBW}{G_{noise}} = \frac{1.5\text{MHz}}{11\frac{V}{V}} = 136.3\text{kHz}$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC504.

See TIPD185.

Design Featured Op Amp

LMV981	
V_{cc}	1.8 V to 5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	116 µA
I_b	14 nA
UGBW	1.5 MHz
SR	0.42 V/µs
#Channels	1 and 2
LMV981	

Design Alternate Op Amp

LMV771	
V_{cc}	2.7 V to 5 V
V_{inCM}	V_{ee} to (V_{cc}–0.9 V)
V_{out}	Rail-to-rail
V_{os}	0.25 mV
I_q	600 µA
I_b	–0.23 pA
UGBW	3.5 MHz
SR	1.5 V/µs
#Channels	1 and 2
LMV771	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.............	1

Band Pass Filtered Inverting Attenuator Circuit

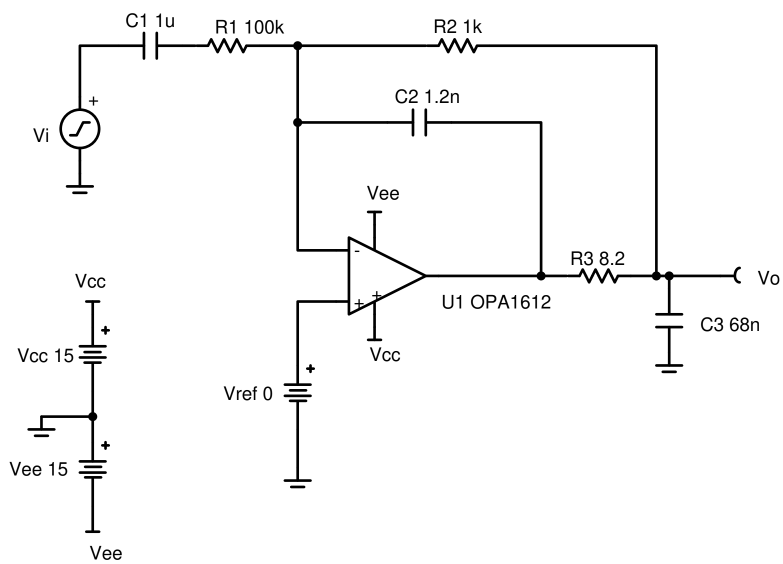
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
100 mV_{pp}	50 V_{pp}	1m V_{pp}	500 mV_{pp}	15 V	–15 V	0 V

Design Description

This tunable band-pass attenuator reduces signal level by –40 dB over the frequency range from 10 Hz to 100 kHz. It also allows for independent control of the DC output level. For this design, the pole frequencies were selected outside the pass band to minimize attenuation within the specified bandwidth range.



Design Notes

1. If a DC voltage is applied to V_{ref} be sure to check common mode limitations.
2. Keep R_3 as small as possible to avoid loading issues while maintaining stability.
3. Keep the frequency of the second pole in the low-pass filter (f_{p3}) at least twice the frequency of the first low-pass filter pole (f_{p2}).

Design Steps

1. Set the passband gain.

$$\text{Gain} = -\frac{R_2}{R_1} = -0.01\ \frac{V}{V}\left(-40\text{dB}\right)$$

$$R_1 = 100\text{k}\Omega$$

$$R_2 = 0.01 \times R_1 = 1\ \ \text{k}\Omega$$

2. Set high-pass filter pole frequency (f_{p1}) below f_l.

$$f_l = 10\text{Hz}, f_{p1} = 2.5\ \text{Hz}$$

3. Set low-pass filter pole frequency (f_{p2} and f_{p3}) above f_h.

$$f_h = 100\text{kHz}$$

$$f_{p2} = 150\text{kHz}$$

$$f_{p3} \geq 2 \times f_{p2} = 300\text{kHz}$$

$$f_{p3} = 300\text{kHz}$$

4. Calculate C_1 to set the location of f_{p1}.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_{p1}} = \frac{1}{2\pi \times 100\text{k}\Omega \times 2.5\text{Hz}} = 0.636\ \mu\text{F} \approx 1\ \ \mu\text{F (Standard Value)}$$

5. Select components to set f_{p2} and f_{p3}.

$$R_3 = 8.2\Omega\ \text{(provides stability for cap loads up to 100nF)}$$

$$C_2 = \frac{1}{2\pi \times \left(R_2 + R_3\right) \times f_{p2}} = \frac{1}{2\pi \times 1008.2\Omega \times 150\text{kHz}}$$
$$= 1052\text{pF} \approx 1200\text{pF (Standard Value)}$$

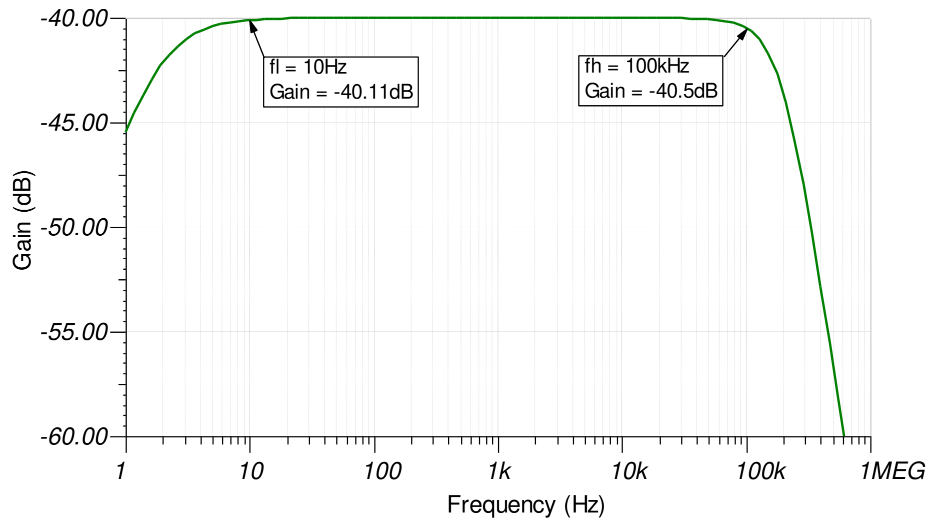
$$C_3 = \frac{1}{2\pi \times R_3 \times f_{p3}} = \frac{1}{2\pi \times 8.2\Omega \times 300\text{kHz}} = 64.7\ \text{nF} \approx 68\text{nF (Standard Value)}$$

Design Simulations

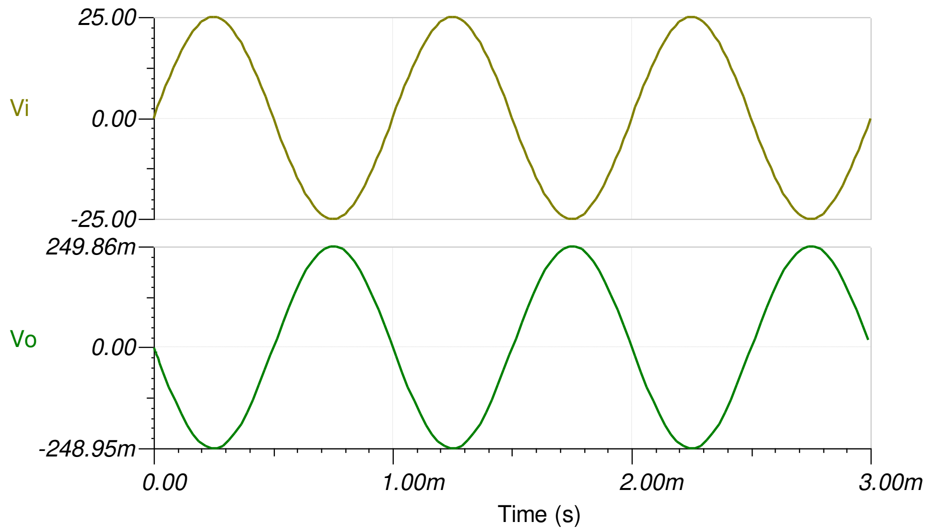
DC Simulation Results

The amplifier will pass DC voltages applied to the noninverting pin up to the common mode limitations of the op amp (±13 V in this design)

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC503.

See TIPD118.

Design Featured Op Amp

OPA1612	
V_{ss}	4.5 V to 36 V
V_{inCM}	V_{ee}+2 V to V_{cc}–2 V
V_{out}	V_{ee}+0.2 V to V_{cc}–0.2 V
V_{os}	100 µV
I_q	3.6 mA/Ch
I_b	60 nA
UGBW	40 MHz
SR	27 V/µs
#Channels	1 and 2
OPA1612	

Design Alternate Op Amp

OPA172	
V_{ss}	4.5 V to 36 V
V_{inCM}	V_{ee}–100 mV to V_{cc}–2 V
V_{out}	Rail-to-rail
V_{os}	200 µV
I_q	1.6 mA/Ch
I_b	8 pA
UGBW	10 MHz
SR	10 V/µs
#Channels	1, 2, and 4
OPA172	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from July 31, 2017 to February 1, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page............. 1

Analog Engineer's Circuit

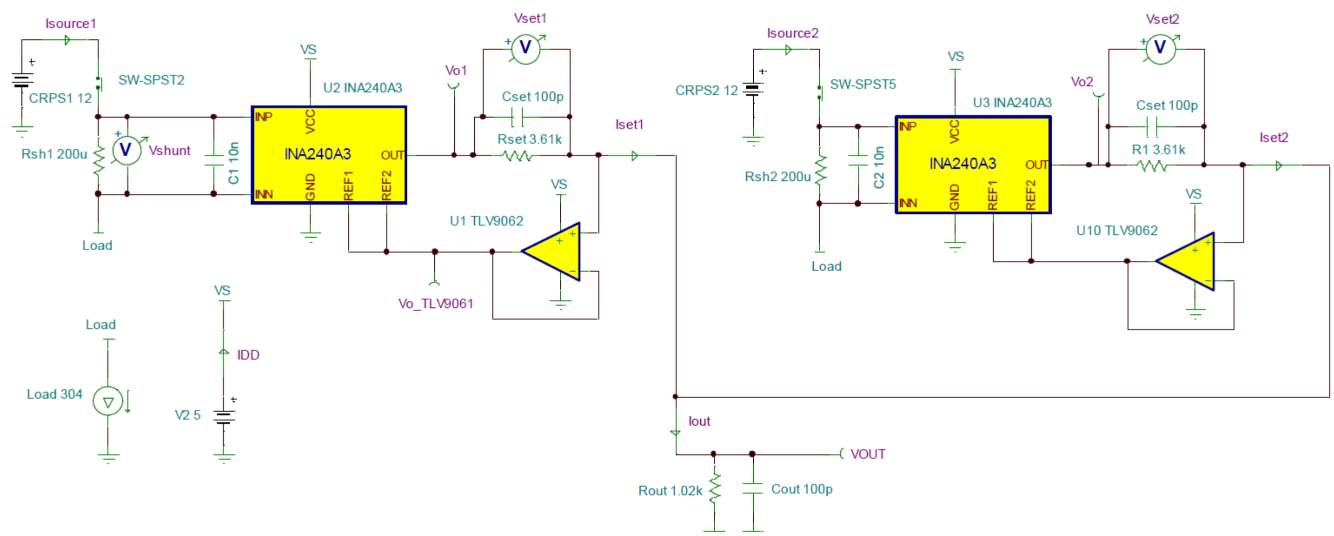
Circuit to measure multiple redundant source currents with singled-ended signal

Amplifiers

Input			Output			Error	Supply		
I_{LOAD} Min	$I_{LOAD\ Max}$	V_{CM}	$I_{OUT\ Min}$	$I_{OUT\ Max}$	Bandwidth	I_{LOAD} > 45 A	I_{DD}	V_S	V_{ee}
5A	304A	12V	42.1µA	1.6842mA	400kHz	2.1% maximum at full-scale range	N × (2.4mA + 750µA) + I_{OUT}	5V	GND (0V)

Design Description

This circuit demonstrates how to convert a voltage-output, current-sense amplifier (CSA) into a current-output circuit using the Howland Current Pump method and operational amplifier (op amp). Furthermore, this circuit demonstrates how to design two separate circuits to measure two separate, but redundant supplies powering one load.



Design Notes

1. The *Getting Started with Current Sense Amplifiers* video series introduces implementation, error sources, and advanced topics for using current sense amplifiers.
2. Choose precision 0.1% resistors to limit gain error at higher currents.
3. The output current (I_{OUT}) is sourced from the VS supply, which adds to the I_Q of the current sense amplifier.
4. Use the V_{OUT} versus I_{OUT} curve ("claw-curve") of the CSA (INA240A3) to set the I_{OUT} limit during maximum power. If a higher signal current is needed, then add an op amp buffer to the output of the current sense amplifier. A buffer on the output allows for smaller R_{OUT}.
5. For applications with higher bus voltages, simply substitute in a bidirectional current sense amplifier with a higher rated input voltage.
6. The V_{OUT} voltage is the input common-mode voltage (V_{CM}) for the op amp.
7. Offset errors can be calibrated out with one-point calibration given that a known sense current is applied and the circuit is operating in the linear region. Gain error calibration requires a two-point calibration.
8. Include a small feed-forward capacitor (C_{SET}) to increase BW and decrease V_{OUT} settling time to a step response in current. Increasing C_{SET} too much introduces gain peaking in the system gain curve, which results in output overshoot to a step response.
9. Follow best practices for printed-circuit board (PCB) layout according to the data sheet: place the decoupling capacitor close to the VS pin, routing the input traces for IN+ and IN– as a differential pair, and so forth.

Design Steps

1. Choose an available current-sense amplifier (CSA) that meets the common-mode voltage requirement. For this design the INA240A3 is selected.
   - Note that choosing the most optimal CSA for the system requires balancing tradeoffs in CSA offset, CSA gain error, shunt resistor power rating and thus total circuit design could require multiple iterations to achieve the satisfactory error over the entire dynamic range of the load.
2. Determine the maximum output current ($I_{SET\_100\%}$) and maximum output swing ($V_{O\_ISYS\_MAX}$) of the INA240A3. Use the output current vs output voltage curve in the data sheet. For this design, choose the maximum I_{SET} to be 850 µA with a maximum output swing of {Vs – 0.2V} = 4.8V = $V_{O\_ISYS\_MAX}$.
3. Given the ADC full-scale range (V_{ADC_FSR} = 1.8V), the number of sources to measure (N = 2), and the maximum CSA output current when the source is at 100% power ($I_{SET\_100\%}$ = 850µA), calculate the maximum allowable R_{OUT} which converts signal current to signal voltage for ADC. For this design R_{OUT} = 1020 Ω is selected.

$$I_{OUT\_I_{SYS\_MAX}} = \text{Total signal current from all N channels when system/load current is at its maximum (304-A).}$$

$$I_{SET1\_100\%} = \text{Signal current from INA240A3 channel 1 when Source 1 is at 100\% power (152-A).}$$

$$V_{ADC\_FSR} = V_{OUT\_I_{SYS\_MAX}} < 1.8V$$

$$I_{OUT\_I_{SYS\_MAX}} = I_{SET1\_100\%} + I_{SET2\_100\%} = I_{SET\_100\%} \times N$$

$$V_{OUT\_I_{SYS\_MAX}} = I_{OUT\_I_{SYS\_MAX}} \times R_{OUT}$$

$$\therefore R_{OUT} < \frac{V_{OUT\_I_{SYS\_MAX}}}{I_{OUT\_I_{SYS\_MAX}}} = \frac{1.8V}{850\mu A \times 2} = 1058.82\Omega$$

$$\rightarrow R_{OUT} = 1020\Omega, 0.1\%$$

$$\rightarrow V_{OUT\_I_{SYS\_MAX}} = 1.734V < 1.8V$$

4. Using the following system of equations, we can solve for the minimum allowable R_{SET}. For this design, R_{SET} = 3610 Ω is selected.

$$V_{OUT\_I_{SYS\_MAX}} = I_{OUT\_I_{SYS\_MAX}} \times R_{OUT}$$
$$V_{OUT\_I_{SYS\_MAX}} = V_{O\_I_{SYS\_MAX}} - V_{SET\_100\%}$$
$$V_{SET\_100\%} = I_{SET\_100\%} \times R_{SET}$$
$$\therefore R_{SET} \geq \frac{V_{O\_I_{SYS\_MAX}} - I_{SET\_100\%} \times R_{OUT} \times N}{I_{SET\_100\%}}$$
$$\therefore R_{SET} \geq \frac{V_{O\_I_{SYS\_MAX}}}{I_{SET\_100\%}} - \left(R_{OUT} \times N\right) = 3607.06\Omega$$
$$\rightarrow R_{SET} = 3610\Omega, 0.1\%$$

5. Using the following system of equations, solve for the maximum allowable shunt resistor. For this design, choose R_{SHUNT} = 200 µΩ.

$$V_{SET1\_100\%} = R_{SET} \times I_{SET1\_100\%} = 3610\Omega \times 850\mu A = 3.0685V$$
$$V_{SHUNT\_100\%} = \frac{V_{SET1\_100\%}}{Gain_{INA240A3}} = \frac{3.0685V}{100 V/V} = 30.685mV$$
$$R_{SHUNT} \leq \frac{V_{SHUNT\_100\%}}{I_{SOURCE\_100\%}} = \frac{30.685mV}{152A}$$
$$\therefore R_{SHUNT} \leq 201.88\mu\Omega$$
$$\rightarrow R_{SHUNT} = 200\mu\Omega, 1\%$$

6. Check that the common-mode voltage (V_{CM}) and output voltage ($V_{O\_TLV9061}$) of the TLV9061 are in the operational region when the circuit is sensing the minimum required 5% source current. The TLV9061 device is a rail-to-rail-input-output (RRIO) op amp so it can operate with very small V_{CM} and output voltages, but A_{OL} will vary. Testing conditions from the data sheet for CMRR and A_{OL} show that choosing $V_{OUT\_5\%}$ ≥ 40mV provides sufficient A_{OL} when circuit sensing minimum load current.
   - If a lower operational V_{CM} is needed, then consider providing a small negative voltage source to the negative supply pin to extend the range of the op amp or current-sense amplifier.

$$V_{O\_MIN\_TLV9061} = 40mV$$
$$V_{SHUNT\_5\%} = 5\% \times I_{SOURCE\_MAX} \times R_{SHUNT} = 7.6A \times 200\mu\Omega$$
$$\therefore V_{SHUNT\_5\%} = 1.52mV$$
$$V_{OUT\_5\%} = V_{SHUNT\_5\%} \times Gain \times \frac{R_{OUT}}{R_{SET}}$$
$$\therefore V_{OUT\_5\%} = 42.94mV > V_{O\_MIN\_TLV9061}$$

7. Using the following equations, calculate and tabulate the total, worst-case RSS error over the dynamic range of the source.

$$RE_{MAX\_P} = \text{Max Positive Relative Error} = \frac{V_{OUT\_MAX} - V_{OUT\_TYP}}{V_{OUT\_TYP}}$$
$$RE_{MAX\_N} = \text{Max Negative Relative Error} = \frac{V_{OUT\_MIN} - V_{OUT\_TYP}}{V_{OUT\_TYP}}$$
$$E_{RSS} = \sqrt{e_{V_{OS\_CSA}}{}^2 + e_{V_{OS\_OPA}}{}^2 + e_{R_{SHUNT}}{}^2 + e_{Gain\_CSA}{}^2 + e_{R_{OUT}}{}^2 + e_{R_{SET}}{}^2}$$
$$V_{OUT\_TYP} = I_{SOURCE1} \times R_{SHUNT\_TYP} \times G_{TYP} \times \frac{R_{OUT\_TYP}}{R_{SET\_TYP}}$$
$$V_{OUT\_MAX} = \left[\left(I_{SOURCE1} \times R_{SHUNT\_MAX} + V_{OS\_CSA\_MAX}\right) \times G_{MAX\_CSA} + V_{OS\_OPA\_MAX}\right] \times \frac{R_{OUT\_MAX}}{R_{SET\_MIN}}$$
$$V_{OUT\_MIN} = \left[\left(I_{SOURCE1} \times R_{SHUNT\_MIN} - V_{OS\_CSA\_MAX}\right) \times G_{MIN\_CSA} - V_{OS\_OPA\_MAX}\right] \times \frac{R_{OUT\_MIN}}{R_{SET\_MAX}}$$

$T_{MAX} = 80^{o}C$

$\varDelta T_{MAX} = 80^{o}C - 25°C = 55°C$

$R_{SHUNT} = 200\mu\Omega,\ 0.1\%,\ 175\frac{ppm}{°C}$

$V_{VS} = 5V; V_{CM} = 12V$

$V_{OSI\_OPA} = \pm 2mV$

$V_{OS\_OPA\_CMRR} = \left|V_{OUT} - 2.5V\right| \times 10^{(-80dB/20dB)}$

$V_{OS\_OPA\_MAX} = V_{OSI\_OPA} + V_{OS\_OPA\_CMRR} + \varDelta T_{MAX} \times \left(530\frac{nV}{°C}\right)$

$V_{OSI\_CSA\_MAX} = \pm 25\mu V$

$V_{OS\_CSA\_CMRR\_MAX} = \left|12V - V_{CM}\right| \times 10^{\left(-CMRR_{MIN}/20dB\right)} = 0$

$V_{OS\_CSA\_PSRR\_MAX} = \left|5V - V_{VS}\right| \times PSRR_{MAX} = 0$

$V_{OS\_Drift\_MAX} = \varDelta T_{MAX} \times \left(\frac{\varDelta V_{OS}}{\varDelta T}\right) = 55°C \times \left(250\frac{nV}{°C}\right) = \pm 13.75\mu V$

$V_{OS\_CSA\_MAX} = V_{OSI\_MAX} + V_{OS\_CMRR} + V_{OS\_PSRR} + V_{OS\_Drift}$

$V_{OS\_CSA\_MAX} = \pm 38.75\mu V$

$e_{V_{OS\_CSA}} = {V_{OS\_CSA\_MAX}}/{V_{SHUNT\_IDEAL}} \times 100$

$e_{V_{OS\_OPA}} = {V_{OS\_OPA\_MAX}}/{V_{SET\_IDEAL}} \times 100$

$e_R = e_{R_{TOLERANCE}} + e_{R_{DRIFT}}$

$e_{R_{SHUNT}} = 1\% + \varDelta T_{MAX} \times TC = 1\% + 55°C \times \left(175\frac{ppm}{°C}\right) \times 10^{-4} = 1.963\%$

$e_{R_{SET}} = e_{R_{OUT}} = 1\% + 55°C \times \left(50\frac{ppm}{°C}\right) \times 10^{-4} = 1.275\%$

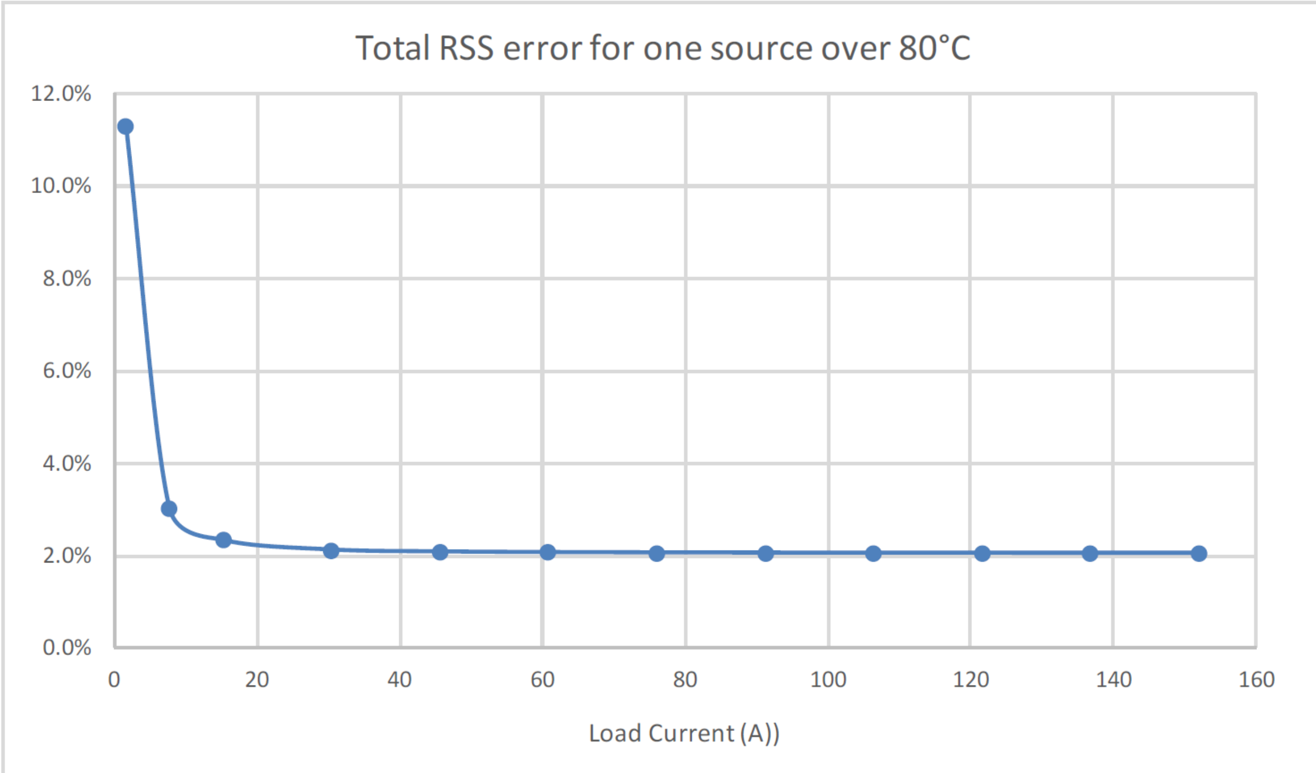
$e_{GAIN\_CSA\_25C} = \pm 0.2\%$

$e_{GAIN\_Drift\_CSA\_MAX} = \varDelta T_{MAX} \times \left(2.5\frac{ppm}{°C}\right) \times 10^{-4} = \pm 0.01375\%$

$G_{MAX} = G_{TYP} \times \left(1 + e_{25C\_MAX} + e_{Drift\_MAX}\right) = 100\,\frac{V}{V} \times (1.002138) = 100.2138\,\frac{V}{V}$

$G_{MIN} = G_{TYP} \times \left(1 - e_{25C\_MAX} - e_{Drift\_MAX}\right) = 100\,\frac{V}{V} \times \left(0.997862\right) = 99.7862\,\frac{V}{V}$

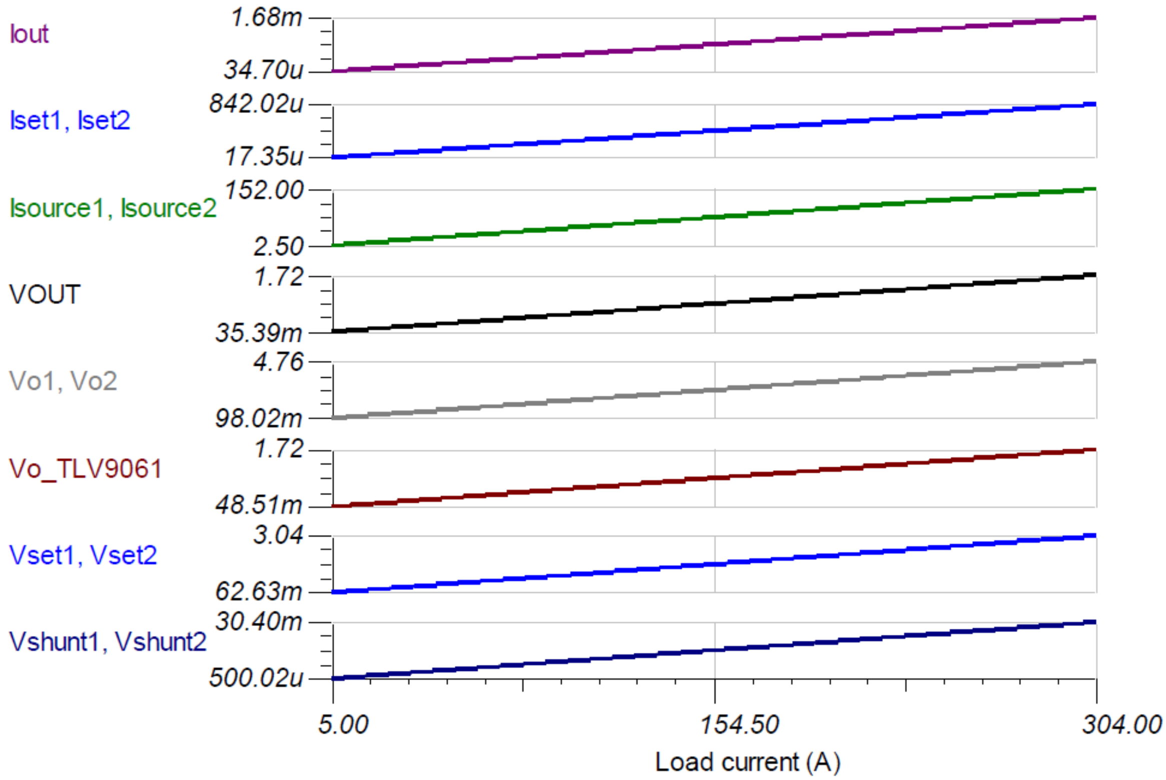
8. Plot the total error as a function of load current



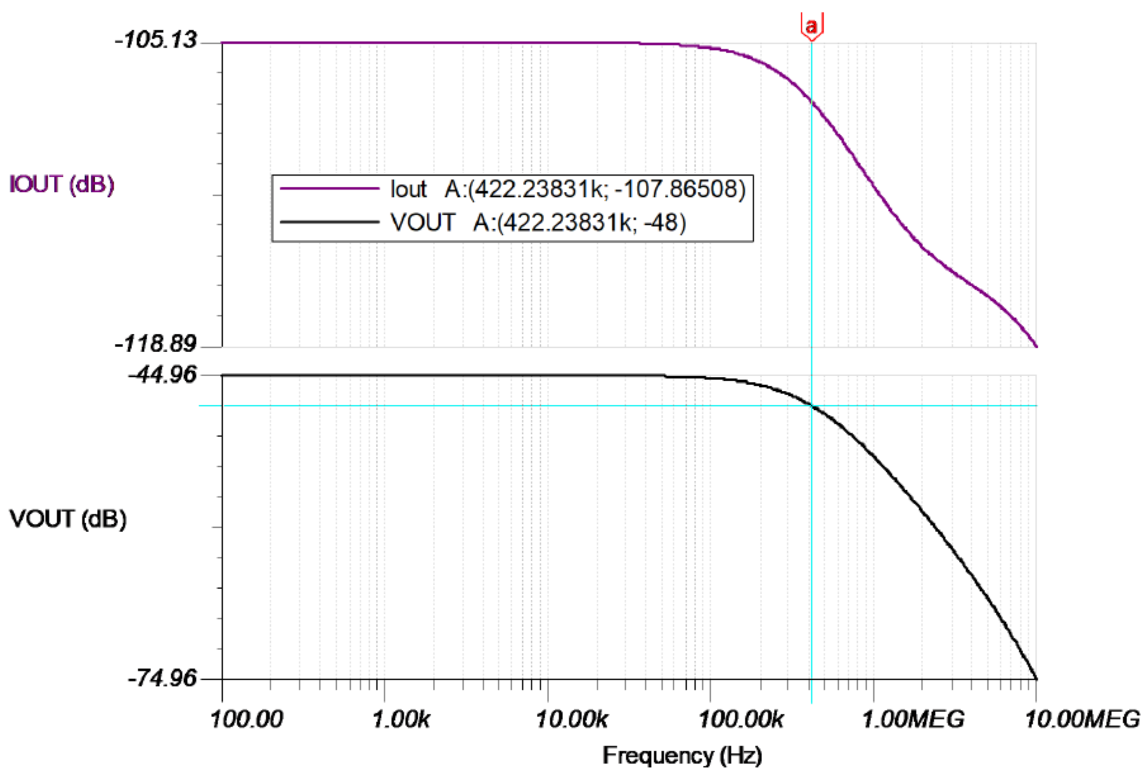
Design Simulations

DC Simulation Results

The following graph shows a linear output response for load currents from 5A to 304A.



AC Simulation Result – I_{LOAD} to I_{OUT} (V_{OUT}) circuit gain



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Getting Started with Current Sense Amplifiers video series

https://training.ti.com/getting-started-current-sense-amplifiers

Current Sense Amplifiers on TI.com

http://www.ti.com/amplifier-circuit/current-sense/products.html

Comprehensive Study of the Howland Current Pump

http://www.ti.com/analog/docs/litabsmultiplefilelist.tsp?literatureNumber=snoa474a&docCategoryId=1&familyId=78

For direct support from TI Engineers use the E2E community

http://e2e.ti.com

Design Featured Current Sense Amplifier

INA240A3	
V_S	2.7V to 5.5V (operational)
V_{CM}	–4V to 80V
Swing to V_S (V_{SP})	V_S – 0.2V
V_{OS}	±25µV at 12V V_{CM}
I_{Q_MAX}	2.4mV
I_{IB}	90µA at 12V
BW	400kHz
# of channels	1
Body size (including pins)	4mm × 3.91mm
www.ti.com/product/ina240	

Design Featured Operational Amplifier

TLV9061 (TLV9061S is shutdown version)	
V_S	1.8V to 5.5V
V_{CM}	(V–) – 0.1V < V_{CM} < (V+) + 0.1V
CMRR	103dB
A_{OL}	130dB
V_{OS}	±1.6mV maximum
I_Q	750µA maximum
I_B (input bias current)	± 0.5pA
GBP (gain bandwidth product)	10MHz
# of channels	1 (2 and 4 channel packages available)
Body size (including pins)	0.80mm × 0.80mm
www.ti.com/product/tlv9061	

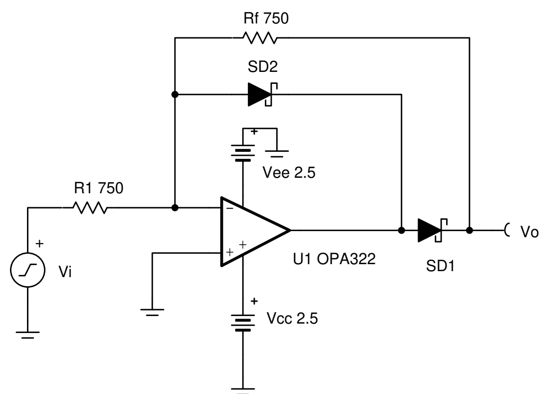
Half-Wave Rectifier Circuit

Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
±0.2 mV_{pp}	±4 V_{pp}	0.1 V_p	2 V_p	2.5 V	–2.5 V

Design Description

The precision half-wave rectifier inverts and transfers only the negative-half input of a time varying input signal (preferably sinusoidal) to its output. By appropriately selecting the feedback resistor values, different gains can be achieved. Precision half-wave rectifiers are commonly used with other op amp circuits such as a peak-detector or bandwidth limited non-inverting amplifier to produce a DC output voltage. This configuration has been designed to work for sinusoidal input signals between 0.2 mV_{pp} and $4V_{pp}$ at frequencies up to 50 kHz.



Design Notes

1. Select an op amp with a high slew rate. When the input signal changes polarities, the amplifier output must slew two diode voltage drops.
2. Set output range based on linear output swing (see A_{ol} specification).
3. Use fast switching diodes. High-frequency input signals will be distorted depending on the speed by which the diodes can transition from blocking to forward conducting mode. Schottky diodes might be a preferable choice, since these have faster transitions than pn-junction diodes at the expense of higher reverse leakage.
4. The resistor tolerance sets the circuit gain error.
5. Minimize noise errors by selecting low-value resistors.

Design Steps

1. Set the desired gain of the half-wave rectifier to select the feedback resistors.

$$V_o = Gain \times V_i$$

$$Gain = -\frac{R_f}{R_1} = -1$$

$$R_f = R_1 = 2 \times R_{eq}$$

   - Where R_{eq} is the parallel combination of R_1 and R_f
2. Select the resistors such that the resistor noise is negligible compared to the voltage broadband noise of the op amp.

$$E_{nr} = \sqrt{4 \times k_b \times T \times R_{eq}}$$

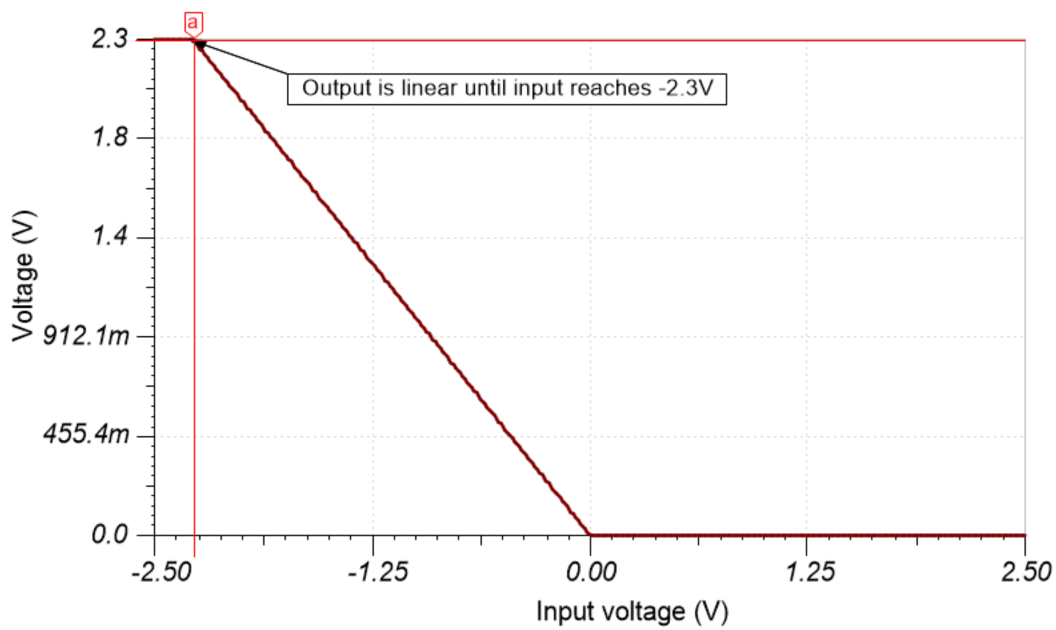
$$R_{eq} \le \frac{Enbb^2}{4 \times k_b \times T \times 3^2} = (Enbb)$$

$$= 7.5\frac{nV}{\sqrt{Hz}} = \frac{\left(7.5 \times 10^{-9}\right)^2}{4 \times 1.381 \times 10^{-23} \times 298 \times 3^2} = 380\Omega$$

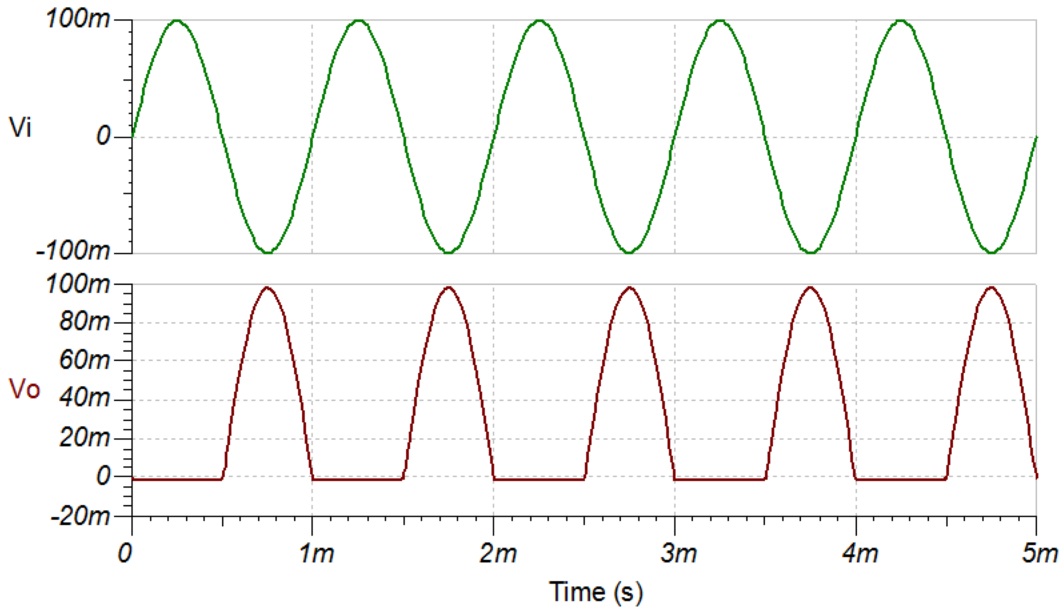
$$R_f = R_1 \le 760\Omega \rightarrow 750\Omega \text{ (Standard Value)}$$

Design Simulations

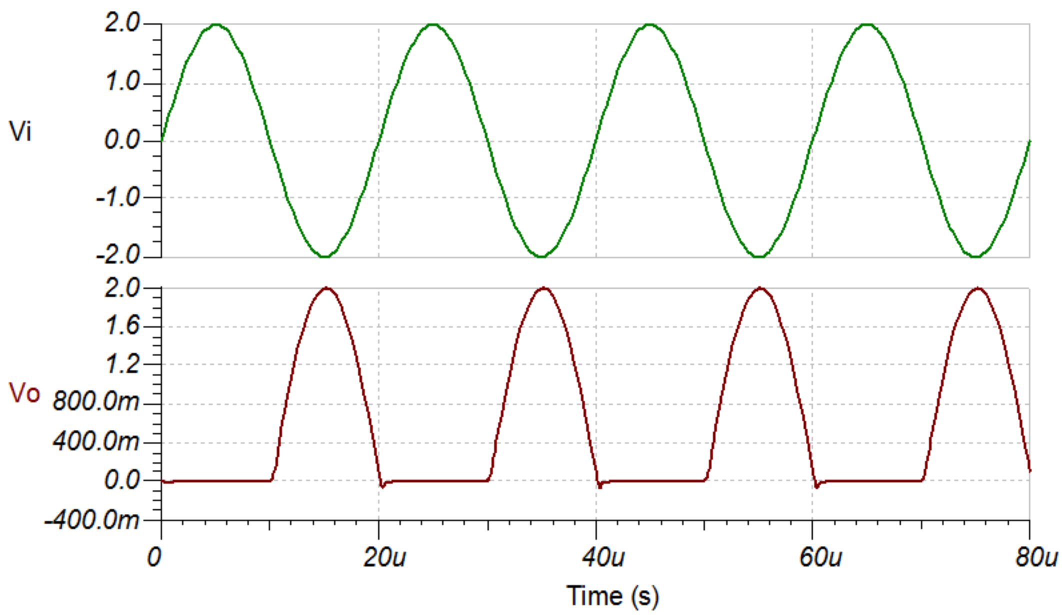
DC Simulation Results



Transient Simulation Results



200 mV$_{pp}$ at 1 kHz



2 V$_{pp}$ at 50 kHz

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC509.

Design Featured Op Amp

OPA322	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	500 µV
I_q	1.6 mA/Ch
I_b	0.2 pA
UGBW	20 MHz
SR	10 V/µs
#Channels	1, 2, and 4
OPA3222	

Design Alternate Op Amp

OPA2325	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	40 µV
I_q	0.65 mA/Ch
I_b	0.2 pA
UGBW	10 MHz
SR	5 V/µs
#Channels	2
OPA2325	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from August 2, 2017 to February 1, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page and link to Spice simulation file.. 1

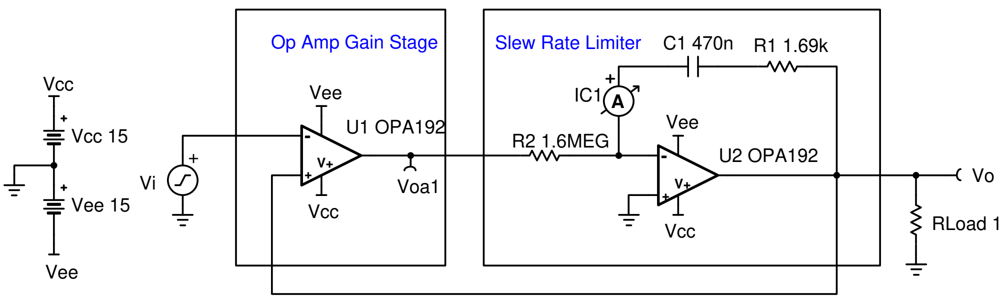
Slew Rate Limiter Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–10 V	10 V	–10 V	10 V	15 V	–15 V	0 V

Design Description

This circuit controls the slew rate of an analog gain stage. This circuit is intended for symmetrical slew rate applications. The desired slew rate must be slower than that of the op amp chosen to implement the slew rate limiter.



Design Notes

1. The gain stage op-amp and slew rate limiting op amp should both be checked for stability.
2. Verify that the current demands for charging or discharging C_1 plus any load current out of U_2 will not limit the voltage swing of U_2.

Design Steps

1. Set slew rate and choose a standard value for the feedback capacitor, C_1.

$$C_1 = 470\text{nF}$$

$$SR = 20\frac{V}{s}$$

2. Choose the value of R_2 to set the capacitor current necessary for the desired slew rate.

$$SR = \frac{I_{C_1}}{C_1}$$

$$20\frac{V}{s} = \frac{I_{C_1}}{470\text{nF}} \text{ where } I_{C_1} = 9.4\ \mu A$$

$$\text{Gain stage op amp } V_{sat} = \pm 14.995 \text{ (typical)}$$

$$I_{C_1} = \frac{V_{sat}}{R_2}$$

$$9.4\ \mu A = \frac{14.995V}{R_2}, \text{ so } R_2 = 1.595\ M\Omega \approx 1.6M\Omega \text{ (Standard Value)}$$

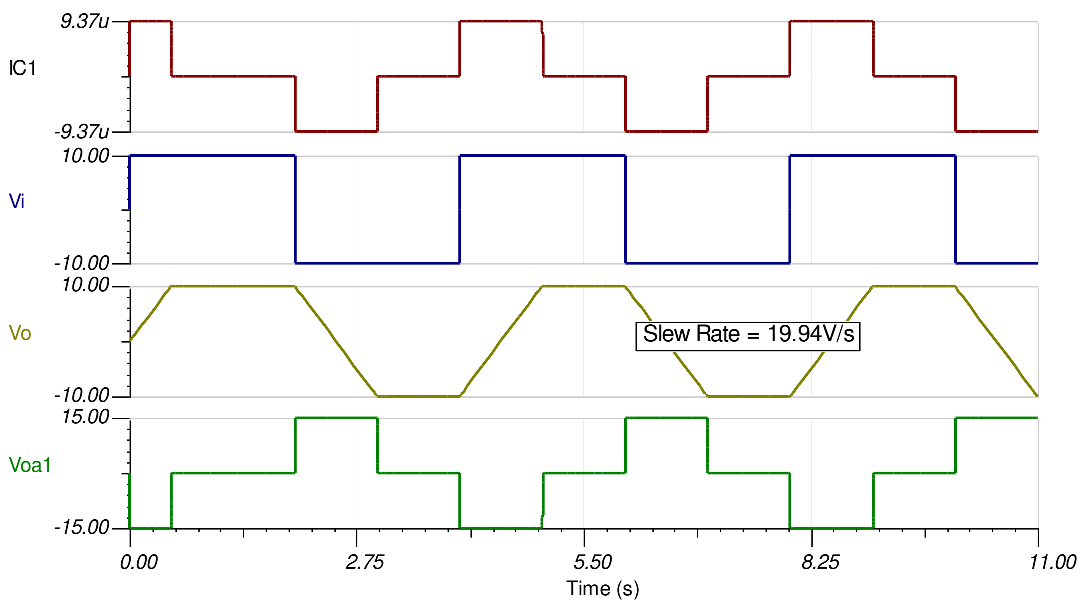
3. Compensate feedback network for stability. R_1 adds a pole to the 1/β network. This pole should be placed so that the 1/β curve levels off a decade before it intersects the open loop gain curve (200 Hz, for this example).

$$f_p = \frac{1}{2\pi \times R_1 \times C_1} = 200\text{Hz}$$

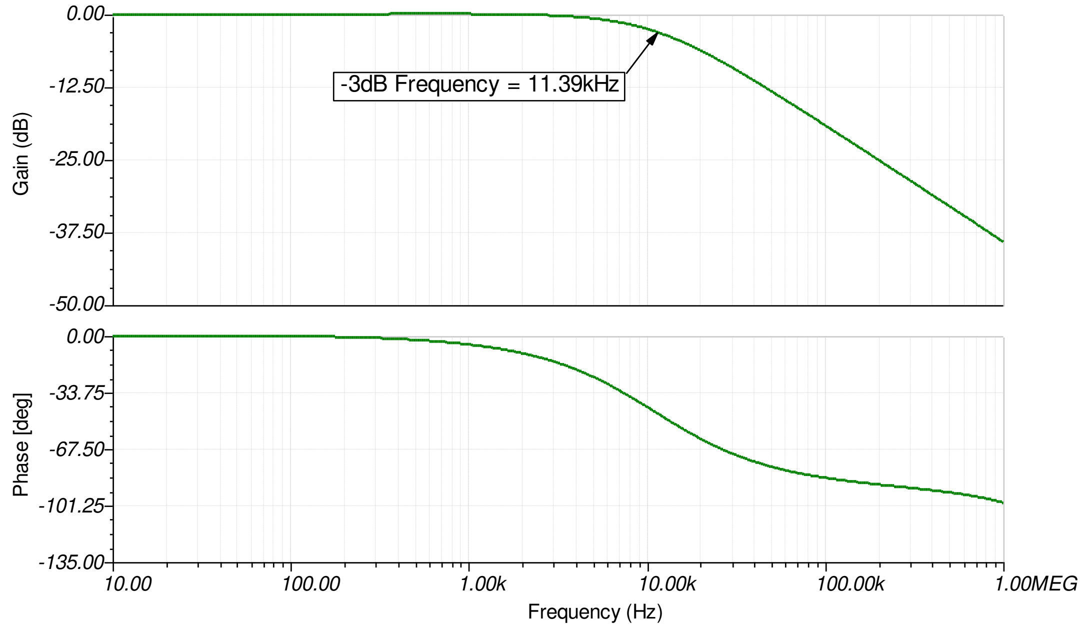
$$200\text{Hz} = \frac{1}{2\pi \times R_1 \times 470\text{nF}}, \text{ so } R_1 = 1.693\ k\Omega \approx 1.69k\Omega \text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC508.

See TIPD140.

Design Featured Op Amp

OPA192	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	1 mA/Ch
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA192	

Design Alternate Op Amp

TLV2372	
V_{cc}	2.7 V to 16 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2 mV
I_q	750 µA/Ch
I_b	1 pA
UGBW	3 MHz
SR	2.1 V/µs
#Channels	1, 2, and 4
TLV2372	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file	1

Single-supply, high-input voltage, full-wave rectifier circuit

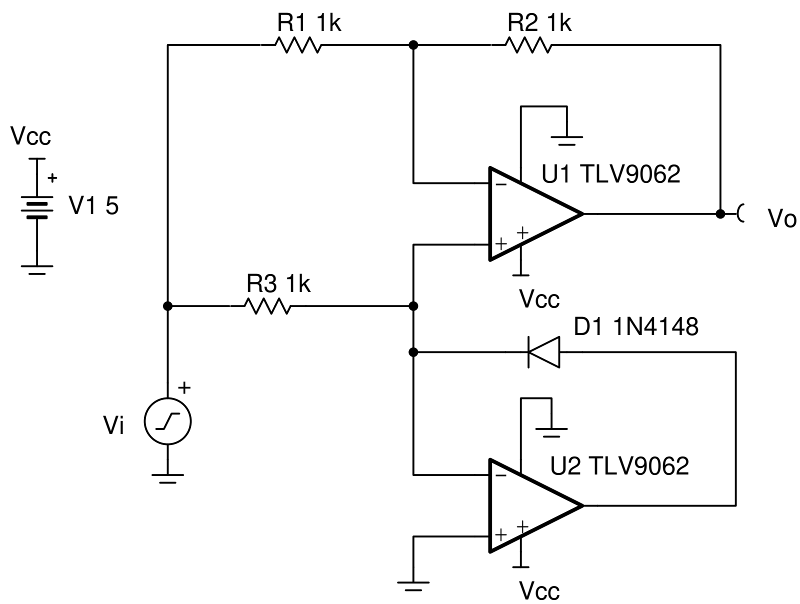
Amplifiers

Design Goals

Input	Output	Frequency	Supply	
V_{iMax}	V_{oMax}	f_{Max}	V_{cc}	V_{ee}
9Vpp	4.5Vpp	50kHz	5V	0V

Design Description

This single-supply precision full-wave rectifier is optimized for high-input voltages. When $V_i > 0V$, D_1 is reverse biased and the top part of the circuit, U1, is activated resulting in a circuit with a gain of 1V/V. When Vi < 0V, D_1 is forward biased and the bottom part of the circuit, U2, is activated resulting in an inverting amplifier circuit with a gain of –1V/V.

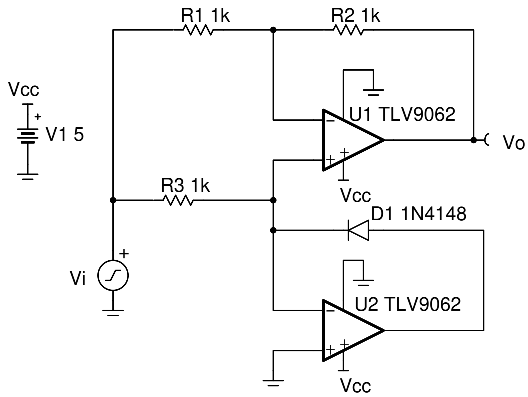


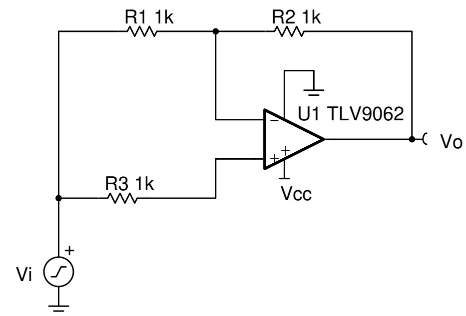
Design Notes

1. Observe common-mode and output swing limitations of op amps.
2. R_3 should be sized small enough that the leakage current from D_1 does not cause errors for positive input cycles while ensuring the op amp can drive the load.
3. Use a fast switching diode for D_1.
4. Resistor tolerance determines the gain error of the circuit.
5. Use a negative charge pump (such as the LM7705) for output swing requirements to GND to maintain linearity for output signals near 0V. For additional information. see *Single-supply, low-input voltage, full-wave rectifier circuit*.
6. For more information on op amp linear operating region, stability, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

1. Circuit analysis for positive input signals. D_1 is reverse-biased disconnecting the output of U_2 from the non-inverting input of U_1.

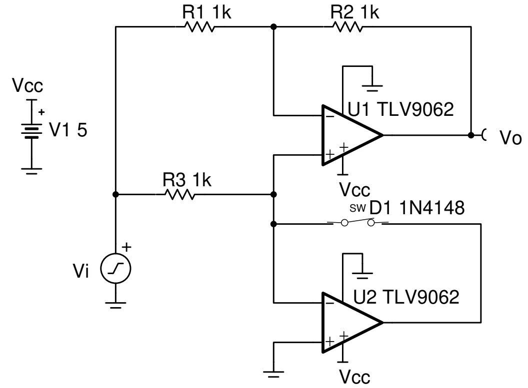


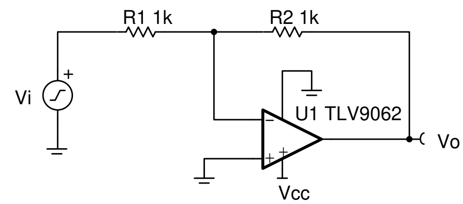


$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1}\right) + \left(1 + \frac{R_2}{R_1}\right) = 1$$

$$V_o = V_i$$

2. Circuit analysis for negative input signals. D_1 is forward biased, which connects the output of U_2 to the non-inverting input of U_1, which is GND.





$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1}\right) = -1$$

$$V_o = -V_i$$

3. Select R_1, R_2, and R_3.

$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

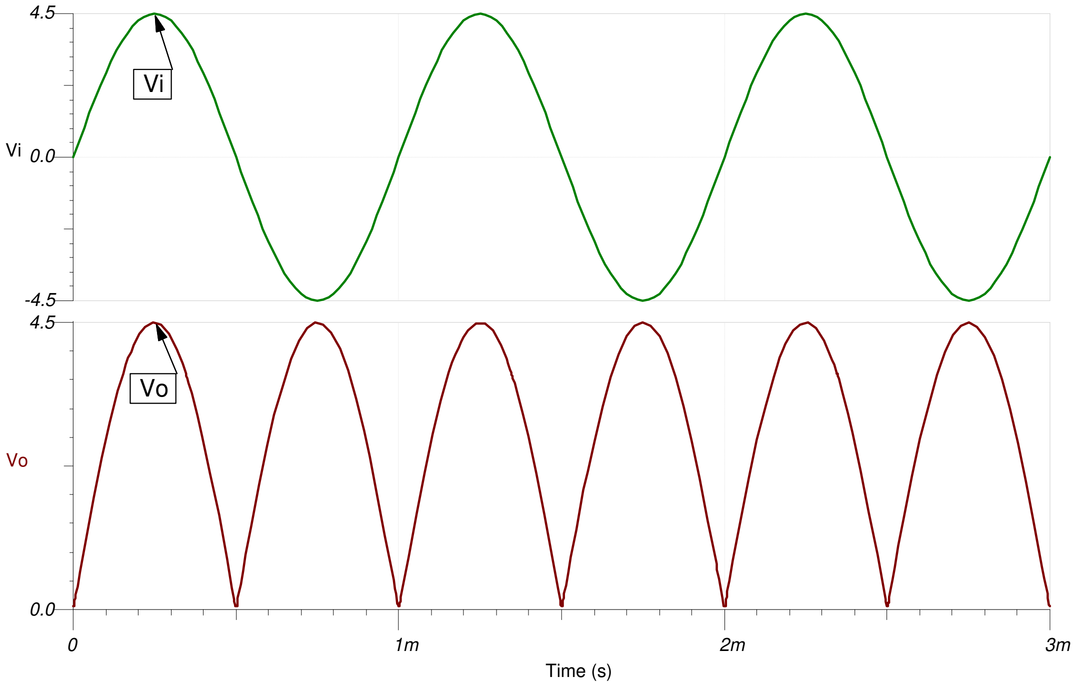
If $R_2 = R_1$ then $V_o = -V_i$

Set $R_1 = R_2 = R_3 = 1k\Omega$

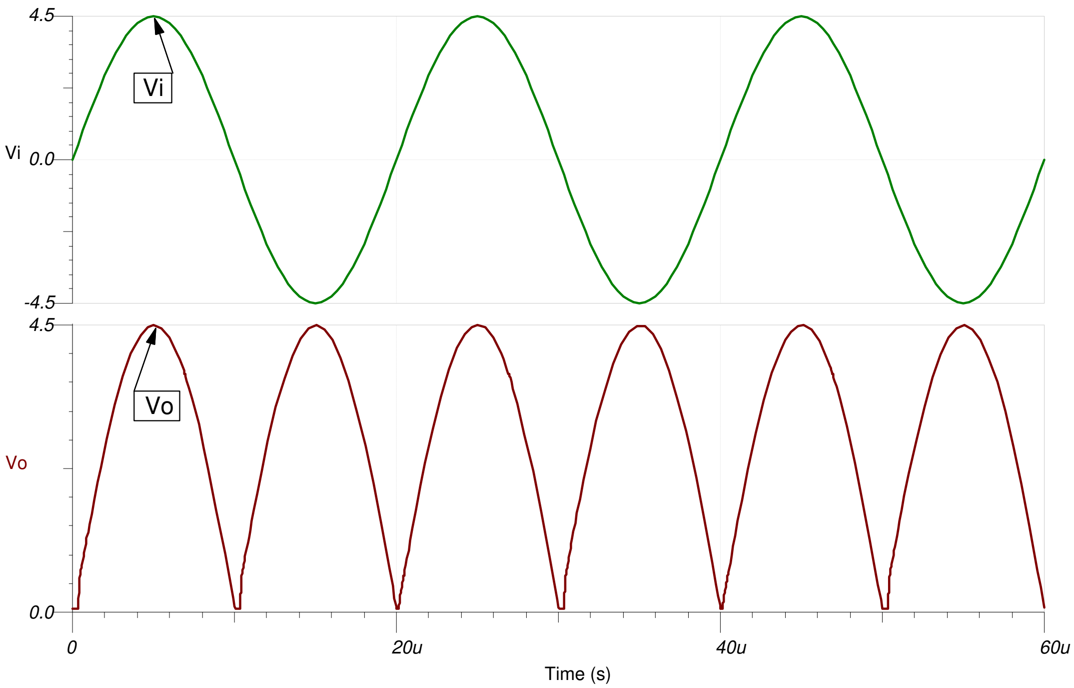
Design Simulations

Transient Simulation Results

A 1-kHz, 9-V_{pp} sine wave yields a 4.5-V_{pp} output sine wave.



A 50-kHz, 9-V_{pp} sine wave yields a 4.5-V_{pp} output sine wave.



Design References

1. See *Analog Engineer's Circuit Cookbooks* for the comprehensive TI circuit library.
2. SPICE Simulation File SBOC529.
3. TI Precision Labs
4. See the *Single-Supply Low-Input Voltage Optimized Precision Full-Wave Rectifier Reference Design*.

Design Featured Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	0.30mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9062	

Design Alternate Op Amps

	OPA322	OPA350
V_{ss}	1.8V to 5.5V	2.7V to 5.5V
V_{inCM}	Rail–to–rail	Rail–to–rail
V_{out}	Rail–to–rail	Rail–to–rail
V_{os}	2mV	0.15mV
I_q	1.9mA	5.2mA
I_b	10pA	0.5pA
UGBW	20MHz	38MHz
SR	10V/µs	22V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/OPA322	www.ti.com/product/OPA350

Full-Wave Rectifier Circuit

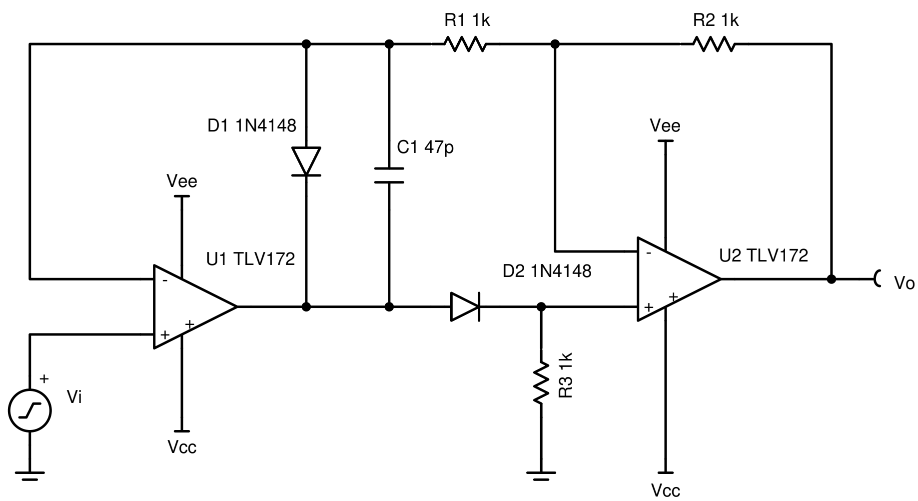
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
±25 mV	±10 V	25 mV	10 V	15 V	–15 V	0 V

Design Description

This absolute value circuit can turn alternating current (AC) signals to single polarity signals. This circuit functions with limited distortion for ±10 V input signals at frequencies up to 50 kHz and for signals as small as ±25 mV at frequencies up to 1 kHz.



Design Notes

1. Be sure to select an op amp with sufficient bandwidth and a high slew rate.
2. For greater precision look for an op amp with low offset voltage, low noise, and low total harmonic distortion (THD).
3. The resistors were selected to be 0.1% tolerance to reduce gain error.
4. Selecting too large of a capacitor C_1 will cause large distortion on the transition edges when the input signal changes polarity. C_1 may not be required for all op amps.
5. Use a fast switching diode.

Design Steps

1. Select gain resistors.
   a. Gain for positive input signals.

   $$\frac{V_o}{V_i} = 1\frac{V}{V}$$

   b. Gain for negative input signals.

   $$\frac{V_o}{V_i} = -\frac{R_2}{R_1} = -1\frac{V}{V}$$

2. Select R_1 and R_2 to reduce thermal noise and to minimize voltage drops due to the reverse leakage current of the diode. These resistors will appear as loads to U_1 and U_2 during negative input signals.

   $$R_1 = R_2 = 1\ \ k\Omega$$

3. R_3 biases the non-inverting node of U_2 to GND during negative input signals. Select R_3 to be the same value as R_1 and R_2. U_1 must be able to drive the R_3 load during positive input signals.

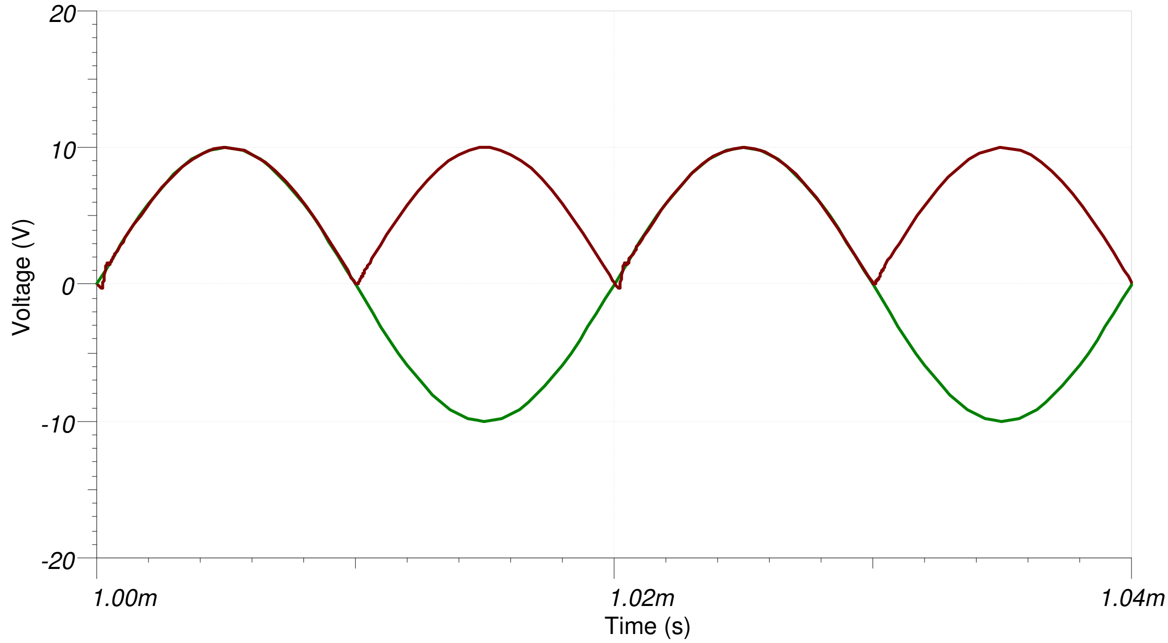
   $$R_3 = 1\ \ k\Omega$$

4. Select C_1 based on the desired transient response. See the *Design Reference* section for more information.

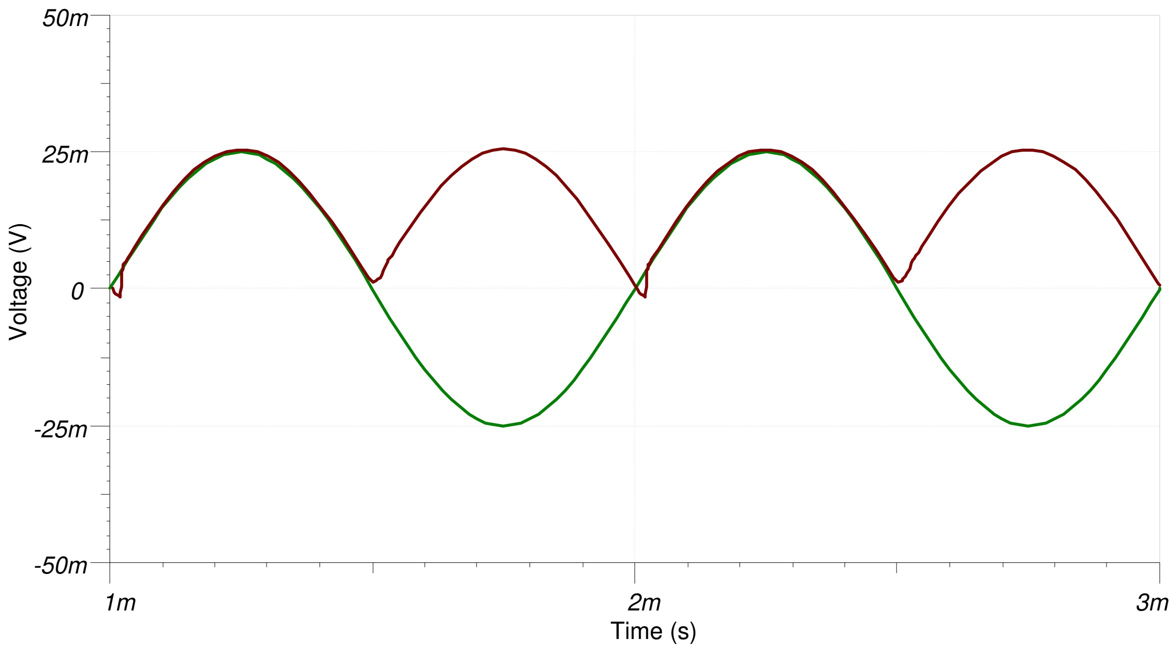
   $$C_1 = 47pF$$

Design Simulations

Transient Simulation Results



±10 V at 50 kHz Input



±25 mV at 1 kHz Input

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC517.

See TIPD139, Prevision Full-Wave Rectifier, Dual-Supply.

Design Featured Op Amp

TLV172	
V_{cc}	4.5 V to 36 V
V_{inCM}	V_{ee} to (V_{cc}–2 V)
V_{out}	Rail-to-rail
V_{os}	0.5 mV
I_q	1.6 mA/Ch
I_b	10 pA
UGBW	10 MHz
SR	10 V/µs
#Channels	1, 2, and 4
TLV172	

Design Alternate Op Amp

OPA197	
V_{cc}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25 µV
I_q	1 mA/Ch
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA197	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 1, 2019 — Page

- Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page and Spice simulation file.......... 1

Analog Engineer's Circuit

Single-Supply, Low-Input Voltage, Full-Wave Rectifier Circuit

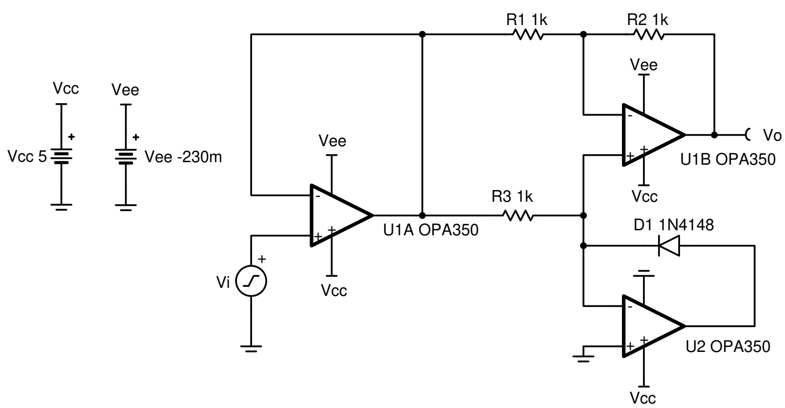
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
5 mVpp	400 mVpp	2.5 mVpp	200 mVpp	5 V	–0.23 V	0 V

Design Description

This single-supply precision absolute value circuit is optimized for low-input voltages. It is designed to function up to 50 kHz and has excellent linearity at signal levels as low as 5 mVpp. The design uses a negative charge pump (such as LM7705) on the negative op amp supply rails to maintain linearity with signal levels near 0 V.

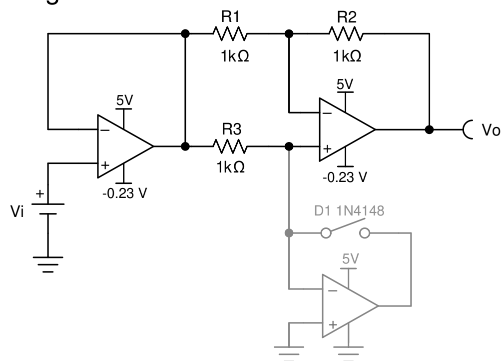


Design Notes

1. Observe common-mode and output swing limitations of op amps.
2. R_3 should be sized small enough that the leakage current from D_1 does not cause errors in positive input cycles while ensuring the op amp can drive the load.
3. Use a fast switching diode for D_1.
4. Removing the input buffer will allow for input signals with peak-to-peak values twice as large as the supply voltage at the expense of lower input impedance and slight gain error.
5. Use precision resistors to minimize gain error.

Design Steps

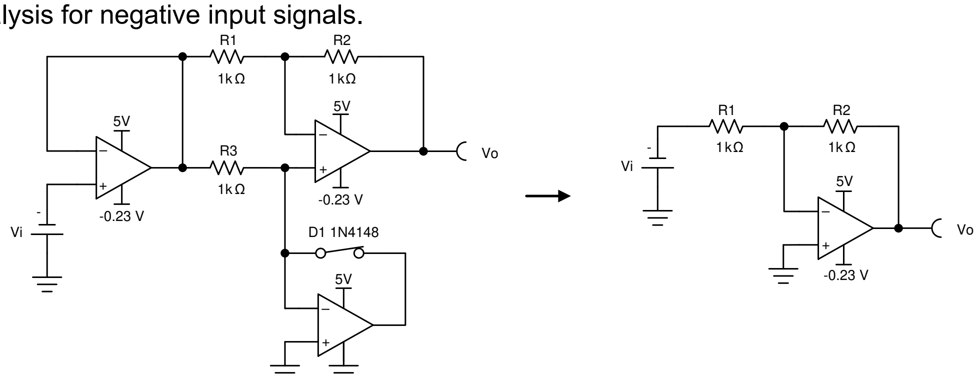
1. Circuit analysis for positive input signals.



$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1}\right) + \left(1 + \frac{R_2}{R_1}\right) = 1$$

$$V_o = V_i$$

2. Circuit analysis for negative input signals.



$$\frac{V_o}{V_i} = \left(-\frac{R_2}{R_1}\right) = -1$$

$$V_o = -V_i$$

3. Select R_1, R_2, and R_3.

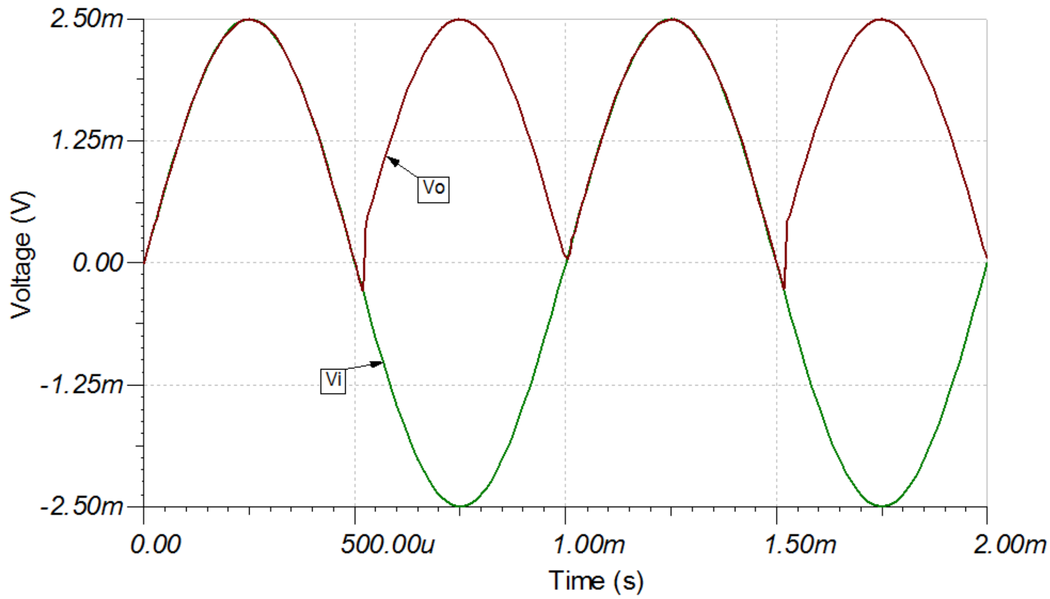
$$\frac{V_o}{V_i} = -\frac{R_2}{R_1}$$

$$\text{If } R_2 = R_1 \quad \text{then } V_o = -V_i$$

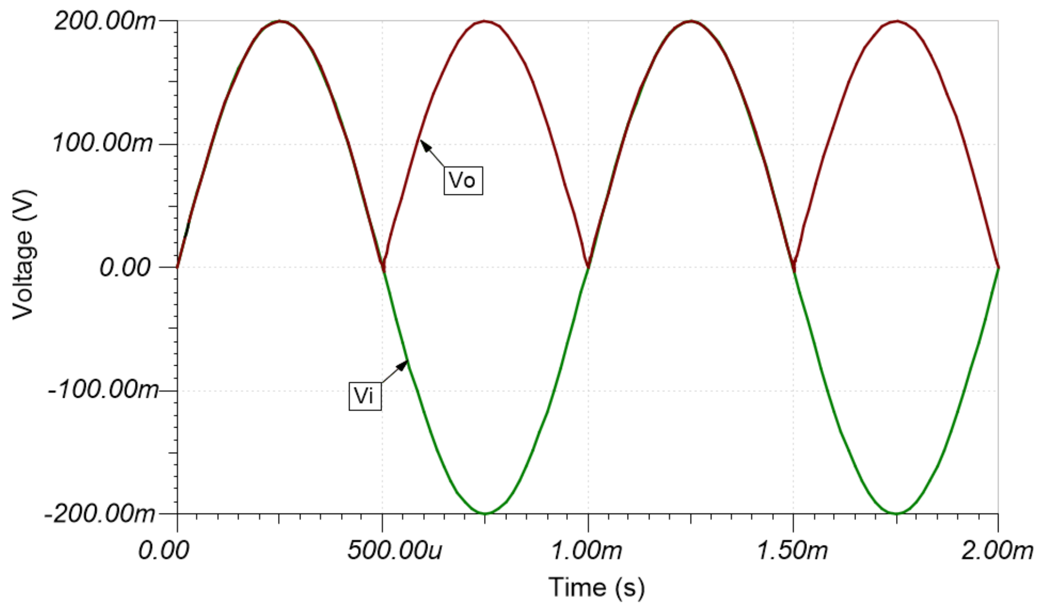
$$\text{Set } R_1 = R_2 = R_3 = 1 \quad k\Omega$$

Design Simulations

Transient Simulation Results



5 mVpp at 1 kHz Input



400 mVpp at 1 kHz Input

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC506.

See TIPD124, Single-Supply Low-Input Voltage Optimized Precision Full-Wave Rectifier Reference Design.

Design Featured Op Amp

OPA350	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	150 µV
I_q	5.2 mA/Ch
I_b	0.5 pA
UGBW	38 MHz
SR	22 V/µs
#Channels	1, 2, and 4
OPA350	

Design Alternate Op Amp

OPA353	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	3 mV
I_q	5.2 mA
I_b	0.5 pA
UGBW	44 MHz
SR	22 V/µs
#Channels	1, 2, and 4
OPA353	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file... 1

Low-pass, filtered, non-inverting amplifier circuit

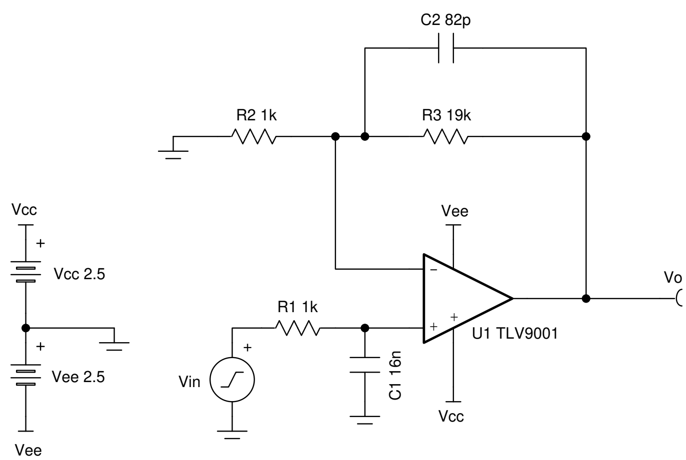
Amplifiers

Design Goals

Input		Output		BW	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f_c	V_{cc}	V_{ee}
–0.1V	0.1V	–2V	2V	10kHz	2.5V	–2.5V

Design Description

This low-pass non-inverting circuit amplifies the signal level by 20V/V (26dB) and filters the signal by setting the pole at 10kHz. Components R_1 and C_1 create a low-pass filter on the non-inverting pin. The frequency response of this circuit is the same as that of a passive RC filter, except that the output is amplified by the pass-band gain of the amplifier. Components C_2 and R_3 are used to set the cutoff frequency, $f_{c,}$ of the non-inverting amplifier.



Design Notes

1. The common-mode voltage is equal to the input voltage applied to the non-inverting input of the op amp.
2. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
3. Set the pole frequency created by R_3 / C_2 to be ten times higher than the pole created by R_1 / C_1 to achieve a single poll roll-off that is dominated by R_1 / C_1. If the filter pairs R_1 / C_1 and R_3 / C_2 have the same pole frequency, the gain will be reduced by 6dB at the cutoff frequency. Also the gain decreases at a rate of –40dB/dec until the response reaches 0dB, after which the slope changes to –20dB/dec until the op amp runs out of bandwidth.
4. C_2 limits the bandwidth of the non-inverting gain stage.
5. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on an op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the *Design References* section.

Design Steps

The DC transfer function of this circuit follows:

$$V_o = V_{in} \times \left(1 + \frac{R_3}{R_2}\right)$$

1. Calculate the gain.

$$\text{Gain} = \frac{V_{oMax} - V_{oMin}}{V_{iMax} - V_{iMin}} = \frac{2V - (-2V)}{0.1V - (-0.1V)} = 20\frac{V}{V}$$

2. Calculate values for R_2 and R_3.

$$\text{Gain} = 1 + \frac{R_3}{R_2} = 20\frac{V}{V} \rightarrow \quad (26dB)$$

Choose $R_2 = 1k\Omega$:

$$R_3 = (\text{Gain} - 1) \times R_2 = 19k\Omega$$

3. Calculate the component values R_1 and C_1 to set the cutoff frequency, f_c. Pick the value of R_1 and then calculate C_1 to set the location of f_c.

Choose $R_1 = 1k\Omega$:

$$C_1 = \frac{1}{2\pi \times R_1 \times f_c} = \frac{1}{2\pi \times 1k\Omega \times 10kHz} = 15.92nF \approx 16nF \text{ (Standard Value)}$$

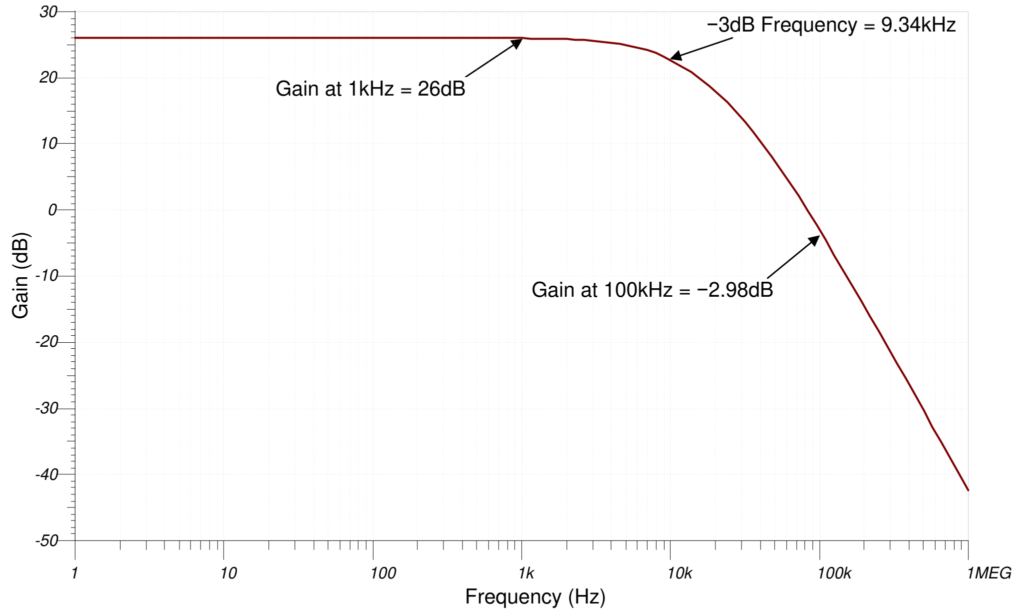
4. Calculate C_2 value to set the cutoff frequency (f_c) of the op amp. Select the corner frequency to be at least ten times larger than f_c.

$f_c = 10kHz;\ 10 \times f_c = 100kHz$

$$C_2 = \frac{1}{2\pi \times R_3 \times 100kHz} = \frac{1}{2\pi \times 19k\Omega \times 100kHz} = 83.77pF \approx 82pF \text{ (Standard Value)}$$

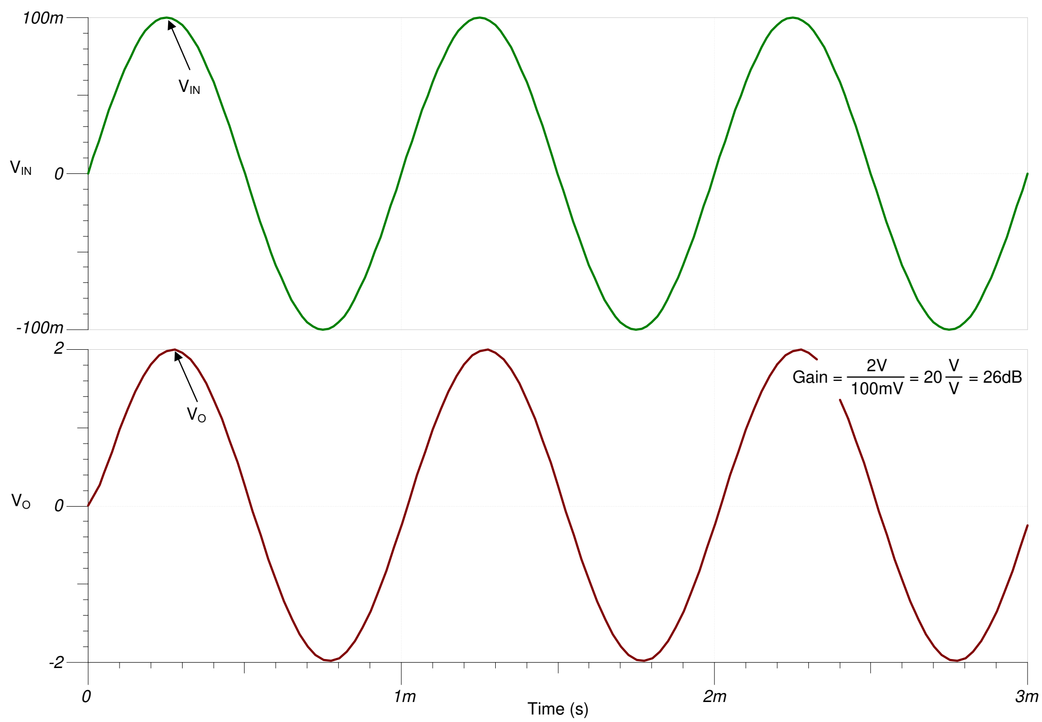
Design Simulations

AC Simulation Results

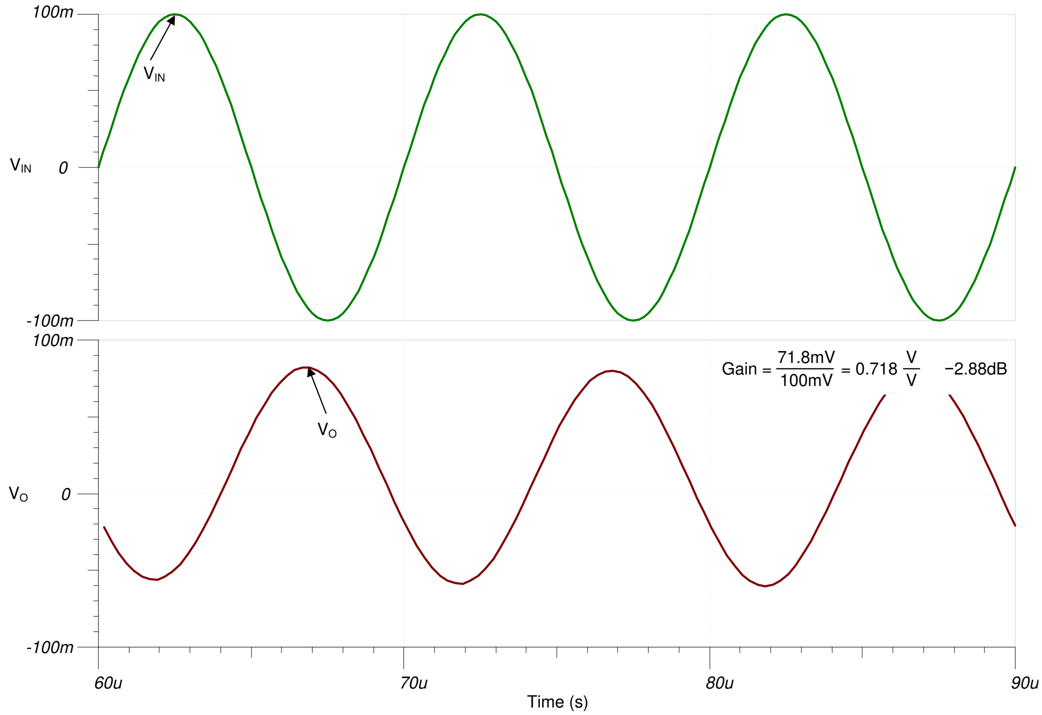


Transient Simulation Results

A 1-kHz, 0.2-V_{PP} sine wave yields a 4-V_{PP} output sine wave.



A 100-kHz, 0.2-V_{PP} sine wave yields a 0.071-V_{PP} output sine wave.



Design References

1. See Analog Engineer's Circuit Cookbooks for the comprehensive TI circuit library.
2. SPICE Simulation File SBOC528.
3. *TI Precision Labs*
4. See the *AC Coupled, Single-Supply, Inverting and Non-inverting Amplifier Reference Design*.

Design Featured Op Amp

TLV9001	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4mV
I_q	60µA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1,2,4
www.ti.com/product/TLV9001	

Design Alternate Op Amp

OPA375	
V_{ss}	2.25V to 5.5V
V_{inCM}	V_{ee} to V_{cc} – 1.2V
V_{out}	Rail-to-rail
V_{os}	0.15mV
I_q	890µA
I_b	10pA
UGBW	10MHz
SR	4.75V/µs
#Channels	1,2,4
www.ti.com/product/OPA375	

Analog Engineer's Circuit

Non-Inverting Op Amp with Non-Inverting Positive Reference Voltage Circuit

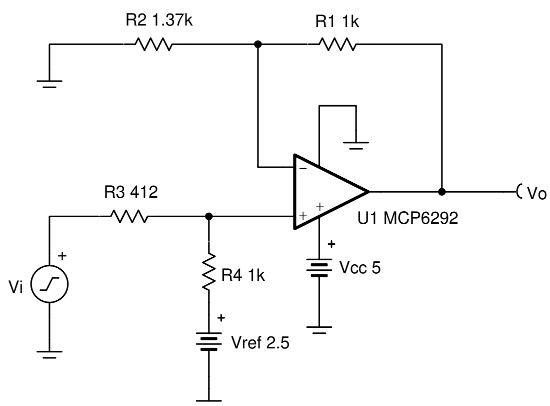
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–1 V	3 V	0.05 V	4.95 V	5 V	0 V	2.5 V

Design Description

This design uses a non-inverting amplifier with a non-inverting positive reference to translate an input signal of –1 V to 3 V to an output voltage of 0.05 V to 4.95 V. This circuit can be used to translate a sensor output voltage with a positive slope and negative offset to a usable ADC input voltage range.



Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Check op amp input common mode voltage range.
3. V_{ref} output must be low impedance.
4. Input impedance of the circuit is equal to the sum of R_3 and R_4.
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100 kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier.
7. Adding a capacitor in parallel with R_1 will improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = V_i \times \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right) + V_{ref} \times \left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$

1. Calculate the gain of the input voltage to produce the desired output swing.

$$G_{input} = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$
$$V_{o\_max} - V_{o\_min} = (V_{i\_max} - V_{i\_min})\left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$
$$\frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$
$$\frac{4.95V - 0.05V}{3V - (-1V)} = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$
$$1.225V = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$

2. Select a value for R_1 and R_4 and insert the values into the previous equation. The other two resistor values must be solved using a system of equations. The proper output swing and offset voltage cannot be calculated if more than two variables are selected.

$$R_1 = R_4 = 1\ \ k\Omega$$
$$1.225V = \left(\frac{1\ \ k\Omega}{R_3 + 1\ \ k\Omega}\right)\left(\frac{1\ \ k\Omega + R_2}{R_2}\right)$$

3. Solve the previous equation for R_3 in terms of R_2.

$$R_3 = \frac{1\ \ M\Omega + (1\ \ k\Omega \times R_2)}{1.225 \times R_2} - 1\ \ k\Omega$$

4. Select any point along the transfer function within the linear output range of the amplifier to set the proper offset voltage at the output (for example, the minimum input and output voltage).

$$V_{o\_min} = V_{i\_min} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right) + V_{ref} \times \left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$
$$0.05V = -1\ \ V \times \left(\frac{1\ \ k\Omega}{R_3 + 1\ \ k\Omega}\right)\left(\frac{1\ \ k\Omega + R_2}{R_2}\right) + 2.5V \times \left(\frac{R_3}{R_3 + 1\ \ k\Omega}\right)\left(\frac{1\ \ k\Omega + R_2}{R_2}\right)$$

5. Insert R_3 into the equation from step 1 and solve for R_2.

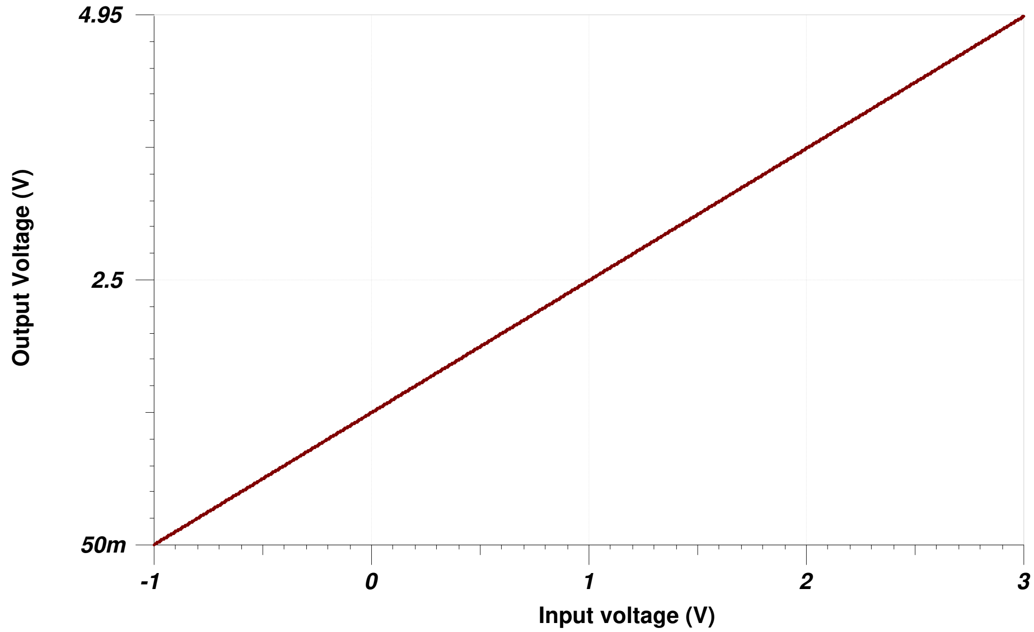
$$0.05V = -1\ \ V \times \left(\frac{1\ \ k\Omega}{\frac{1\ \ M\Omega + 1\ \ k\Omega \times R_2}{1.225 \times R_2} - 1\ \ k\Omega + 1\ \ k\Omega}\right)\left(\frac{1\ \ k\Omega + R_2}{R_2}\right) + 2.5V \times \left(\frac{\frac{1\ \ M\Omega + 1\ \ k\Omega \times R_2}{1.225 \times R_2} - 1\ \ k\Omega}{\frac{1\ \ M\Omega + 1\ \ k\Omega \times R_2}{1.225 \times R_2} - 1\ \ k\Omega + 1\ \ k\Omega}\right)$$
$$\left(\frac{1\ \ k\Omega + R_2}{R_2}\right)$$
$$R_2 = 1360.5\Omega \quad \approx 1370\Omega$$

6. Insert R_2 into the equation from step 1 to solve for R_3.

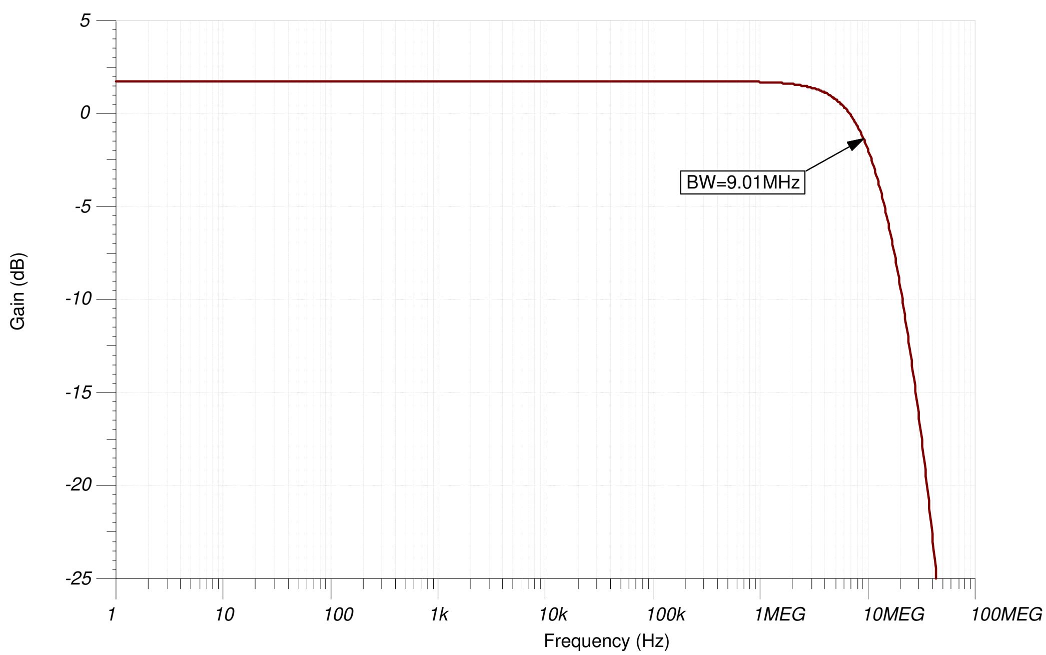
$$R_3 = \frac{1\ \ M\Omega + 1\ \ k\Omega \times (1370\Omega)}{1.225 \times (1370\Omega)} - 1\ \ k\Omega$$
$$R_3 = 412.18\Omega \approx 412\Omega$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC513.

See *Designing Gain and Offset in Thirty Seconds*.

Design Featured Op Amp

MCP6292	
V_{ss}	2.4 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3 mV
I_q	600 µA
I_b	1 pA
UGBW	10 MHz
SR	6.5 V/µs
#Channels	1, 2, and 4
MCP6292	

Design Alternate Op Amp

OPA388	
V_{ss}	2.5 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.25 µV
I_q	1.9 mA
I_b	30 pA
UGBW	10 MHz
SR	5 V/µs
#Channels	1, 2, and 4
OPA388	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.. 1

Inverting Amplifier With T-Network Feedback Circuit

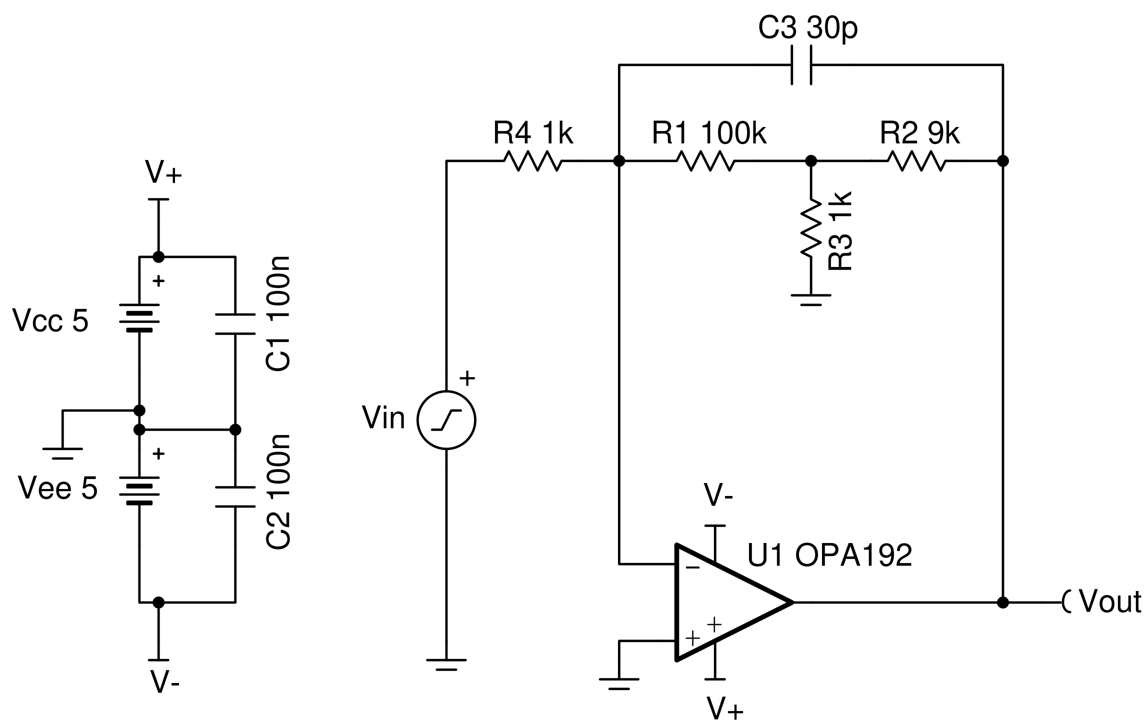
Amplifiers

Design Goals

Input		Output		BW	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}
–2.5mV	2.5mV	–2.5V	2.5V	5kHz	5V	–5V

Design Description

This design inverts the input signal, V_{in}, and applies a signal gain of 1000V/V or 60dB. The inverting amplifier with T-feedback network can be used to obtain a high gain without a small value for R_4 or very large values for the feedback resistors.



Design Notes

1. C_3 and the equivalent resistance of feedback resistors set the cutoff frequency, f_p.
2. The common-mode voltage in this circuit does not vary with input voltage.
3. Using high-value resistors can degrade the phase margin and increase noise.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Due to the high gain of the circuit, be sure to use an op amp with sufficient gain bandwidth product. Remember to use the noise gain when calculating bandwidth. Use precision, or low offset, devices due to the high gain of the circuit.
6. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth see the *Design References* section.

Design Steps

1. Calculate required gain.

$$\text{Gain} = \frac{V_{oMax} - V_{oMin}}{V_{iMax} - V_{iMin}} = \frac{2.5V - (-2.5V)}{2.5mV - (-2.5mV)} = 1000\frac{V}{V} = 60dB$$

2. Calculate resistor values to set the required gain.

$$\text{Gain} = \left(\frac{\frac{R_2 \times R_1}{R_3} + R_1 + R_2}{R_4}\right)$$

Choose the input resistor R_4 to be 1kΩ. To obtain a gain of 1000V/V, normally a 1-MΩ resistor would be required. A T-network allows us to use smaller resistor values in the feedback loop. Selecting R_1 to be 100kΩ and R_2 to be 9kΩ allows calculation of the value for R_3. R_2 is in the 10kΩ range so the op amp can easily drive the feedback network.

$$R_3 = \left(\frac{R_2 \times R_1}{(\text{Gain} \times R_4) - R_1 - R_2}\right) = \left(\frac{9k\Omega \times 100k\Omega}{(1000 \times 1k\Omega) - 100k\Omega - 9k\Omega}\right) = 1k\Omega$$

3. Calculate C_3 using the equivalent resistance of the feedback resistors, R_{eq}, to set the location of f_p.

$$R_{eq} = \left(\frac{R_2 \times R_1}{R_3} + R_1 + R_2\right) = \left(\frac{9k\Omega \times 100k\Omega}{1k\Omega} + 100k\Omega + 9k\Omega\right) = 1.009M\Omega$$

$$f_p = \frac{1}{2\pi \times R_{eq} \times C_3} = 5kHz$$

$$C_3 = \frac{1}{2\pi \times R_{eq} \times f_p} = \frac{1}{2\pi \times 1.009M\Omega \times 5kHz} = 31.55pF \approx 30pF \text{ (Standard Value)}$$

4. Calculate the small signal circuit bandwidth to ensure it meets the 5 kHz requirement. Be sure to use the noise gain, NG, or non-inverting gain of the circuit.

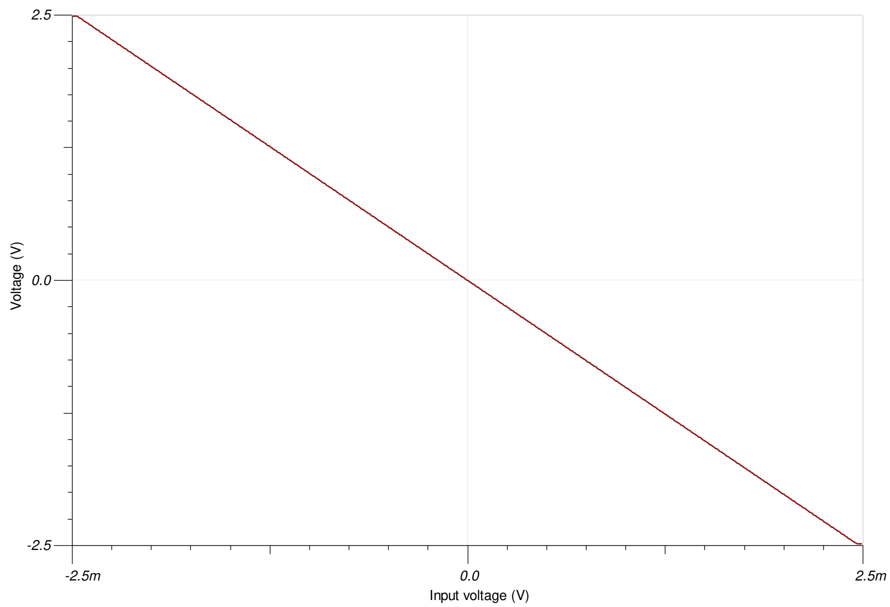
$$NG = 1 + \frac{R_{eq}}{R_4} = 1 + 1009 = 1010\frac{V}{V}$$

$$BW = \frac{GBP}{NG} = \frac{10MHz}{1010\ V/V} = 9.9kHz$$

- BW_{OPA192} = 10MHz; therefore this requirement is met.

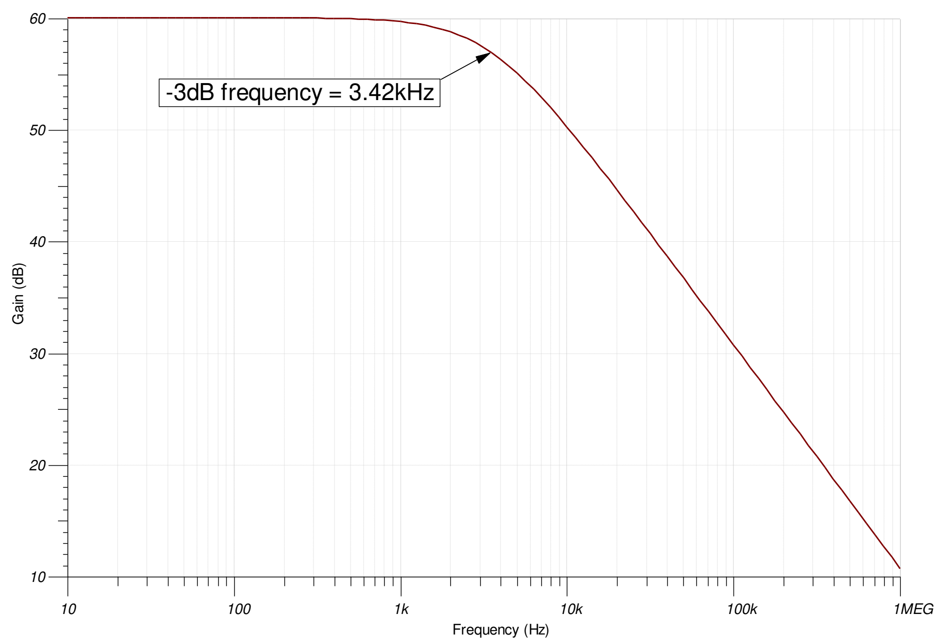
Design Simulations

DC Simulation Results

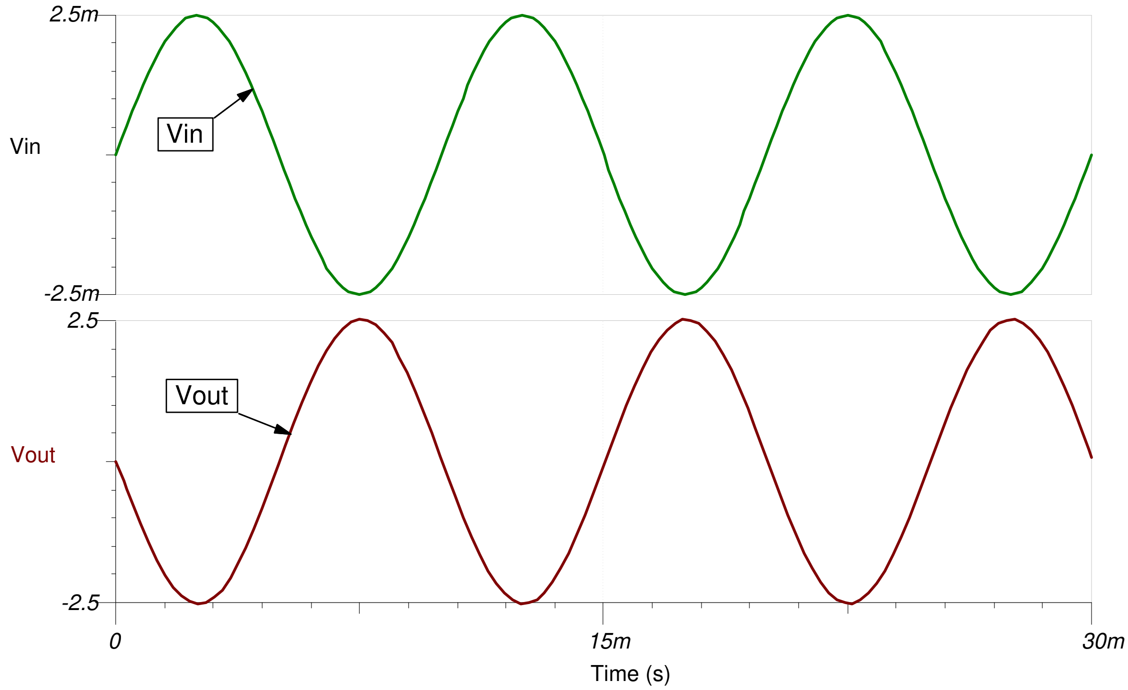


AC Simulation Results

The simulation is very close to the calculation.



Transient Simulation Results



Design References

1. See *Analog Engineer's Circuit Cookbooks* for the comprehensive TI circuit library.
2. TI Precision Labs
3. See the *1 MHz, Single-Supply, Photodiode Amplifier Reference Design*.

Design Featured Op Amp

OPA192	
V_{ss}	±2.25V to ±18V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	5µV
I_q	1mA
I_b	5pA
UGBW	10MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/OPA192	

Design Alternate Op Amp

TLV9062	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-Rail
V_{out}	Rail-to-Rail
V_{os}	0.3mV
I_q	538µA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1,2,4
www.ti.com/product/TLV9062	

Analog Engineer's Circuit

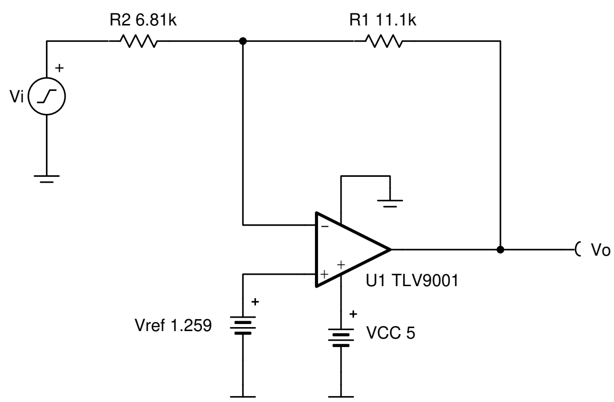
Inverting Op Amp with Non-Inverting Positive Reference Voltage Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–1 V	2 V	0.05 V	4.95 V	5 V	0 V	1.259 V

Design Description

This design uses an inverting amplifier with a non-inverting positive reference voltage to translate an input signal of –1 V to 2 V to an output voltage of 0.05 V to 4.95 V. This circuit can be used to translate a sensor output voltage with a positive slope and negative offset to a usable ADC input voltage range.



Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Amplifier common mode voltage is equal to the reference voltage.
3. V_{ref} can be created with a voltage divider.
4. Input impedance of the circuit is equal to R_2.
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100 kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1. Adding a capacitor in parallel with R_1 will also improve stability of the circuit, if high-value resistors are used.

Design Steps

$$V_o = -Vi \times \left(\frac{R_1}{R_2}\right) + V_{ref} \times \left(1 + \frac{R_1}{R_2}\right)$$

1. Calculate the gain of the input signal.

$$G_{input} = -\frac{R_1}{R_2}$$

$$V_{o\_max} - V_{o\_min} = \left(V_{i\_max} - V_{i\_min}\right)\left(-\frac{R_1}{R_2}\right)$$

$$-\frac{R_1}{R_2} = -\frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = -\frac{4.95V - 0.05V}{2V - (-1\ \ V)} = -1.633\frac{V}{V}$$

2. Select R_2 and calculate R_1.

$$R_2 = 6.81\ \ k\Omega$$

$$R_1 = G_{input} \times R_2 = 1.633\frac{V}{V} \times 6.81\ \ k\Omega = 11.123k\Omega \approx 11.1\ \ k\Omega\quad \text{(Standard Value)}$$

3. Calculate the reference voltage.

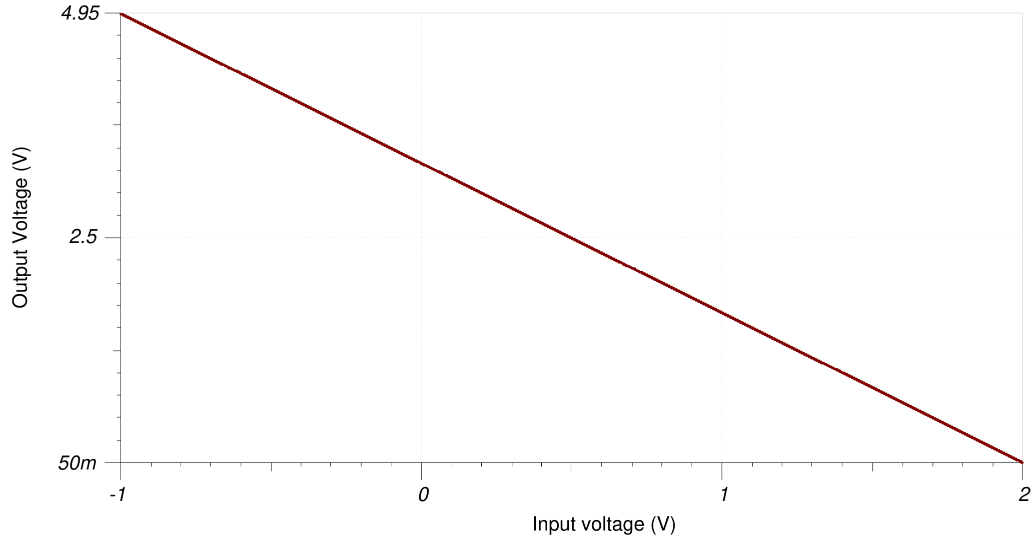
$$V_{o\_min} = -V_{i\_max} \times \left(\frac{R_1}{R_2}\right) + V_{ref} \times \left(1 + \frac{R_1}{R_2}\right)$$

$$0.05V = -2V \times \left(\frac{11.11\ \ k\Omega}{6.81\ \ k\Omega}\right) + V_{ref} \times \left(1 + \frac{11.11\ \ k\Omega}{6.81\ \ k\Omega}\right)$$

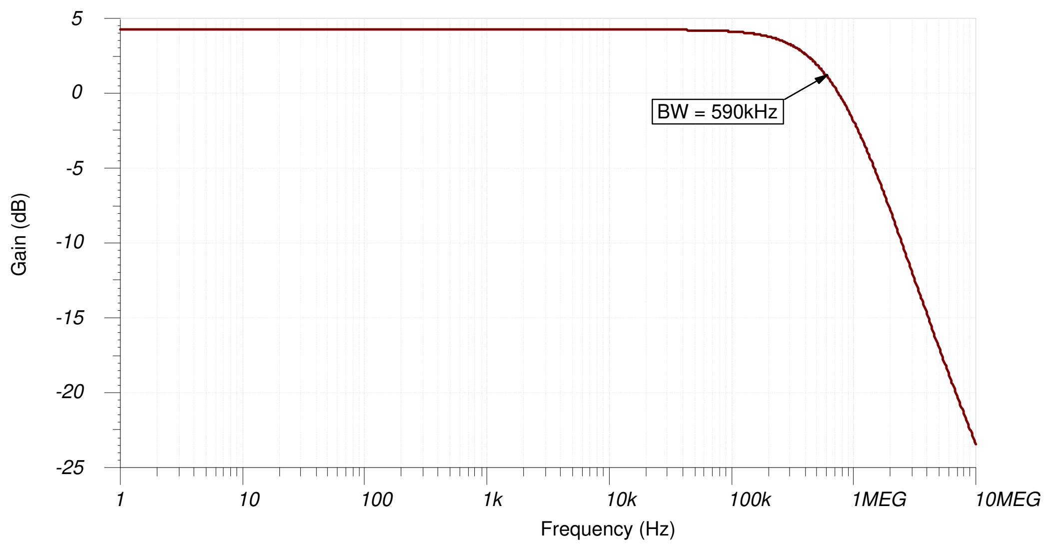
$$V_{ref} = \frac{V_{o\_min} + V_{i\_max} \times \left(\frac{R_1}{R_2}\right)}{\left(1 + \frac{R_1}{R_2}\right)} \frac{0.05V + 2V \times \left(\frac{11.11\ \ k\Omega}{6.81\ \ k\Omega}\right)}{\left(1 + \frac{11.11\ \ k\Omega}{6.81\ \ k\Omega}\right)} = 1.259V$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC514.

See *Designing Gain and Offset in Thirty Seconds*.

Design Featured Op Amp

TLV9001	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4 mV
I_q	60 µA
I_b	5 pA
UGBW	1 MHz
SR	2 V/µs
#Channels	1, 2, and 4
TLV9001	

Design Alternate Op Amp

OPA376	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	760 µA
I_b	0.2 pA
UGBW	5.5 MHz
SR	2 V/µs
#Channels	1, 2, and 4
OPA376	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.. 1

Analog Engineer's Circuit

Single-Ended Input to Differential Output Circuit Using a Fully-Differential Amplifier

Sean Cashin

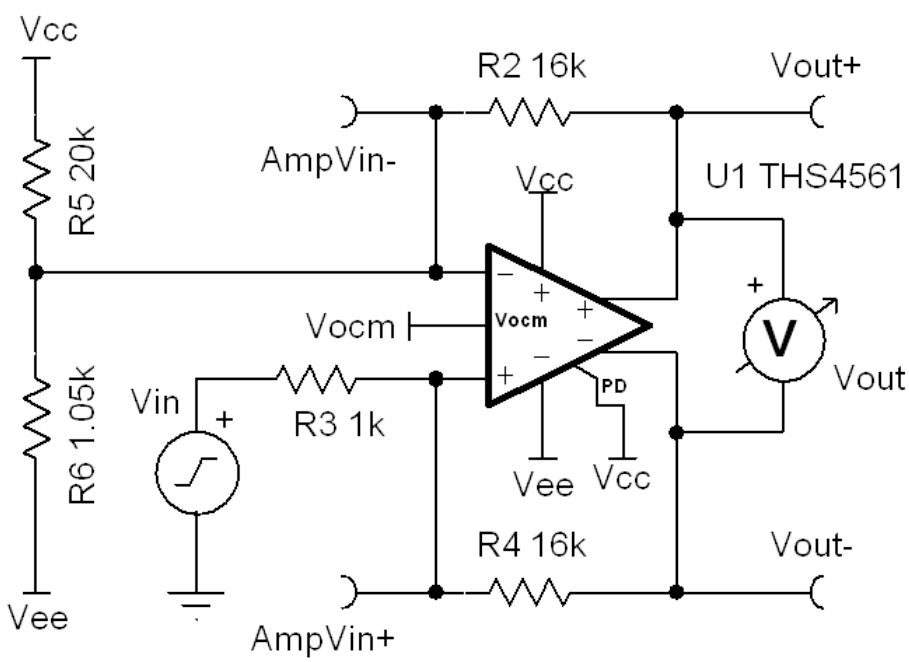
Design Goals

Input	Output	Supply	
Single-Ended	Differential	V_{cc}	V_{ee}
0 V to 1 V	16 Vpp	10 V	0 V

Output Common-Mode	3 dB Bandwidth	AC Gain (Gac)
5 V	3 MHz	16 V/V

Design Description

This design uses a fully-differential amplifier (FDA) as a single-ended input to differential output amplifier.



Design Notes

1. The ratio R_4/R_3, equal to $R_2/(R_5||R_6)$, sets the gain of the amplifier.
2. The main difference between a single-ended input and a differential input is that the available input swing is only half. This is because one of the input voltages is fixed at a reference.
3. It is recommended to set this reference to mid-input signal range, rather than the min-input, to induce polarity reversal in the measured differential input. This preserves the ability of the outputs to crossover, which provides the doubling of output swing possible with an FDA.
4. The impedance of the reference voltage must be equal to the signal input resistor. This can be done by creating a resistor divider with a Thevnin equivalent of the correct reference voltage and impedance.

Design Steps

- Find the resistor divider with that produces a 0.5V, 1-kΩ reference from Vs = 10V.

$$\frac{R_6}{R_5+R_6} \quad F \quad \frac{0.5V}{10V} \qquad \frac{R_5 \cdot R_6}{R_5+R_6} \quad E = 1\,k\Omega$$

$$R_6 \quad FR_5 + FR_6$$

$$R_6\left(1-F\right) \quad FR_5$$

$$R_5 \quad \frac{R_6\left(1-F\right)}{F}$$

$$\frac{R_6\left(1-F\right)/F \cdot R_6}{R_6\left(1-F\right)/F + R_6} \quad E$$

$$\frac{{R_6}^2 \cdot \left(1-F\right)/F}{\left(R_6/F - R_6\right) + R_6} \quad E$$

$$\frac{{R_6}^2 \cdot \left(1-F\right)/F}{R_6/F} \quad E$$

$$R_6 \cdot \left(1-F\right) \quad E$$

$$R_6 \quad \frac{E}{1-F} \quad \frac{1k\Omega}{1-0.05} = 1.05k\Omega$$

$$R_5 \quad \frac{1.05\Omega\left(1-0.05\right)}{0.05} \quad 20k\Omega$$

- Verify that the minimum input of 0 V and the maximum input of 1 V result in an output within the 9.4 V range available for V_{ocm} = 5 V.

  Since the resistor divider acts like a 0.5 V reference, the measured differential input for a 0 V V_{IN} is:

$$V_{IN} \quad 0V - 0.5V \quad -0.5V$$

- The output is:

$$-0.5V \cdot \frac{16V}{V} \quad -8V > -9.8V$$

- Likewise, for a 1 V input:

$$V_{IN} = 1V - 0.5V = 0.5V$$

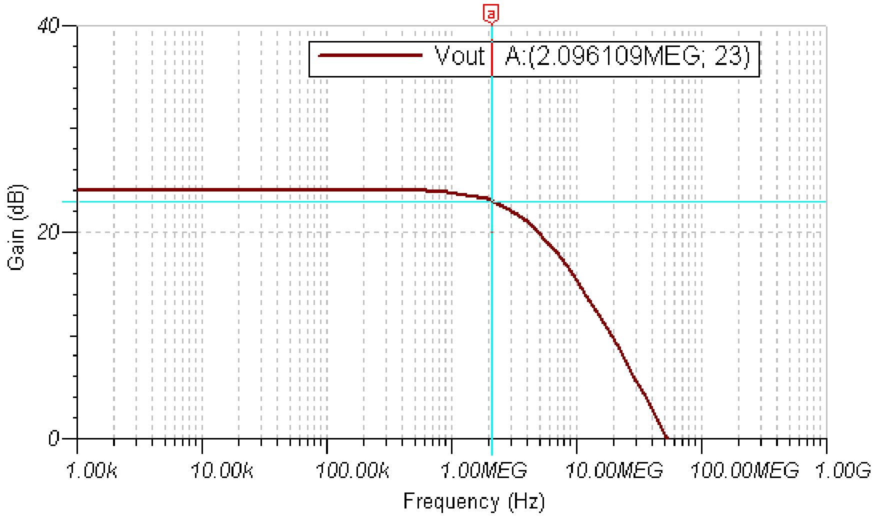
$$0.5V \cdot \frac{16V}{V} \quad 8V < 9.8V$$

Note

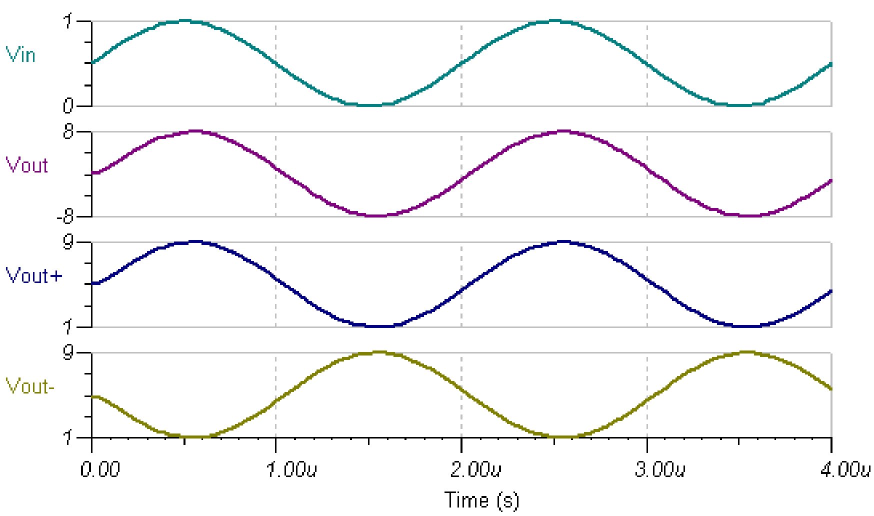
With a reference voltage of 0 V, a 1 V input results in an output voltage greater than the maximum output range of the amplifier.

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the TI Precision Labs video – Op Amps: Fully Differential Amplifiers – Designing a Front-End Circuit for Driving a Differential Input ADC, for more information.

Design Featured Op Amp

THS4561	
V_{ss}	3 V to 13.5 V
V_{inCM}	V_{ee}-0.1 V to V_{cc}-1.1 V
V_{out}	V_{ee}+0.2 V to V_{cc}-0.2
V_{os}	TBD
I_q	TBD
I_b	TBD
UGBW	70 MHz
SR	4.4 V/µs
#Channels	1
THS4561	

Design Alternate Op Amp

THS4131	
V_{ss}	5 V to 33 V
V_{inCM}	V_{ee}+1.3 V to V_{cc}-0.1 V
V_{out}	Varies
V_{os}	2 mV
I_q	14 mA
I_b	2 µA
UGBW	80 MHz
SR	52 V/µs
#Channels	1
THS4131	

Analog Engineer's Circuit

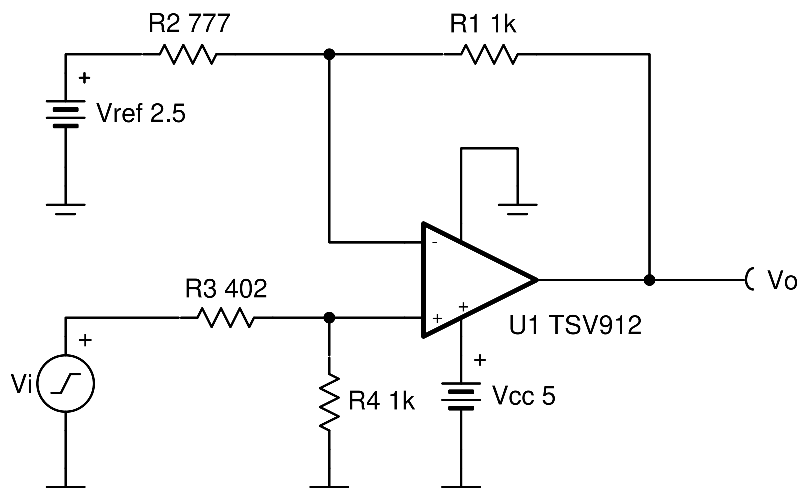
Non-Inverting Op Amp with Inverting Positive Reference Voltage Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
2 V	5 V	0.05 V	4.95 V	5 V	0 V	2.5 V

Design Description

This design uses a non-inverting amplifier with an inverting positive reference to translate an input signal of 2 V to 5 V to an output voltage of 0.05 V to 4.95 V. This circuit can be used to translate a sensor output voltage with a positive slope and offset to a usable ADC input voltage range.



Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Check op amp input common mode voltage range. The common mode voltage varies with the input voltage.
3. V_{ref} must be low impedance.
4. Input impedance of the circuit is equal to the sum of R_3 and R_4.
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100 kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier.
7. Adding a capacitor in parallel with R_1 will improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = V_i \times \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right) - V_{ref} \times \left(\frac{R_1}{R_2}\right)$$

1. Calculate the gain of the input to produce the largest output swing.

$$V_{o\_max} - V_{o\_min} = \left(V_{i\_max} - V_{i\_min}\right)\left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$

$$\frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$

$$\frac{4.95V - 0.05V}{5V - 2V} = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$

$$1.633\frac{V}{V} = \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right)$$

2. Select a value for R_1 and R_4 and insert the values into the previous equation. The other two resistor values must be solved using a system of equations. The proper output swing and offset voltage cannot be calculated if more than two variables are selected.

$$R_1 = R_4 = 1\ \ k\Omega$$

$$1.633\frac{V}{V} = \left(\frac{1\ \ k\Omega}{R_3 + 1\ \ k\Omega}\right)\left(\frac{1\ \ k\Omega + R_2}{R_2}\right)$$

3. Solve the previous equation for R_3 in terms of R_2.

$$R_3 = \frac{1\ \ M\Omega + (1\ \ k\Omega \times R_2)}{1.633 \times R_2} - 1\ \ k\Omega$$

4. Select any point along the transfer function within the linear output range of the amplifier to set the proper offset voltage at the output (for example, the minimum input and output voltage).

$$V_{o\_min} = V_{i\_min} \times \left(\frac{R_4}{R_3 + R_4}\right)\left(\frac{R_1 + R_2}{R_2}\right) - V_{ref} \times \left(\frac{R_1}{R_2}\right)$$

$$0.05V = 2V \times \left(\frac{1\ \ k\Omega}{R_3 + 1\ \ k\Omega}\right)\left(\frac{1\ \ k\Omega + R_2}{R_2}\right) - V_{ref} \times \left(\frac{1\ \ k\Omega}{R_2}\right)$$

5. Insert R_3 from step 3 into the equation from step 4 and solve for R_2.

$$0.05V = 2V \times \left(\frac{1\ \ k\Omega}{\frac{1\ \ M\Omega + 1\ \ k\Omega \times R_2}{1.633 \times R_2} - 1\ \ k\Omega + 1\ \ k\Omega}\right)\left(\frac{1\ \ k\Omega + R_2}{R_2}\right) - V_{ref} \times \left(\frac{1\ \ k\Omega}{R_2}\right)$$

$$R_2 = 777.2\Omega \approx 777\Omega$$

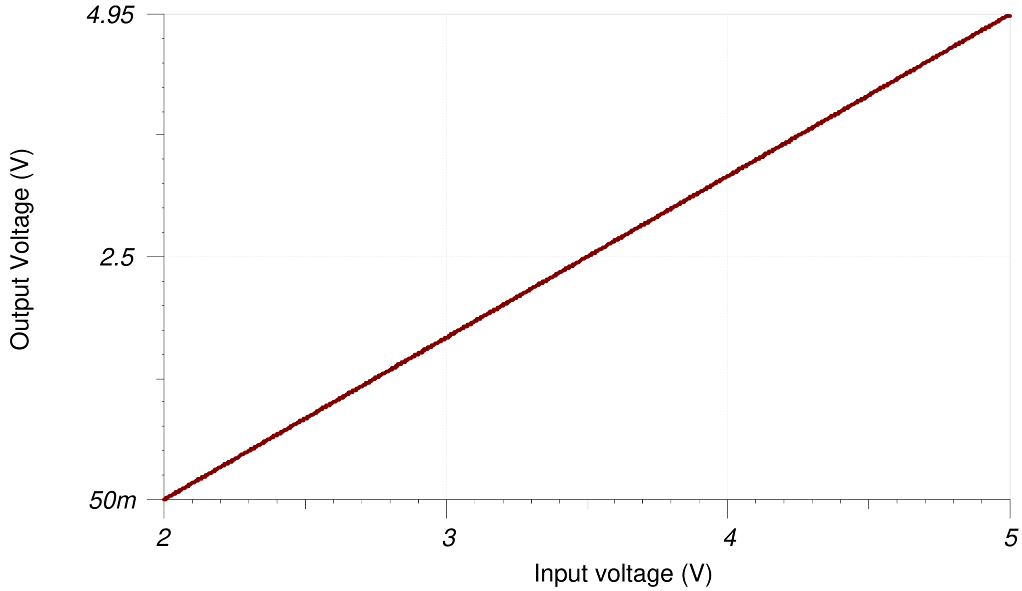
6. Insert R_2 calculation from step 5, and solve for R_3.

$$R_3 = \frac{1\ \ M\Omega + (1\ \ k\Omega \times R_2)}{1.633 \times R_2} - 1\ \ k\Omega$$

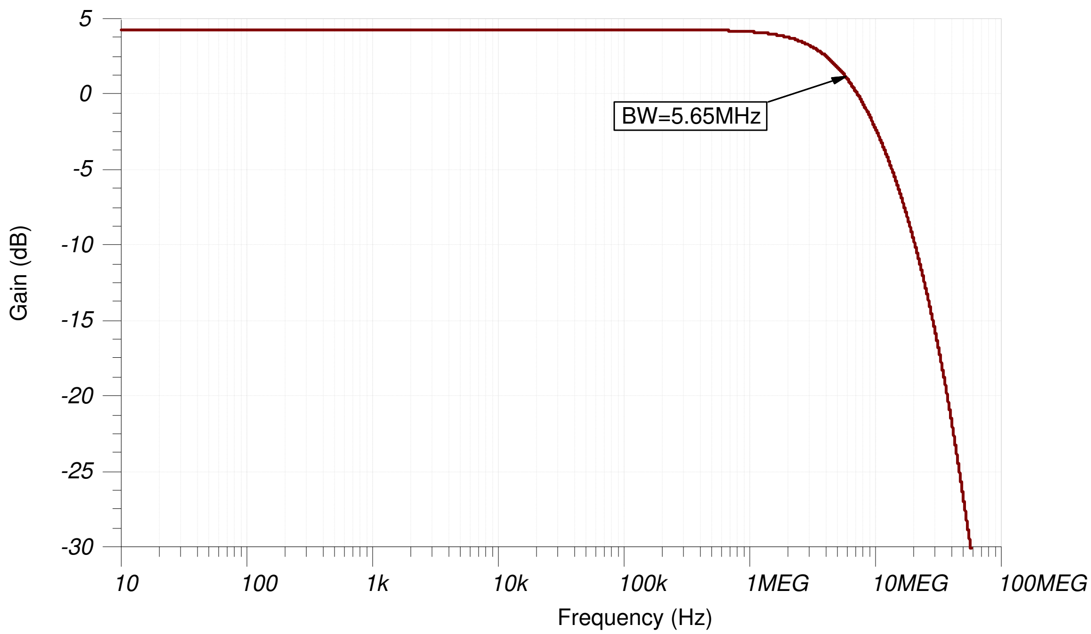
$$R_3 = \frac{1\ \ M\Omega + 1\ \ k\Omega \times (777\Omega)}{1.633 \times (777\Omega)} - 1\ \ k\Omega = 400.49\Omega \approx 402\Omega$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC512.

See *TI Precision Lab Videos on Input and Output Limitations*.

Design Featured Op Amp

TSV912	
V_{ss}	2.5 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3 mV
I_q	550 µA
I_b	1 pA
UGBW	8 MHz
SR	4.5 V/µs
#Channels	1, 2, and 4
TSV912	

Design Alternate Op Amp

OPA191	
V_{ss}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	140 µA/Ch
I_b	5 pA
UGBW	2.5 MHz
SR	5.5 V/µs
#Channels	1, 2, and 4
OPA191	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 4, 2019 to February 5, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file........ 1

Analog Engineer's Circuit

Single-Ended Input to Differential Output Circuit

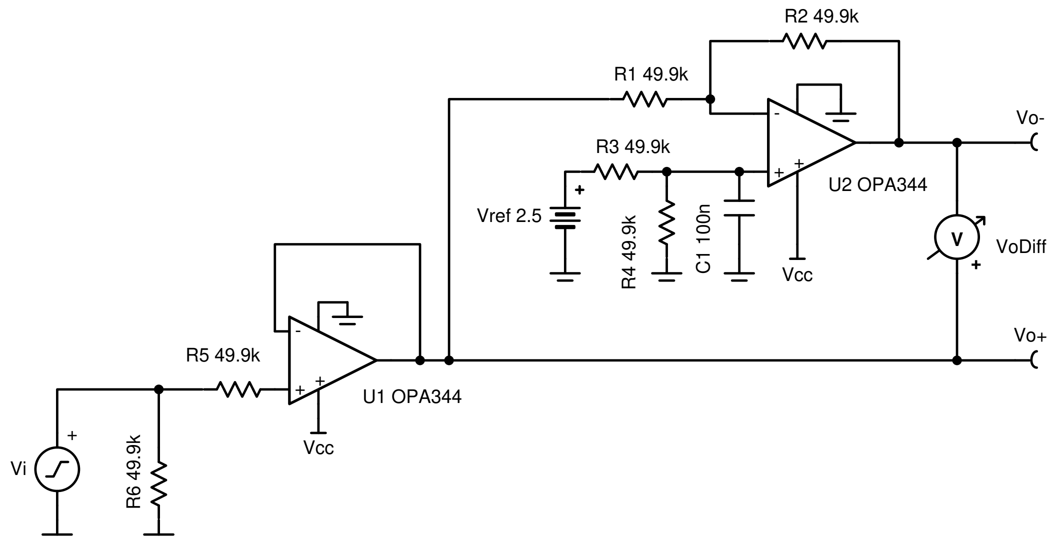
TEXAS INSTRUMENTS

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	$V_{oDiffMin}$	$V_{oDiffMax}$	V_{cc}	V_{ee}	V_{ref}
0.1 V	2.4 V	–2.3 V	2.3 V	2.7 V	0 V	2.5 V

Design Description

This circuit converts a single ended input of 0.1 V to 2.4 V into a differential output of ±2.3 V on a single 2.7 V supply. The input and output ranges can be scaled as necessary as long as the op amp input common-mode range and output swing limits are met.



Design Notes

1. Op amps with rail-to-rail input and output will maximize the input and output range of the circuit.
2. Op amps with low V_{os} and offset drift will reduce DC errors.
3. Use low tolerance resistors to minimize gain error.
4. Set output range based on linear output swing (see A_{ol} specification).
5. Keep feedback resistors low or add capacitor in parallel with R_2 for stability.

Design Steps

1. Buffer V_i signal to generate V_{o+}.

$$V_{O+} = V_i$$

2. Invert and level shift V_{o+} using a difference amplifier to create V_{o-}.

$$V_{o-} = (V_{ref} - V_{o+}) \times \left(\frac{R_2}{R_1}\right)$$

3. Select resistances so that the resistor noise is smaller than the amplifier broadband noise.

$$E_{nv} = 30\frac{nV}{\sqrt{Hz}} \text{ (Voltage noise from op amp)}$$

$$\text{If } R_1 = R_2 = R_3 = R_4 = 49.9k\Omega \text{ then}$$

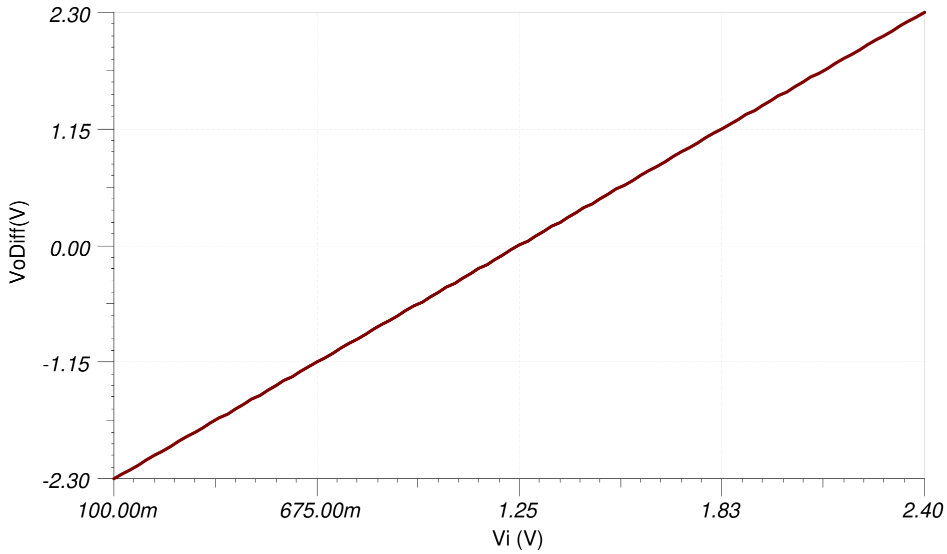
$$E_{nr} = \sqrt{\left(\sqrt{4 \times kB \times T \times (R_1 || R_2)}\right)^2 + \left(\sqrt{4 \times kB \times T \times (R_3 || R_4)}\right)^2} = 28.7\frac{nV}{\sqrt{Hz}} \ (<E_{nv})$$

4. Select resistances that protect the input of the amplifier and prevents floating inputs. To simplify the bill of materials (BOM), select R_5 = R_6.

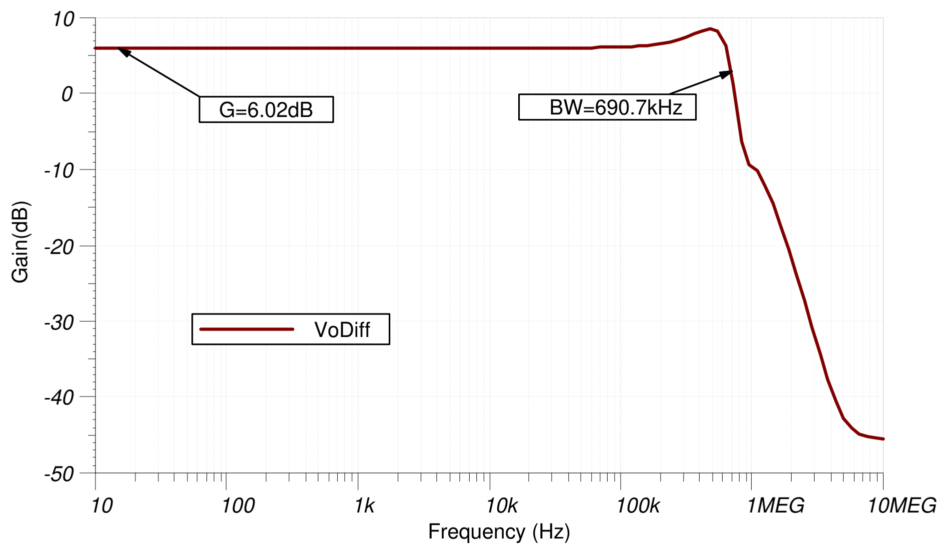
$$R_5 = R_6 = 49.9k\Omega$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC510.

See TIPD131, Single-Ended Input to Differential Output Conversion Circuit Reference Design.

Design Featured Op Amp

OPA344	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.2 mV
I_q	150 µA
I_b	0.2 pA
UGBW	1 MHz
SR	0.8 V/µs
#Channels	1, 2, and 4
OPA344	

Design Alternate Op Amp

OPA335	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	V_{ee}–0.1 V to V_{cc}–1.5 V
V_{out}	Rail-to-rail
V_{os}	1 µV
I_q	285 µA/Ch
I_b	70 pA
UGBW	2 MHz
SR	1.6 V/µs
#Channels	1 and 2
OPA335	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file............ 1

Analog Engineer's Circuit

Differential Input to Differential Output Circuit Using a Fully-Differential Amplifier

Sean Cashin

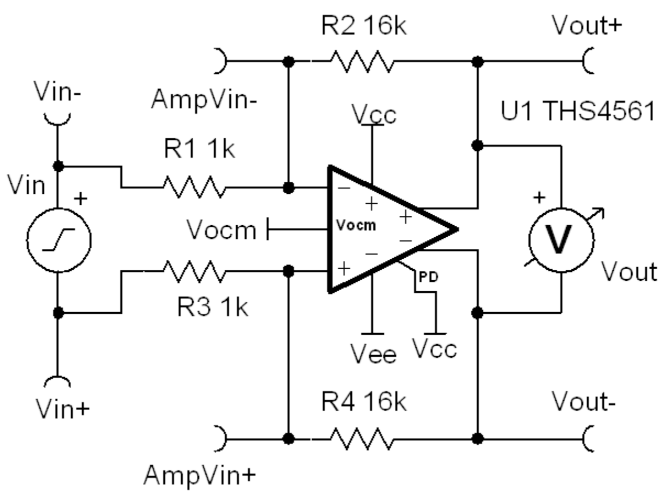
Design Goals

Input	Output	Supply	
Differential	Differential	V_{cc}	V_{ee}
1 Vpp	16 Vpp	10 V	0 V

Output Common-Mode	3 dB Bandwidth	AC Gain (Gac)
5 V	3 MHz	16 V/V

Design Description

This design uses a fully differential amplifier (FDA) as a differential input to differential output amplifier.



Design Notes

1. The ratio R2/R1, equal to R4/R3, sets the gain of the amplifier.
2. For a given supply, the output swing for and FDA is twice that of a single ended amplifier. This is because a fully differential amplifier swings both terminals of the output, instead of swinging one and fixing the other to either ground or a Vref. The minimum voltage of an FDA is therefore achieved when Vout+ is held at the negative rail and Vout- is held at the positive rail, and the maximum is achieved when Vout+ is held at the positive rail and Vout- is held at the negative rail.
3. FDAs are useful for noise sensitive signals, since noise coupling equally into both inputs will not be amplified, as is the case in a single ended signal referenced to ground.
4. The output voltages will be centered about the output common-mode voltage set by Vocm.
5. Both feedback paths should be kept symmetrical in layout.

Design Steps

- Set the ratio R2/ R1 to select the AC voltage gain. To keep the feedback paths balanced,

  $$R_1 = R_3 = 1k\Omega \text{ (Standard Value)}$$

  $$R_2 = R_4 = R_1 \cdot (G_{AC}) = 1k\Omega \cdot \left(16\frac{V}{V}\right) = 16k\Omega \text{ (Standard Value)}$$

- Given the output rails of 9.8 V and 0.2 V for Vs = 10 V, verify that 16 Vpp falls within the output range available for V_{ocm} = 5 V.

  In normal operation:

  $$AmpV_{IN+} = AmpV_{IN-}$$
  $$V_{OUT+} - V_{ocm} = V_{ocm} - V_{OUT-}$$
  $$V_{OUT} = V_{OUT+} - V_{OUT-}$$

- Rearrange to solve for each output voltage in edge conditions

  $$V_{OUT-} = 2V_{ocm} - V_{OUT+}$$
  $$V_{OUT-} = V_{OUT+} - V_{OUT}$$
  $$2V_{OUT+} = 2V_{ocm} + V_{OUT}$$
  $$V_{OUT+} = V_{ocm} + \frac{V_{OUT}}{2}$$
  $$V_{OUT-} = V_{ocm} - \frac{V_{OUT}}{2}$$

- Verifying for Vout = +8 V and V_{ocm} = +5 V,

  $$V_{OUT+} = 5 + \frac{8}{2} = 9V < 9.8V$$
  $$V_{OUT-} = 5 - \frac{8}{2} = 1V > 0.2V$$

- Verifying for Vout = -8 V and V_{ocm} = +5 V,

  $$V_{OUT+} = 5 + \frac{-8}{2} = 1V > 0.2V$$
  $$V_{OUT-} = 5 - \frac{-8}{2} = 9V > 9.8V$$

  Note that the maximum swing possible is:

  $$(9.8V - 0.2V) - (0.2V - 9.8V) = 18.4V_{pp}, \text{ or } \pm 9.4V$$

- Use the input common mode voltage range of the amplifier and the feedback resistor divider to find the signal input range when the output range is 1 V to 9 V. Due to symmetry, calculation of one side is sufficient.

$$\mathrm{Min}(\mathrm{AmpV_{IN+}}) = \mathrm{Min}(\mathrm{AmpV_{IN-}}) = \mathrm{Vee} - 0.1\mathrm{V} = -0.1\mathrm{V}$$

$$\mathrm{Max}(\mathrm{AmpV_{IN+}}) = \mathrm{Max}(\mathrm{AmpV_{IN-}}) = \mathrm{Vcc} - 1.1\mathrm{V} = 8.9\mathrm{V}$$

$$\frac{\mathrm{AmpV_{IN-}} - V_{IN-}}{R_1} = \frac{V_{OUT+} - \mathrm{AmpV_{IN-}}}{R_2}$$

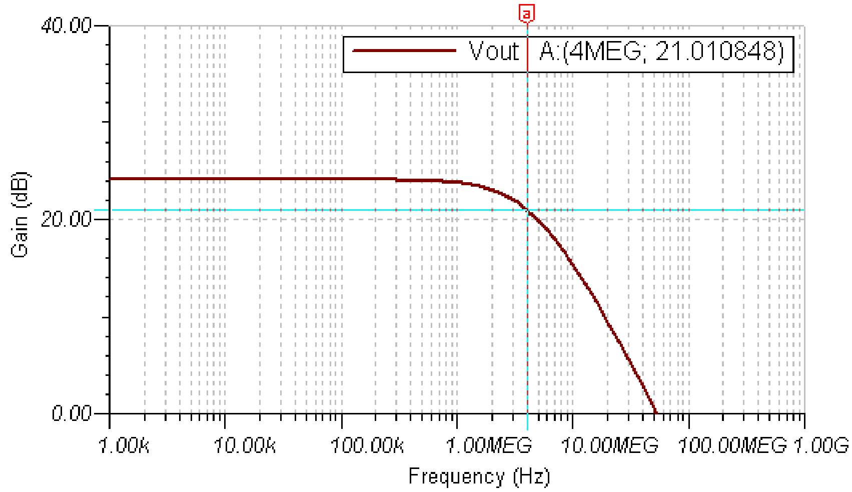
$$V_{IN-} = \mathrm{AmpV_{IN-}} - \frac{V_{OUT+} - \mathrm{AmpV_{IN-}}}{\frac{R_2}{R_1}}$$

$$\mathrm{Min}(V_{IN-}) = -0.1\mathrm{V} - \frac{9\mathrm{V} - (-0.1\mathrm{V})}{16\,\frac{\mathrm{V}}{\mathrm{V}}} = -0.65\mathrm{V}$$

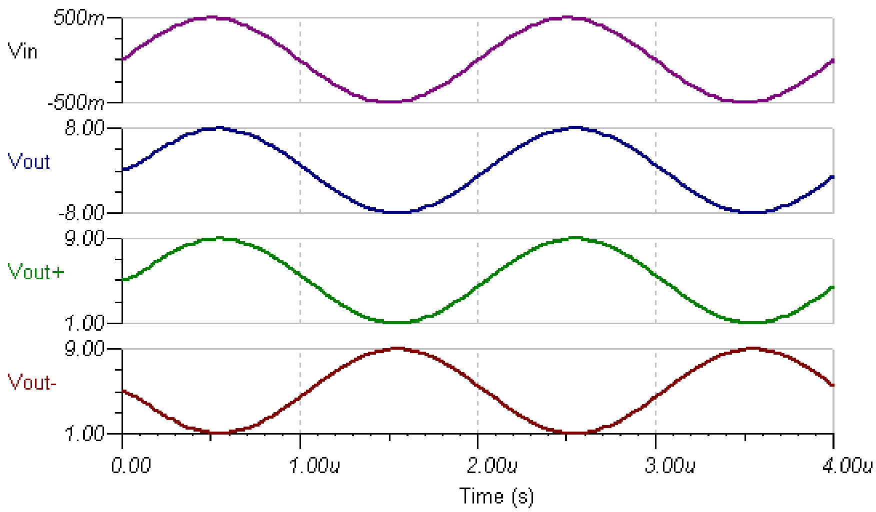
$$\mathrm{Max}(V_{IN-}) = 8.9\mathrm{V} + \frac{8.9\mathrm{V} - 1\mathrm{V}}{16\,\frac{\mathrm{V}}{\mathrm{V}}} = 9.4\mathrm{V}$$

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the TIDA-01036 tool folder for more information.

Design Featured Op Amp

THS4561	
V_{ss}	3 V to 13.5 V
V_{inCM}	V_{ee}-0.1 V to V_{CC}-1.1 V
V_{out}	V_{ee}+0.2 V to V_{cc}-0.2
V_{os}	TBD
I_q	TBD
I_b	TBD
UGBW	70 MHz
SR	4.4 V/µs
#Channels	1
THS4561	

Design Alternate Op Amp

THS4131	
V_{ss}	5 V to 33 V
V_{inCM}	V_{ee}+1.3 V to V_{cc}-0.1 V
V_{out}	Varies
V_{os}	2 mV
I_q	14 mA
I_b	2 µA
UGBW	80 MHz
SR	52 V/µs
#Channels	1
THS4131	

AC Coupled Instrumentation Amplifier Circuit

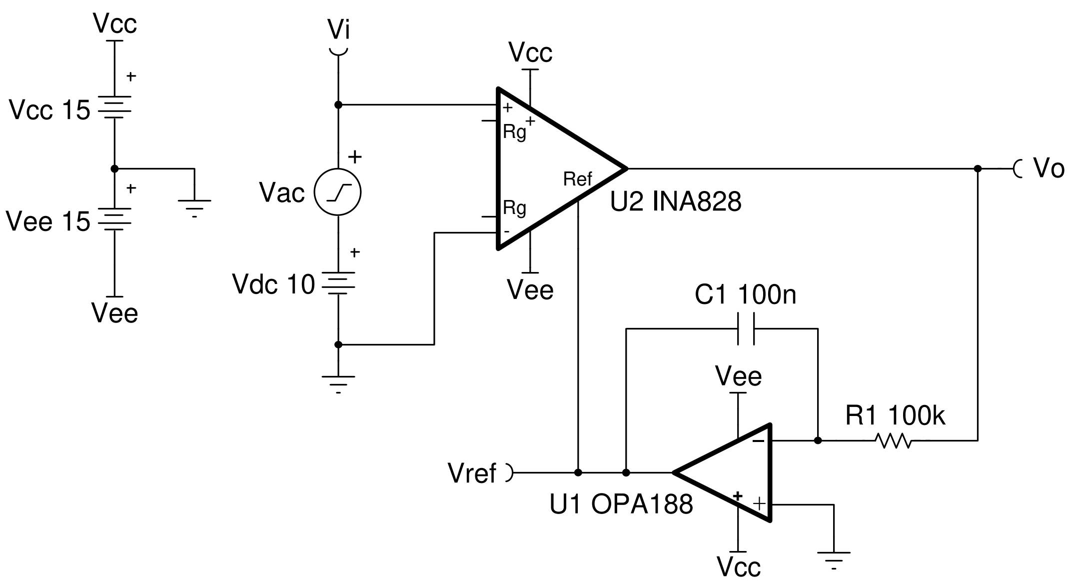
Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–13 V	13 V	–14.85 V	14.85	15	–15

Lower Cutoff Frequency (f_L)	Gain	Input
16 Hz	1	±2VAC; +10VDC

Design Description

This circuit produces an AC-coupled output from a DC-coupled input to an instrumentation amplifier. The output is fed back through an integrator, and the output of the integrator is used to modulate the reference voltage of the amplifier. This creates a high-pass filter and effectively cancels the output offset. This circuit avoids the need for large capacitors and resistors on the input, which can significantly degrade CMRR due to component mismatch.



Design Notes

1. The DC correction from output to reference is unity-gain. U_1 can only correct for a signal within its input/output limitations, thus the magnitude of DC voltage that can be corrected for will degrade with increasing instrumentation amplifier gain. See the table in Design Steps for more information.
2. Large values of R_1 and C_1 will lower the cutoff frequency, but increase startup transient response time. Startup behavior can be observed in the Transient Simulation Results.
3. When AC-coupling this way, the total input voltage must remain within the common-mode input range of the instrumentation amplifier.

Design Steps

1. Set the lower cutoff frequency for circuit (integrator cutoff frequency). The upper cutoff frequency will be dictated by the gain and instrumentation amplifier bandwidth.

$$f_L = \frac{1}{2\pi \times R_1 \times C_1} = 16\ \text{Hz}$$

2. Choose a standard value for R_1 and C_1.

$$C_1 = 100\ \text{nF}$$

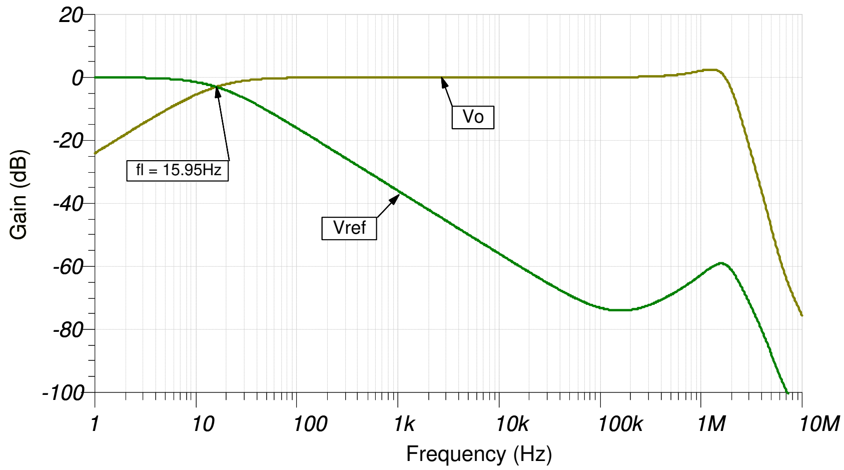
$$R_1 = \frac{1}{2\pi \times 100\ \text{nF} \times 16\ \text{Hz}} = 99.47\ \text{k}\Omega \approx 100\ \text{k}\Omega \quad (\text{standard} \quad \text{value})$$

3. The DC rejection capabilities of the circuit will degrade with gain. The following table provides a good estimate of the DC correction range for higher gains.

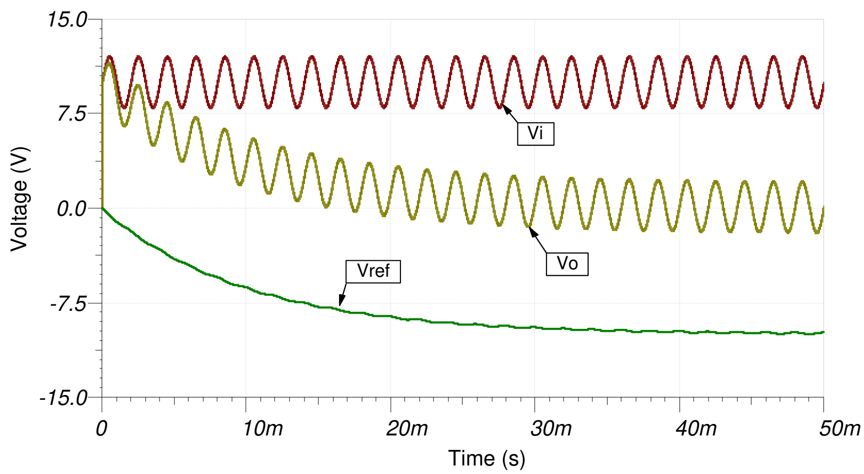
Gain	DC Correction Range
1 V/V	±10 V
10 V/V	±1 V
100 V/V	±0.1 V
1000 V/V	±0.01 V

Design Simulations

AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, SBOMAU0.

See TIPD191, Instrumentation Amplifier with DC Rejection Reference Design.

Design Featured Instrumentation Amplifier

INA828	
V_{ss}	4.5 V to 36 V
V_{inCM}	V_{ee}+2 V to V_{cc}–2 V
V_{out}	V_{ee}+150 mV to V_{cc}–150 mV
V_{os}	20 µV
I_q	600 µA
I_b	150 pA
UGBW	2 MHz
SR	1.2 V/µs
#Channels	1
INA828	

Design Featured Op Amp

OPA188	
V_{ss}	8 V to 36 V
V_{inCM}	V_{ee} to V_{cc}–1.5 V
V_{out}	Rail-to-rail
V_{os}	6 µV
I_q	450 µA
I_b	±160 pA
UGBW	2 MHz
SR	0.8 V/µs
#Channels	1, 2, and 4
OPA188	

Design Alternate Op Amp

TLV171	
V_{ss}	2.7 V to 36 V
V_{inCM}	V_{ee}–0.1 V to V_{cc}–2 V
V_{out}	Rail-to-rail
V_{os}	750 µV
I_q	525 µA
I_b	±10 pA
UGBW	3 MHz
SR	1.5 V/µs
#Channels	1, 2, and 4
TLV171	

Analog Engineer's Circuit

Inverting attenuator circuit

TEXAS INSTRUMENTS

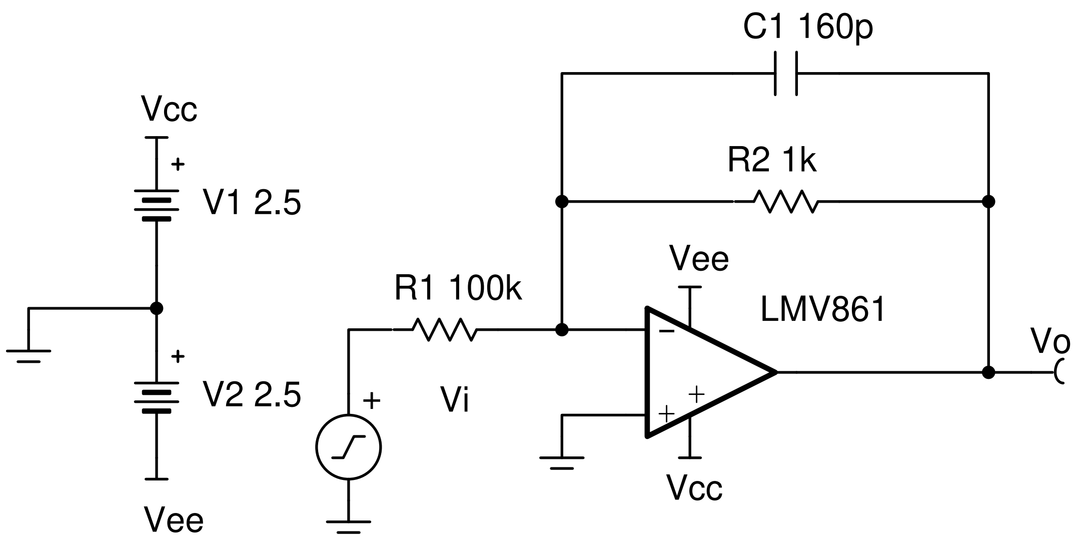
Amplifiers

Design Goals

Input		Output		BW	Gain	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f_p	G	V_{cc}	V_{ee}
–200V	200V	–2V	2V	1MHz	–40dB	2.5V	–2.5V

Design Description

This circuit inverts the input signal, V_i, and applies a signal gain of –40dB. The common-mode voltage of an inverting amplifier is equal to the voltage applied to the non-inverting input, which is ground in this design.



Design Notes

1. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistor. Make sure this value is large when compared to the output impedance of the source.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit. The capacitor in parallel with R_2 provides filtering and improves stability of the circuit if high-value resistors are used for both the input and feedback resistances.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP).
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth see the *Design References* section.
8. Note that higher input voltage levels may require the use of multiple resistors in series to help reduce the voltage drop across the individual resistors. For more information, see the *Design References* section.

Design Steps

The transfer function of this circuit follows:

$$V_o = V_i \times \left(-\frac{R_2}{R_1}\right)$$

1. Calculate the gain required for the circuit.

$$G = \frac{V_{oMax} - V_{oMin}}{V_{iMax} - V_{iMin}} = \frac{2V - (-2V)}{200V - (-200V)} = 0.01\frac{V}{V} = -40dB$$

2. Choose the starting value of R_1.

$$R_1 = 100k\Omega$$

3. Calculate for a desired signal attenuation of 0.01 V/V.

$$G = \frac{R_2}{R_1} \rightarrow R_2 = R_1 \times G = 0.01\frac{V}{V} \times 100k\Omega = 1k\Omega$$

4. Select the feedback capacitor, C_1, to meet the circuit bandwidth.

$$C_1 \le \frac{1}{2\pi \times R_2 \times f_p} \rightarrow C_1 \le \frac{1}{2\pi \times 1k\Omega \times 1MHz} \le 159.15pF \approx 160pF \text{ (Standard Value)}$$

5. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$V_p < \frac{SR}{2\pi \times f_p} \rightarrow SR > 2\pi \times f \times V_p \rightarrow SR > 2\pi \times 1\text{ MHz} \times 2\text{ V} = 12.6\frac{V}{\mu S}$$

   - SR_{LMV861} = 18V/µs; therefore, it meets this requirement.

6. Calculate the circuit bandwidth to ensure it meets the 1-MHz requirement. Be sure to use the noise gain, NG, or non-inverting gain, of the circuit.

$$NG = 1 + \frac{R_2}{R_1} = 1.01\frac{V}{V} \rightarrow BW = \frac{GBP}{NG} = \frac{30MHz}{1.01\frac{V}{V}} = 29.7MHz$$

   - BW_{LMV861} = 30MHz; therefore, it meets this requirement.

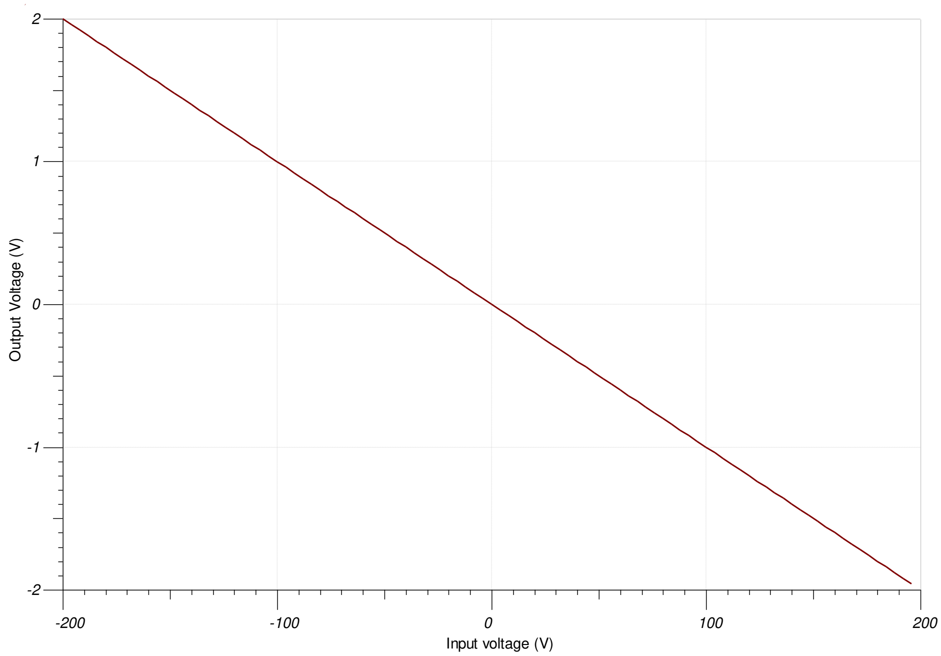
7. If C_1 is not used to limit the circuit bandwidth, to avoid stability issues ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2\pi \times (C_{cm} + C_{diff}) \times (R_2 \,||\, R_1)} > \frac{GBP_{LMV861}}{NG}$$

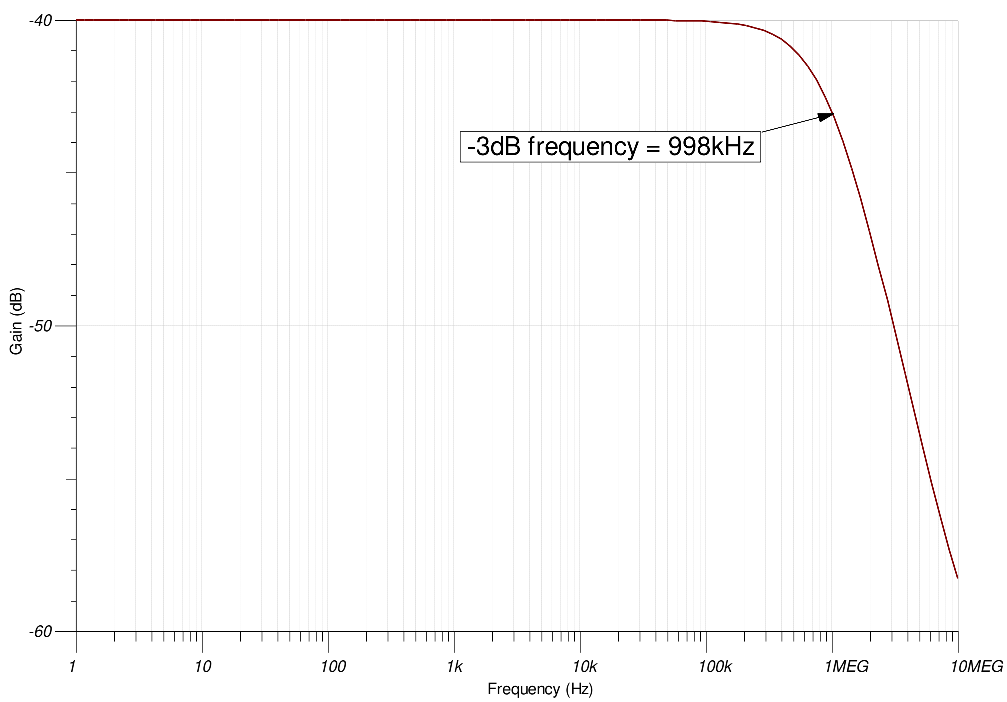
   - C_{cm} and C_{diff} are the common-mode and differential input capacitance of the LMV861, respectively.

Design Simulations

DC Simulation Results

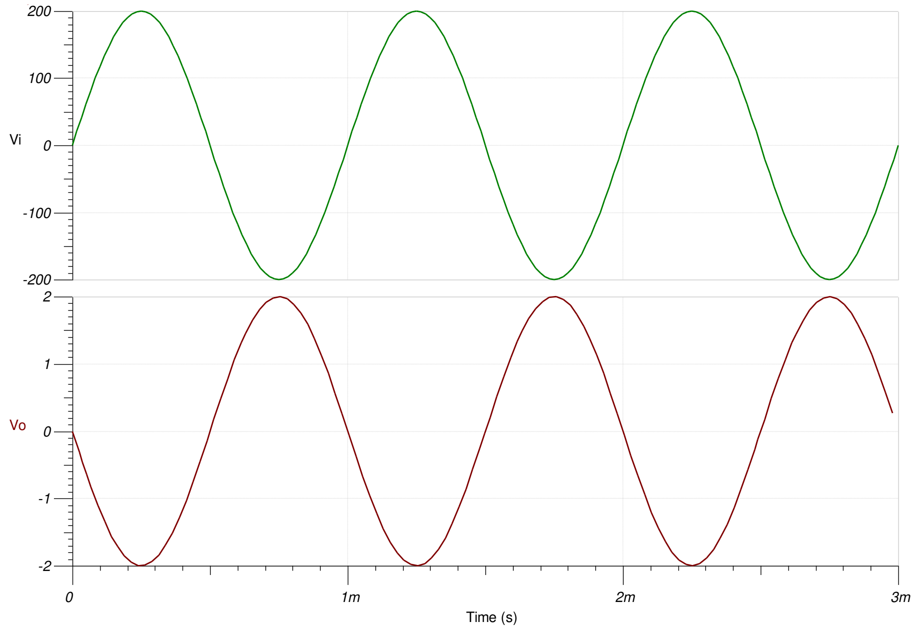


AC Simulation Results



Transient Simulation Results

A 1-kHz, 400-Vpp input sine wave yields a 4-Vpp output sine wave.



Design References

1. See *Analog Engineer's Circuit Cookbooks* for the comprehensive TI circuit library.
2. SPICE Simulation File SBOC522.
3. TI Precision Labs
4. For more information on circuits with larger input voltages, see *Considerations for High-Voltage Measurements*.

Design Featured Op Amp

LMV861	
V_{ss}	2.7V to 5.5V
V_{inCM}	(Vee – 0.1V) to (Vcc – 1.1V)
V_{out}	Rail-to-rail
V_{os}	0.273mV
I_q	2.25mA
I_b	0.1pA
UGBW	30MHz
SR	18V/µs
#Channels	1, 2
www.ti.com/product/LMV861	

Design Alternate Op Amp

	TLV9002	OPA377
V_{ss}	1.8V to 5.5V	2.2V to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{out}	Rail-to-rail	Rail-to-rail
V_{os}	0.4mV	0.25mV
I_q	0.06mA	0.76mA
I_b	5pA	0.2pA
UGBW	1MHz	5.5MHz
SR	2V/µs	2V/µs
#Channels	1, 2, 4	1, 2, 4
	www.ti.com/product/TLV9002	www.ti.com/product/OPA377

Analog Engineer's Circuit Amplifiers

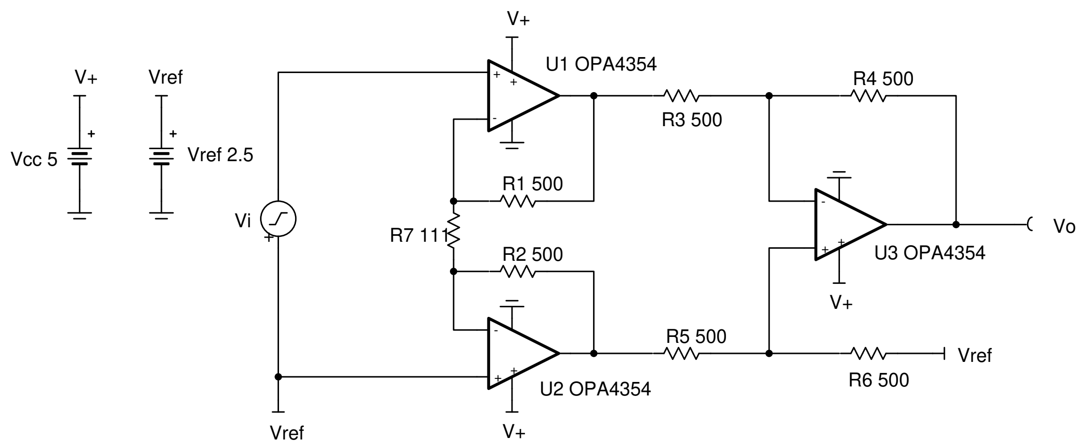
Discrete Wide Bandwidth INA Circuit

Design Goals

Input		Output		Bandwidth	Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	BW	V_{cc}	V_{ee}	V_{ref}
–0.24V	+0.24V	+0.1V	+4.9V	10MHz	+2.5V	0V	2.5V

Design Description

This design uses 3 op–amps to build a discrete wide bandwidth instrumentation amplifier. The circuit converts a differential, high frequency signal to a single–ended output.



Design Notes

1. Reduce the capacitance on the output of each op amp to avoid stability issues.
2. Use low gain configurations to maximize the bandwidth of the circuit.
3. Use precision resistors to achieve high DC CMRR performance.
4. Use small resistors in op–amp feedback to maintain stability.
5. Set the reference voltage, V_{ref}, at mid–supply to allow the output to swing to both supply rails.
6. Phase margin of 45° or greater is required for stable operation.
7. R_7 sets the gain of the instrumentation amplifier.
8. Linear operation depends upon the input common–mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the A_{ol} test conditions in the op amps datasheets.
9. V_{ref} also sets the common-mode voltage of the input, V_i, to ensure linear operation.

Design Steps

1. The transfer function of the circuit is given below.

$$V_o = V_i \times \left(1 + \frac{2 \times R_1}{R_7}\right) \times \left(\frac{R_6}{R_5}\right)$$

where V_i is the differential input voltage

Vref is the reference voltage provided to the amplifier

$$Gain = \left(1 + \frac{2 \times R_1}{R_7}\right) \times \left(\frac{R_6}{R_5}\right)$$

2. To maximize the usable bandwidth of design, set the gain of the diff amp stage to 1V/V. Use smaller value resistors to minimize noise.

Choose $R_3 = R_4 = R_5 = R_6 = 500\ \Omega$ (Standard value)

3. Choose values for resistors R_1 and R_2. Keep these values low to minimize noise.

$R_1 = R_2 = 500\ \Omega$ (Standard value)

4. Calculate resistor R_7 to set the gain of the circuit to 10V/V

$$G = \left(1 + \frac{2 \times R_1}{R_7}\right) = 10\frac{V}{V} \rightarrow \frac{2 \times 500\Omega}{R_7} = 9\frac{V}{V}$$

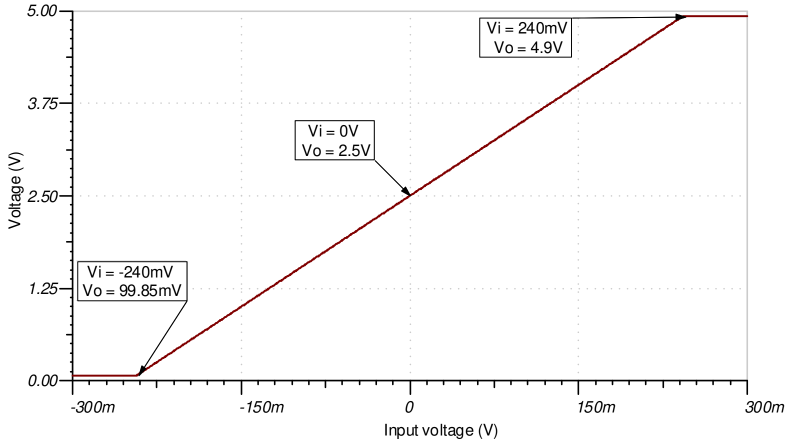
$$R_7 = \frac{1000\Omega}{9\frac{V}{V}} = 111.11\Omega \rightarrow R_7 = 111\Omega\ (Standard\ Value)$$

5. Calculate the reference voltage to bias the input to mid-supply. This will maximize the linear output swing of the instrumentation amplifier. See References for more information on the linear operating region of instrumentation amplifiers.

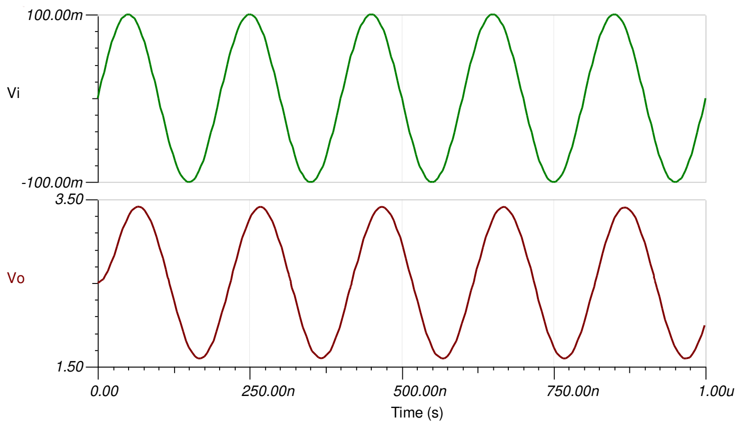
$$V_{ref} = \frac{V_s}{2} = \frac{5\ V}{2} = 2.5\ V$$

Design Simulations

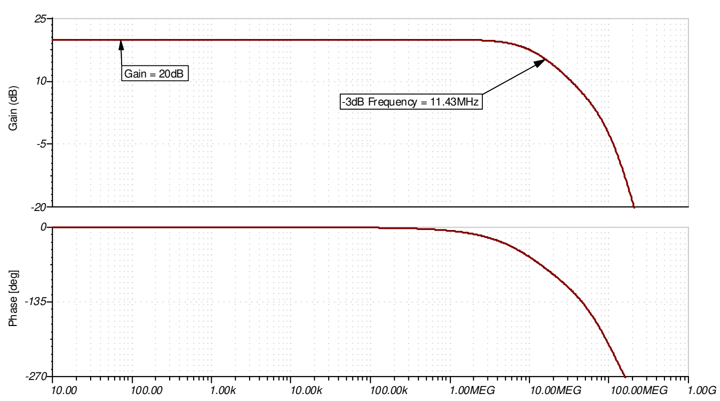
DC Simulation Results



Transient Simulation Results



AC Simulation Results



References

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOMAU6
3. TI Precision Labs
4. *Instrumentation Amplifier V_{CM} vs. V_{OUT} Plots*
5. Common-mode Range Calculator for Instrumentation Amplifiers

Design Featured Op Amp

OPA354	
V_{ss}	2.5V to 5.5V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	2mV
I_q	4.9mA/Ch
I_b	3pA
UGBW	250MHz
SR	150V/µs
#Channels	1,2,4
www.ti.com/product/opa354	

Design Alternate Op Amp

OPA322	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	500µV
I_q	1.6mA/Ch
I_b	0.2pA
UGBW	20MHz
SR	10V/µs
#Channels	1,2,4
www.ti.com/product/opa322	

Revision History

Revision	Date	Change
A	December 2020	Updated R11 to R7 for resistor number consistency

Analog Engineer's Circuit

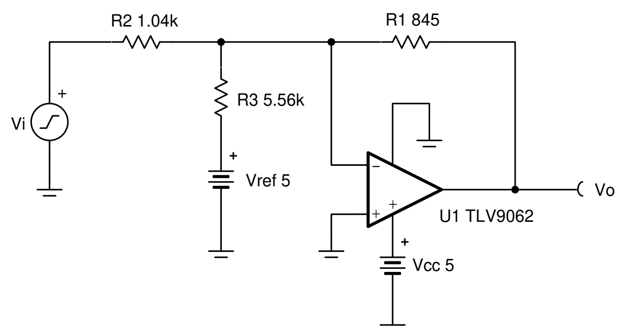
Inverting Op Amp with Inverting Positive Reference Voltage Circuit

Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–5 V	–1 V	0.05 V	3.3 V	5 V	0 V	5 V

Design Description

This design uses an inverting amplifier with an inverting positive reference to translate an input signal of –5 V to –1 V to an output voltage of 3.3 V to 0.05 V. This circuit can be used to translate a negative sensor output voltage to a usable ADC input voltage range.



Design Notes

1. Use op amp linear output operating range. Usually specified under A_{OL} test conditions.
2. Common mode range must extend down to or below ground.
3. V_{ref} output must be low impedance.
4. Input impedance of the circuit is equal to R_2.
5. Choose low-value resistors to use in the feedback. It is recommended to use resistor values less than 100 kΩ. Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit.
6. The cutoff frequency of the circuit is dependent on the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1. Adding a capacitor in parallel with R_1 will also improve stability of the circuit if high-value resistors are used.

Design Steps

$$V_o = -V_i \times \left(\frac{R_1}{R_2}\right) - V_{ref} \times \left(\frac{R_1}{R_3}\right)$$

1. Calculate the gain of the input signal.

$$G_{input} = \frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}} = \frac{3.3V - 0.05V}{-1V - (-5\ \ V)} = 0.8125\frac{V}{V}$$

2. Calculate R_1 and R_2.

$$\text{Choose}\quad R_1 = 845\Omega$$

$$R_2 = \frac{R_1}{G_{input}} = \frac{R_1}{0.8125\frac{V}{V}} = 1.04\ \ k\Omega$$

3. Calculate the gain of the reference voltage required to offset the output.

$$G_{ref} = \frac{R_1}{R_3}$$

$$-V_{i\_min} \times \left(\frac{R_1}{R_2}\right) - V_{ref} \times \left(\frac{R_1}{R_3}\right) = V_{o\_min}$$

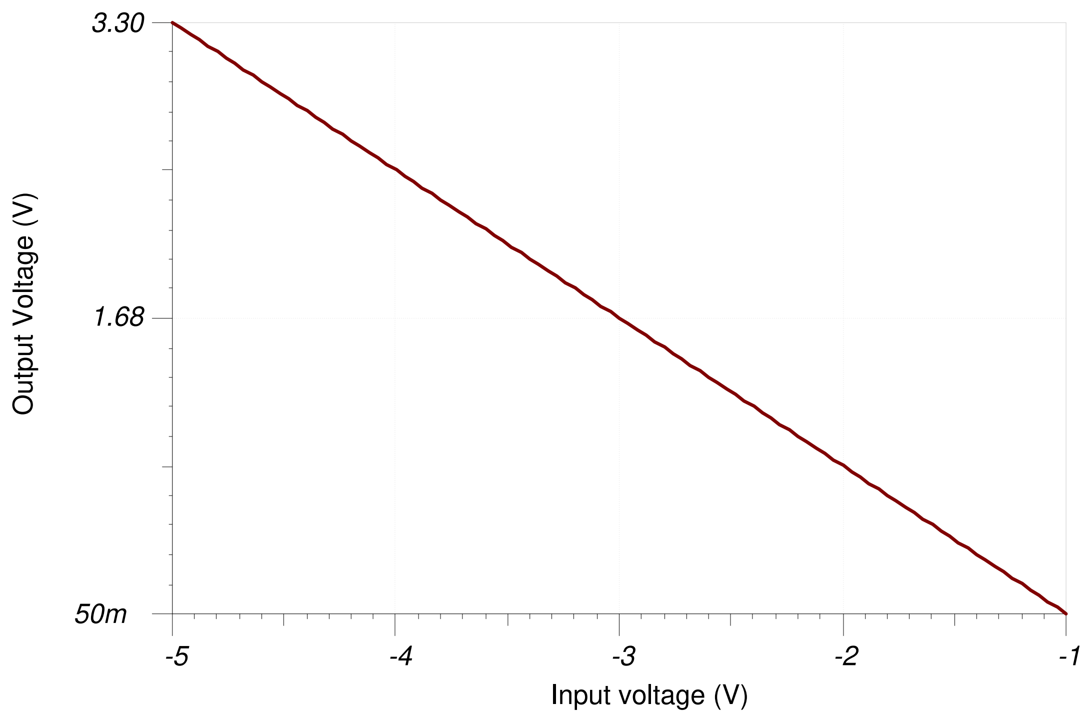
$$\frac{R_1}{R_3} = \frac{V_{o\_min} + V_{i\_min} \times \left(\frac{R_1}{R_2}\right)}{-V_{ref}} = \frac{0.05V + (-1\ \ V)\left(\frac{845\Omega}{1.04k\Omega}\right)}{-5} = 0.1525\frac{V}{V}$$

4. Calculate R_3.

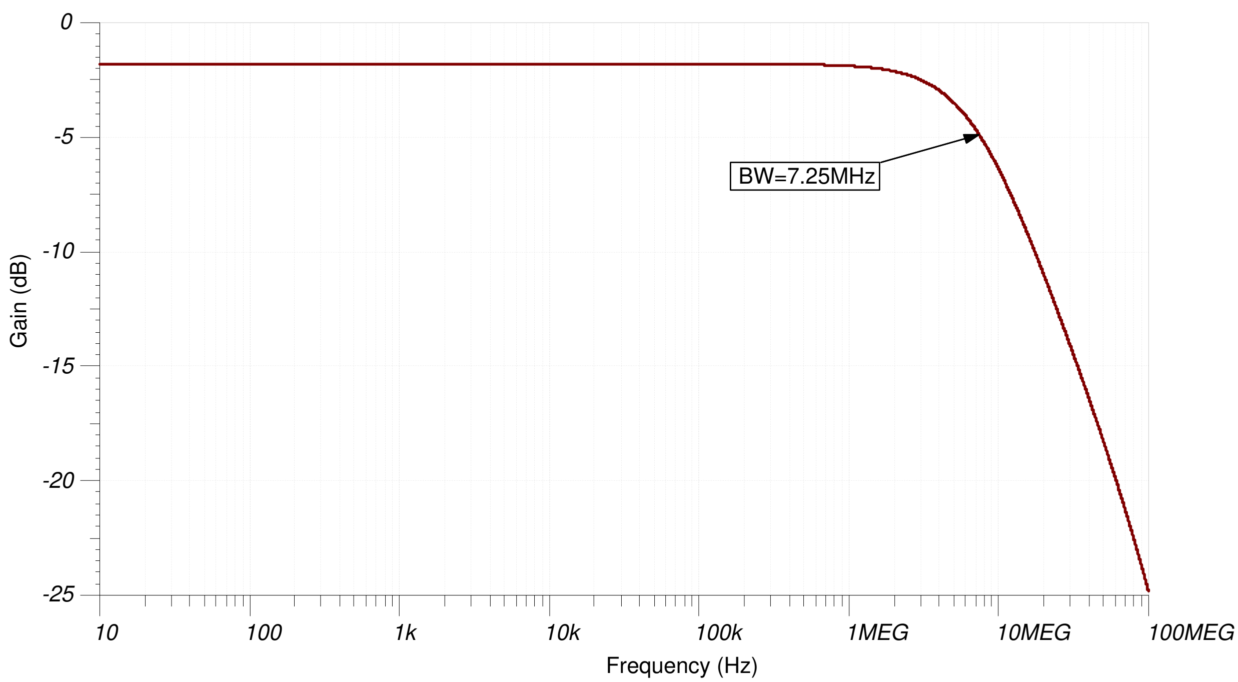
$$R_3 = \frac{R_1}{G_{ref}} = \frac{845\Omega}{0.1525\frac{V}{V}} = 5.54\ \ k\Omega \approx 5.56\ \ k\Omega$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC511.

See *Designing Gain and Offset in Thirty Seconds*.

Design Featured Op Amp

TLV9062	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3 mV
I_q	538 µA
I_b	0.5 pA
UGBW	10 MHz
SR	6.5 V/µs
#Channels	1, 2, and 4
TLV9062	

Design Alternate Op Amp

OPA197	
V_{ss}	4.5 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	25 µV
I_q	1 mA
I_b	5 pA
UGBW	10 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA197	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019 **Page**

- Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.. 1

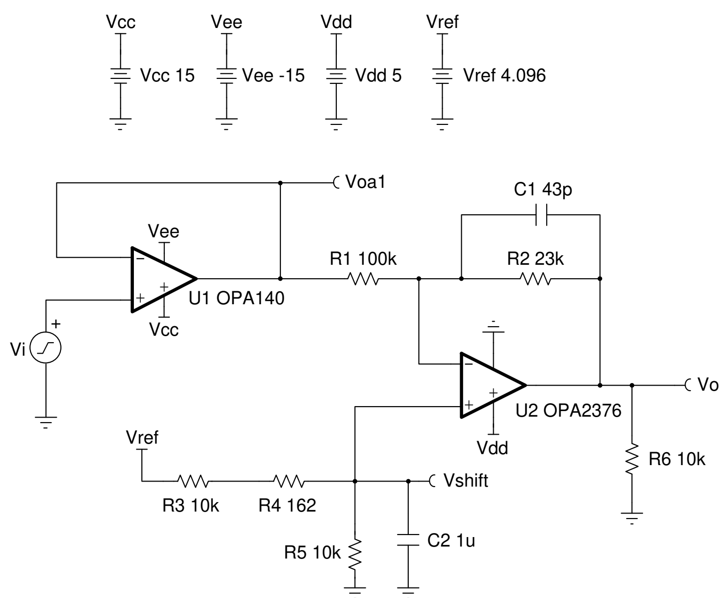
Inverting Dual-Supply to Single-Supply Amplifier Circuit

Design Goals

Input		Output		Supply			
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{dd}	V_{ref}
–10 V	+10 V	+0.2 V	+4.8 V	+15 V	–15 V	+5 V	+4.096 V

Design Description

This inverting dual-supply to single-supply amplifier translates a ±10 V signal to a 0 V to 5 V signal for use with an ADC. Levels can easily be adjusted using the given equations. The buffer can be replaced with other ±15 V configurations to accommodate the desired input signal, as long as the output of the first stage is low impedance.



Design Notes

1. Observe common-mode limitations of the input buffer.
2. A high-impedance source will alter the gain characteristics of U_2 if buffer amplifier U1 is not used.
3. R_6 provides a path to ground for the output of U_1 if the ±15 V supplies come up before the 5 V supply. This limits the voltage at the inverting pin of U_2 through the voltage divider created by R_1, R_2, and R_6 and prevents damage to U_2 as well as to any converter that may be connected to its output. To best protect the devices a transient voltage suppressor (TVS) should be used at the power pins of U_2.
4. A capacitor across R_5 will help filter V_{ref} and provide a cleaner V_{shift}.

Design Steps

The transfer function for this circuit follows:

$$V_o = -\frac{R_2}{R_1} \times V_i + \left(1 + \frac{R_2}{R_1}\right) \times V_{shift}$$

1. Set the gain of the amplifier.

$$\frac{\Delta V_o}{\Delta V_i} = \frac{V_{oMax} - V_{oMin}}{V_{iMax} - V_{iMin}} = \frac{4.8\ V - 0.2\ V}{10\ V - (-10\ V)} = 0.23$$

$$\frac{\Delta V_o}{\Delta V_i} = \frac{R_2}{R_1}$$

$$R_2 = 0.23 \times R_1$$

$$\text{Choose} \quad R_1 = 100k\Omega \quad (\text{standard} \quad \text{value})$$

$$R_2 = 23k\Omega \quad (\text{for} \quad \text{standard} \quad \text{values} \quad \text{use} \quad 22k\Omega \quad \text{and} \quad 1k\Omega \quad \text{in} \quad \text{series})$$

2. Set V_{shift} to translate the signal to single supply.

$$\text{At} \quad \text{midscale,} \quad V_{in} = 0V$$

$$\text{Then} \quad V_o = \left(1 + \frac{R_2}{R_1}\right) \times V_{shift}$$

$$V_{shift} = \frac{V_o}{\left(1 + \frac{R_2}{R_1}\right)} = \frac{2.5V}{1.23} = 2.033V$$

3. Select resistors for reference voltage divider to achieve V_{shift}.

$$V_{ref} = 4.096V$$

$$V_{shift} = V_{ref} \times \frac{R_5}{(R_3 + R_4) + R_5}$$

$$\frac{V_{shift}}{V_{ref}} = \frac{2.033V}{4.096V} = \frac{R_5}{(R_3 + R_4) + R_5}$$

$$R_3 + R_4 = 1.0161 \times R_5$$

$$\text{Select} \quad \text{a} \quad \text{standard} \quad \text{value} \quad \text{for} \quad R_5$$

$$R_5 = 10k\Omega$$

$$R_3 + R_4 = 10.161k\Omega$$

$$R_3 = 10k\Omega$$

$$R_4 = 162\Omega \quad (\text{standard} \quad 1\% \quad \text{value})$$

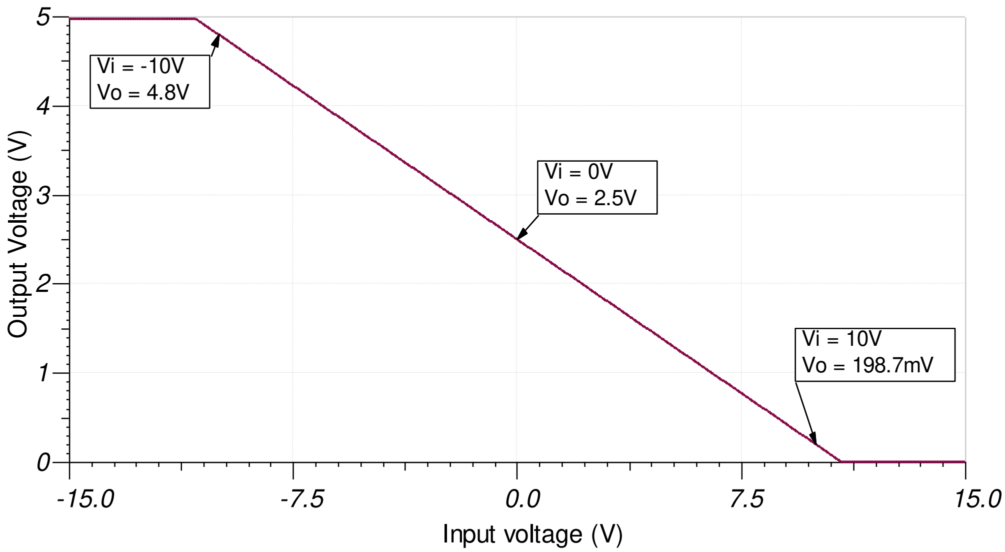
4. Large feedback resistors can interact with the input capacitance and cause instability. Choose C_1 to add a pole to the transfer function to counteract this. The pole must be lower in frequency than the effective bandwidth of the op amp.

$$C_1 = 43\text{pF}$$

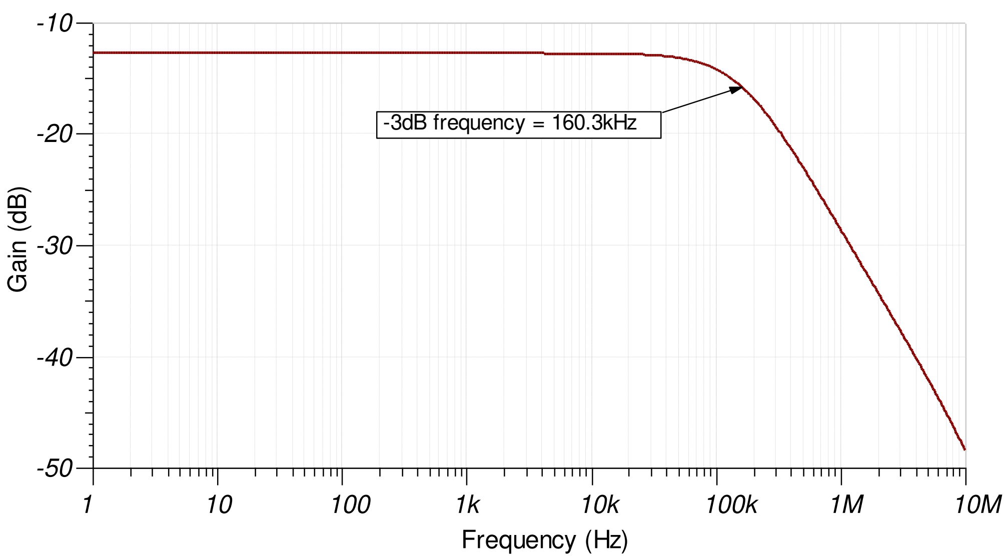
$$f_p = \frac{1}{2\pi \times R_2 \times C_1} = 160.3\text{kHz}$$

Design Simulations

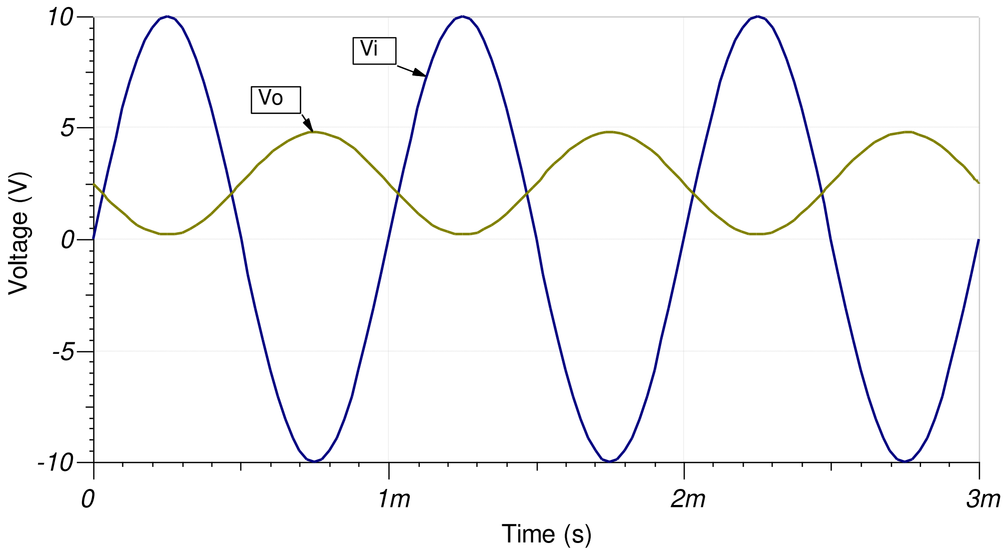
DC Simulation Results



AC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See TINA-TI™ circuit simulation file, SBOMAT9.

See TIPD148.

Design Featured Op Amp

OPA376	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	V_{ee} to V_{cc}-1.3 V
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	760 µA/Ch
I_b	0.2 pA
UGBW	5.5 MHz
SR	2 V/µs
#Channels	1, 2, and 4
OPA376	

Design Featured Op Amp

OPA140	
V_{ss}	4.5 V to 36 V
V_{inCM}	V_{ee}-0.1 V to V_{cc}-3.5 V
V_{out}	Rail-to-rail
V_{os}	30 µV
I_q	1.8 mA/Ch
I_b	±0.5 pA
UGBW	11 MHz
SR	20 V/µs
#Channels	1, 2, and 4
OPA140	

Analog Engineer's Circuit

Dual-Supply, Discrete, Programmable Gain Amplifier Circuit

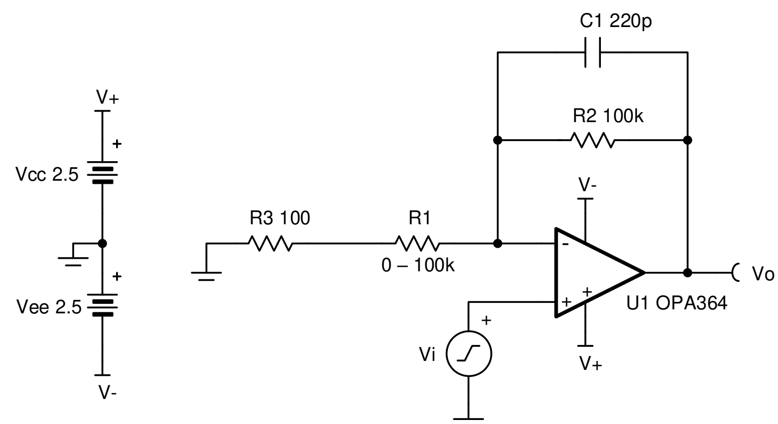
Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
–1.25 V	+1.25 V	–2.4 V	+2.4 V	+2.5 V	–2.5 V

Gain	Cutoff Frequency
6 dB (2 V/V) to 60 dB (1000 V/V)	7 kHz

Design Description

This circuit provides programmable, non-inverting gains ranging from 6 dB (2 V/V) to 60 dB (1000 V/V) using a variable input resistance. The design maintains the same cutoff frequency over the gain range.



Design Notes

1. Choose a digital potentiometer, such as TPL0102 for R_1 to design a low-cost digital programmable gain amplifier.
2. R_3 sets the maximum gain when R_1 approaches 0 Ω.
3. A feedback capacitor limits the bandwidth and prevent stability issues.
4. Stability should be evaluated across the selected gain range. The minimum gain setting will likely be most sensitive to stability issues.
5. Some digital potentiometers can vary in absolute value by as much as ±20% so gain calibration may be necessary.

Design Steps

1. Choose R_2 and R_3, to set the maximum gain when R_1 approaches 0:

$$G_{max} = 1 + \frac{R_2}{R_3}$$
$$G_{max} - 1 = \frac{R_2}{R_3} \rightarrow R_2 = \left(G_{max} - 1\right) \times R_3$$
$$\text{Set} \quad R_3 = 100\ \Omega$$
$$R_2 = \left(1000\ \frac{V}{V} - 1\right) \times 100 = 99\ k\Omega \rightarrow R_2 = 100\ k\Omega \ \left(\text{Standard} \quad \text{value}\right)$$

2. Choose the potentiometer maximum value to set the minimum gain:

$$G_{min} = 1 + \frac{R_2}{R_{1,max} + R_3}$$
$$G_{min} - 1 = \frac{R_2}{R_{1,max} + R_3}$$
$$R_{1,max} + R_3 = \frac{R_2}{G_{min} - 1}$$
$$R_{1,max} = \frac{R_2}{G_{min} - 1} - R_3 = \frac{100k\Omega}{2 - 1} - 100\Omega = 99.9k\Omega \rightarrow R_{1,max} = 100k\Omega \ \left(\text{Standard} \quad \text{value}\right)$$
$$R_{1,min} = 0\Omega \ \left(\text{Wiper} \quad \text{resistance,} \quad \text{typically} \quad 25\Omega, \quad \text{will} \quad \text{introduce} \quad \text{some} \quad \text{error}\right)$$

3. Choose the bandwidth with a feedback capacitor:

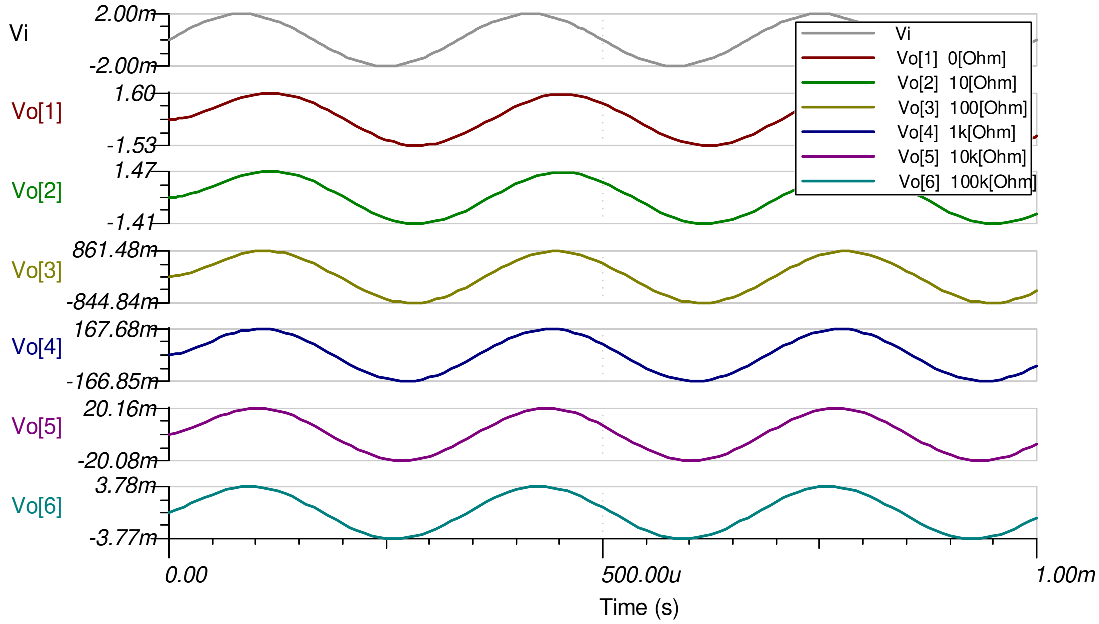
$$f_c = \frac{GBW}{G_{max}} = \frac{7MHz}{1000\frac{V}{V}} = 7kHz$$
$$f_c = 7kHz \rightarrow C_1 = \frac{1}{2\pi \times R_2 \times f_c} = 227pF \quad \rightarrow C_1 = 220pF \ \left(\text{Standard} \quad \text{Value}\right)$$

4. Check for stability at minimum gain (2V/V), which is when R_1=100 kΩ. To satisfy the requirement f_c (circuit bandwidth) must be less than f_{zero} (zero created by the resistive feedback network and the differential and common-mode input capacitances).

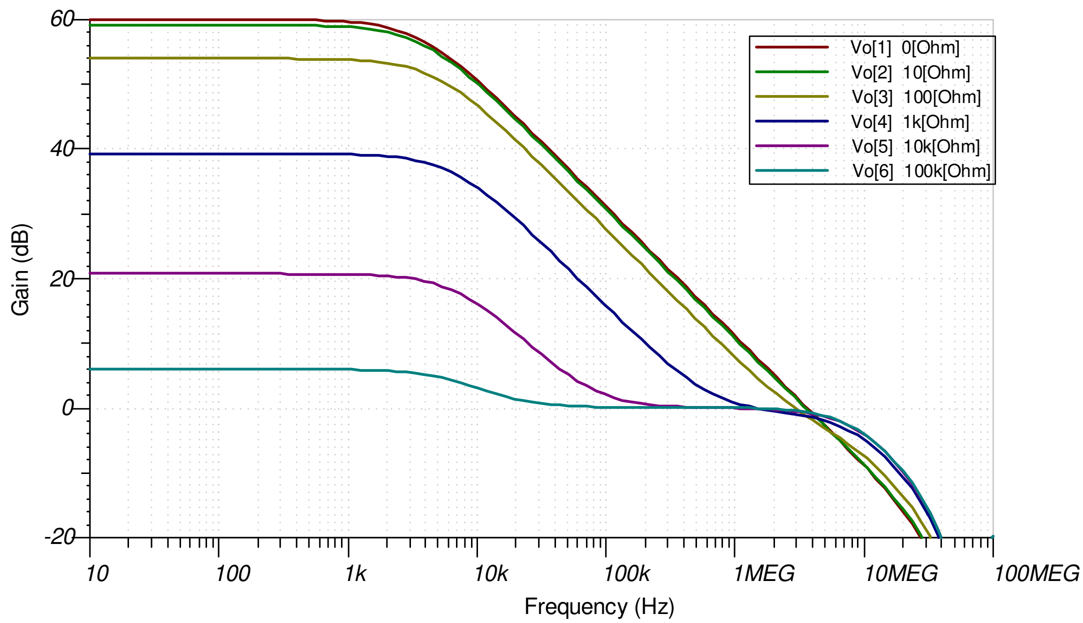
$$f_c = \frac{1}{2\pi \times C_1 \times R_2} = 7\ kHz$$
$$f_{zero} = \frac{1}{2\pi \times (C_{cm} + C_{diff}) \times (R_2 \parallel R_1)} = \frac{1}{2 \times \pi \times \left(3\ pF + 2\ pF\right) \times \left(\frac{100\ k\Omega \times 100\ k\Omega}{100\ k\Omega + 100\ k\Omega}\right)}$$
$$f_{zero} = 637\ kHz$$
$$7\ kHz < 637\ kHz \rightarrow f_c < f_{zero}$$

Design Simulations

Transient Simulation Results



AC Simulation Results



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOC521
3. TI Precision Designs TIPD204
4. TI Precision Labs

Design Featured Op Amp

OPA364	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	1.1 mA
I_b	1 pA
UGBW	7 MHz
SR	5 V/µs
#Channels	1, 2, and 4
OPA364	

Design Alternate Op Amp

OPA376	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5 µV
I_q	760 µA
I_b	0.2 pA
UGBW	5.5 MHz
SR	2 V/µs
#Channels	1, 2, and 4
OPA376	

Single-supply diff-in to diff-out AC amplifier circuit

TEXAS INSTRUMENTS

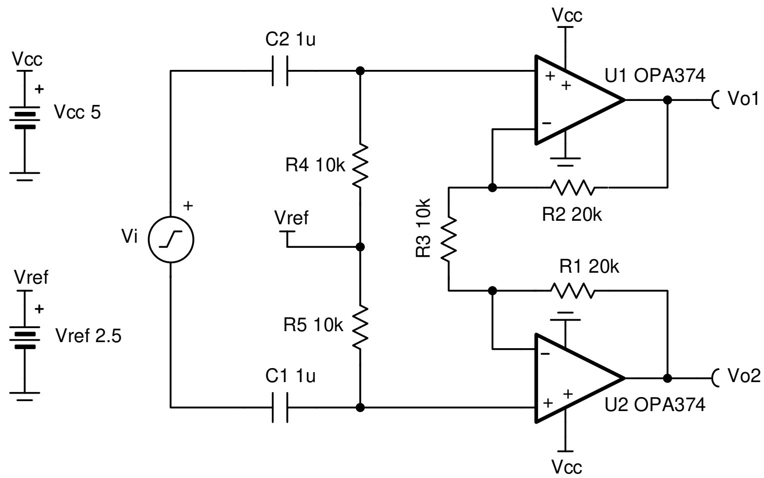
Design Goals

Diff. Input V_i		**Diff. Output ($V_{o1} - V_{o2}$)**		**Supply**		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–500mV	+500mV	–2.5V	+2.5V	+5	0V	+2.5V

Lower Cutoff Freq.	**Upper Cutoff Freq.**
16Hz	> 1MHz

Design Description

This circuit uses 2 op amps to build a discrete, single-supply diff-in diff-out amplifier. The circuit converts a differential signal to a differential output signal.



Design Notes

1. Ensure that R_1 and R_2 are well matched with high accuracy resistors to maintain high DC common-mode rejection performance.
2. Increase R_4 and R_5 to match the necessary input impedance at the expense of thermal noise performance.
3. Bias for single-supply operation can also be created by a voltage divider from V_{cc} to ground.
4. V_{ref} sets the output voltage of the instrumentation amplifier bias at mid-supply to allow the output to swing to both supply rails.
5. Choose C_1 and C_2 to select the lower cutoff frequency.
6. Linear operation is contingent upon the input common-mode and the output swing ranges of the discrete op amps used. The linear output swing ranges are specified under the Aol test conditions in the op amps data sheets

Design Steps

1. The transfer function of the circuit is shown below.

$$V_{oDiff} = V_i \times G + V_{ref}$$
$$\text{where} \quad V_i = \text{the differential input voltage}$$
$$V_{ref} = \text{the reference voltage provided to the amplifier}$$
$$G = 1 + 2 \times \left(\frac{R_1}{R_3}\right)$$

2. Choose resistors $R_1 = R_2$ to maintain common-mode rejection performance.

$$\text{Choose} \quad R_1 = R_2 = 20\ \text{k}\Omega \quad (\text{Standard value})$$

3. Choose resistors R_4 and R_5 to meet the desired input impedance.

$$\text{Choose} \quad R_4 = R_5 = 10\ \text{k}\Omega \quad (\text{Standard value})$$

4. Calculate R_3 to set the differential gain.

$$\text{Gain} = 1 + \left(\frac{2 \times R_1}{R_3}\right) = 5\ \frac{V}{V}$$
$$R_1 = R_2 = 20\ \text{k}\ \Omega$$
$$G = 1 + \frac{2 \times 20\ \text{k}\Omega}{R_3} = 5\ \frac{V}{V} \rightarrow 5\ \frac{V}{V} - 1 = \frac{40\ \text{k}\Omega}{R_3} = 4 \rightarrow R_3 = \frac{40\ \text{k}\Omega}{4} = 10\ \text{k}\Omega \ \left(\text{Standard value}\right)$$

5. Set the reference voltage V_{ref} at mid-supply.

$$V_{ref} = \frac{V_{cc}}{2} = \frac{5\ V}{2} \rightarrow V_{ref} = 2.5V$$

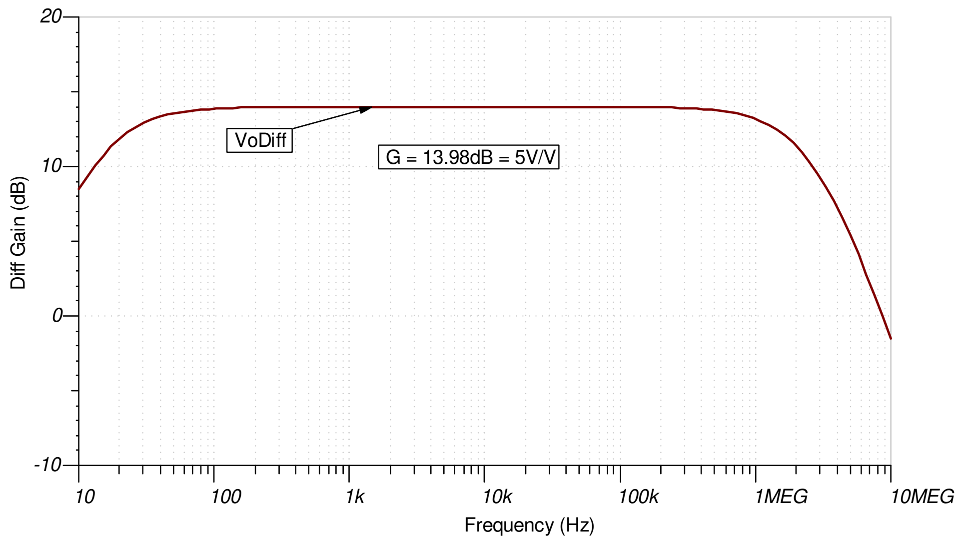
6. Calculate C_1 and C_2 to set the lower cutoff frequency.

$$f_c = \frac{1}{2 \times \pi \times R_4 \times C_1} = 16\ \text{Hz}$$
$$R_4 = R_5 = 10\ \text{k}\Omega$$
$$f_c = \frac{1}{2 \times \pi \times 10\ \text{k}\Omega \times C_1} = 16\ \text{Hz} \rightarrow C_1 = \frac{1}{2 \times \pi \times 10\ \text{k}\Omega \times 16\ \text{Hz}} = 0.99\mu\text{F} \rightarrow C_1 = C_2 = 1\mu\text{F} \ \left(\text{Standard value}\right)$$

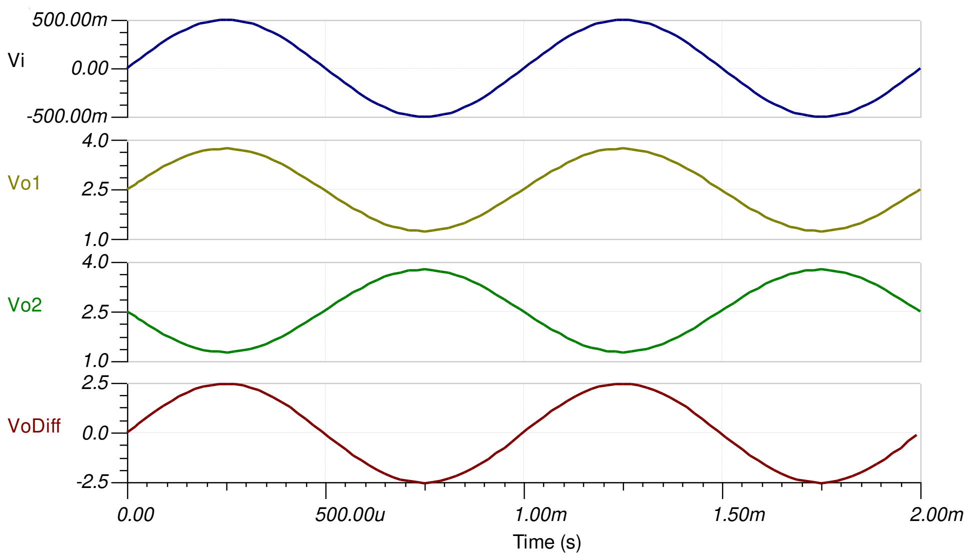
Design Simulations

AC Simulation Results

In the following figure, notice the lower –3-dB cutoff frequency is approximately 16Hz and the upper cutoff frequency is > 1MHz as required for this design.



Transient Simulation Results



References

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOMAU5.
3. TI Precision Labs

Design Featured Op Amp

OPA374	
V_{ss}	2.3V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1mV
I_q	585µA/Ch
I_b	0.5pA
UGBW	6.5MHz
SR	5V/µs
#Channels	1,2,4
www.ti.com/product/opa374	

Design Alternate Op Amp

TLV9061	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	0.538mA
I_b	0.5pA
UGBW	10MHz
SR	6.5V/µs
#Channels	1,2,4
www.ti.com/product/tlv9061	

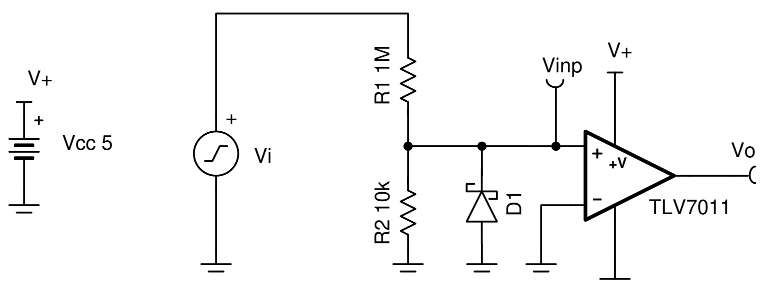
Zero Crossing Detection Using Comparator Circuit

Design Goals

Supply			Input Signal		MAX AC Mains Leakage Current
V_{cc}	V_{ee}	Type	V_i	f	I_{ac}
5 V	0 V	Single	240 V AC RMS	50 Hz	<500 μA

Design Description

The zero crossing detector circuit changes the comparator output state when the AC input crosses the zero reference voltage. This is done by setting the comparator inverting input to the zero reference voltage and applying the attenuated input to the noninverting input.The voltage divider R_1 and R_2 attenuates the input AC signal. The diode D_1 is used to insure the noninverting input never goes below the negative input common mode limit of the comparator. Zero crossing detection is often used in power control circuits.



Design Notes

1. Some hysteresis should be used to prevent unwanted transitions due to the slow speed of the input signal.
2. Select a comparator with a large input common mode range
3. The phase inversion protection feature of the TLV7011 can prevent phase reversal in situations where the input goes outside of the input common mode limits
4. A diode should be used to protect the comparator when the input goes below the negative input common mode limit.

Design Steps

1. Calculate the peak value of the input signal.

$$V_p = V_{RMS}\,X\,\sqrt{2} = 340V$$

2. Select the resistor divider to attenuate the input 340 V signal down to 3.4 V in order to be within the positive common range of the comparator.

$$340V\ x\ G = 3.4V$$

$$G = 0.01\frac{V}{V}$$

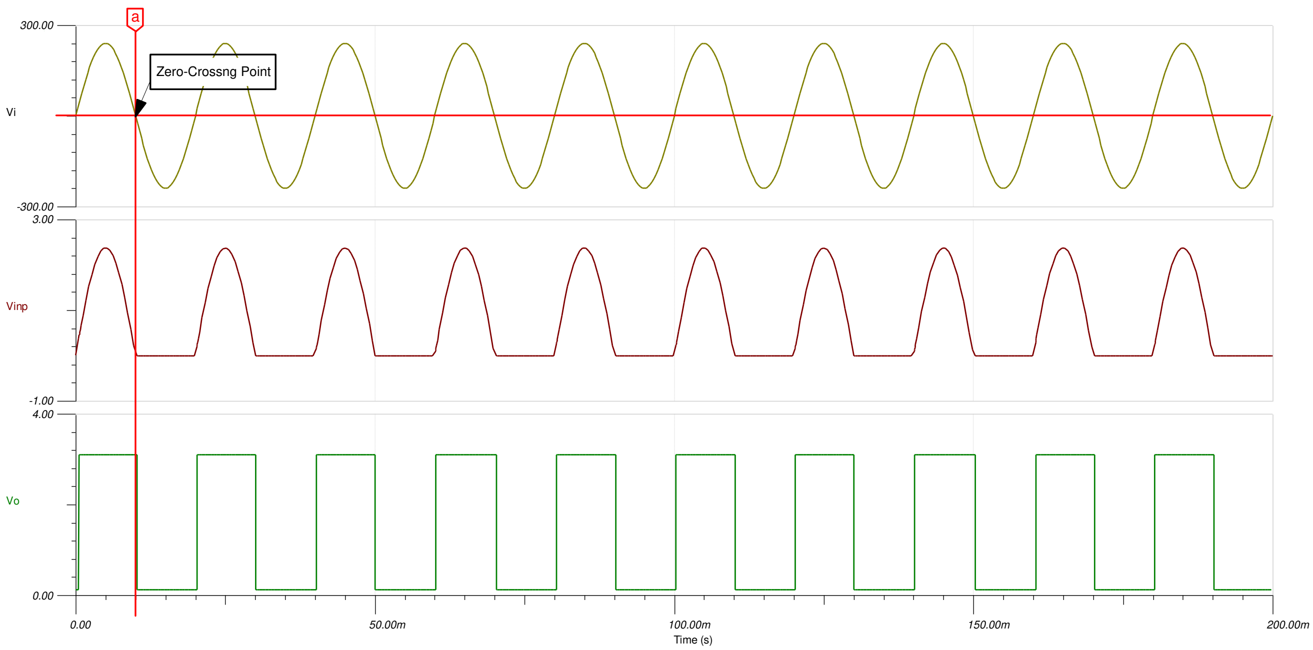
$$\left(\frac{R_2}{R_1+R_2}\right) = 0.01$$

3. Select R_1 as 1MΩ and R_2 as 10 kΩ (the closest 1% value).
4. Select the diode, D_1, in order to limit the negative voltage at the noninverting input. A zener diode with a voltage rating of 0.3 V can be used.
5. Calculate the AC mains leakage current to check if it meets the leakage current design goal of less than 500 μA.

$$I_{ac} = \frac{V_p}{R_1} = 340\mu A$$

Design Simulations

Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit spice simulation file, SBOMAP5.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, TI Precision Labs.

Design Featured Comparator

TLV7011	
V_{ss}	1.6 to 5.5V
V_{inCM}	Rail-to-rail
t_{pd}	260ns
V_{os}	0.5mV
V_{HYS}	4mV
I_q	5µA
Output Type	Push-Pull
#Channels	1
TLV7011	

Design Alternate Comparator

TLV3201	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
t_{pd}	40 ns
V_{os}	1 V
V_{HYS}	1.2 mV
I_q	40 µA
Output Type	Push-Pull
#Channels	1
TLV3201	

Window Comparator Circuit

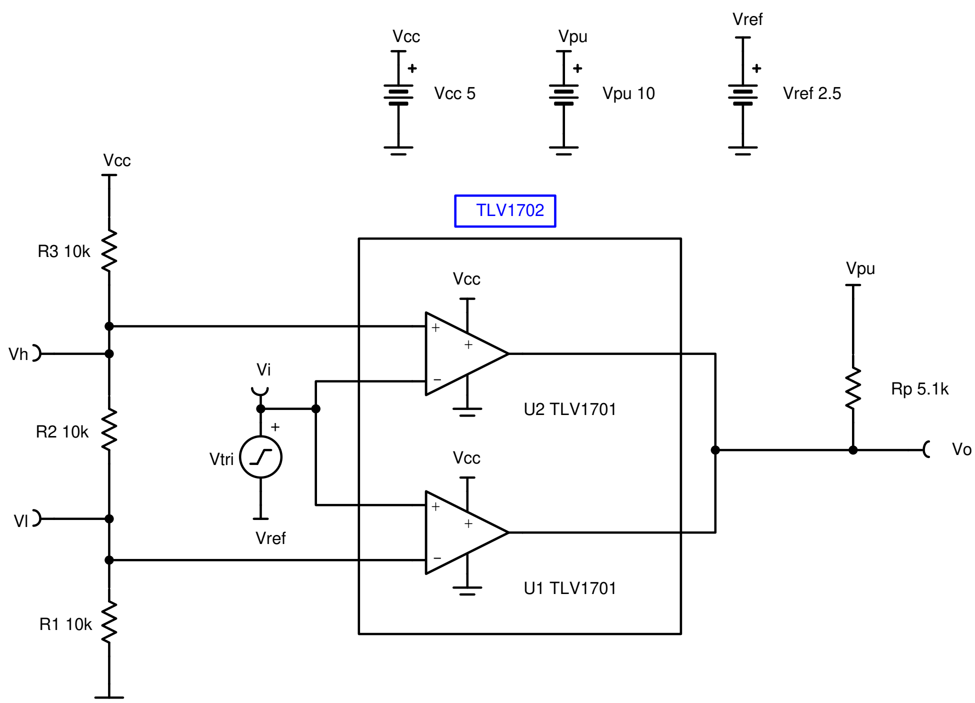
Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
0 V	5 V	0 V	36 V	5 V	0 V	2.5 V

V_L (Lower Threshold)	V_H (Upper Threshold)	Upper to Lower Threshold Ratio
1.66 V	3.33 V	2

Design Description

This circuit utilizes two comparators in parallel to determine if a signal is between two reference voltages. If the signal is within the window, the output is high. If the signal level is outside of the window, the output is low. For this design, the reference voltages are generated from a single supply with voltage dividers.



Design Notes

1. The input should not exceed the common mode limitations of the comparators.
2. If higher pullup voltages are used, R_p should be sized accordingly to prevent large current draw. The TLV1701 supports pullup voltages up to 36 V.
3. Comparator must be open-drain or open-collector to allow for the ORed output.

Design Steps

1. Define the upper (V_H) and lower (V_L) window voltages.

$$V_H = V_{cc} \times \frac{R_1 + R_2}{R_1 + R_2 + R_3} = 3.33\text{ V}$$

$$V_L = V_{cc} \times \frac{R_1}{R_1 + R_2 + R_3} = 1.66\text{ V}$$

$$\frac{V_H}{V_L} = 1 + \frac{R_2}{R_1} = \frac{3.33\text{V}}{1.66\text{V}} = 2$$

2. Choose resistor values to achieve the desired window voltages.

$$\frac{V_H}{V_L} = 1 + \frac{R_2}{R_1} = 2\text{, so } R_2 = R_1$$

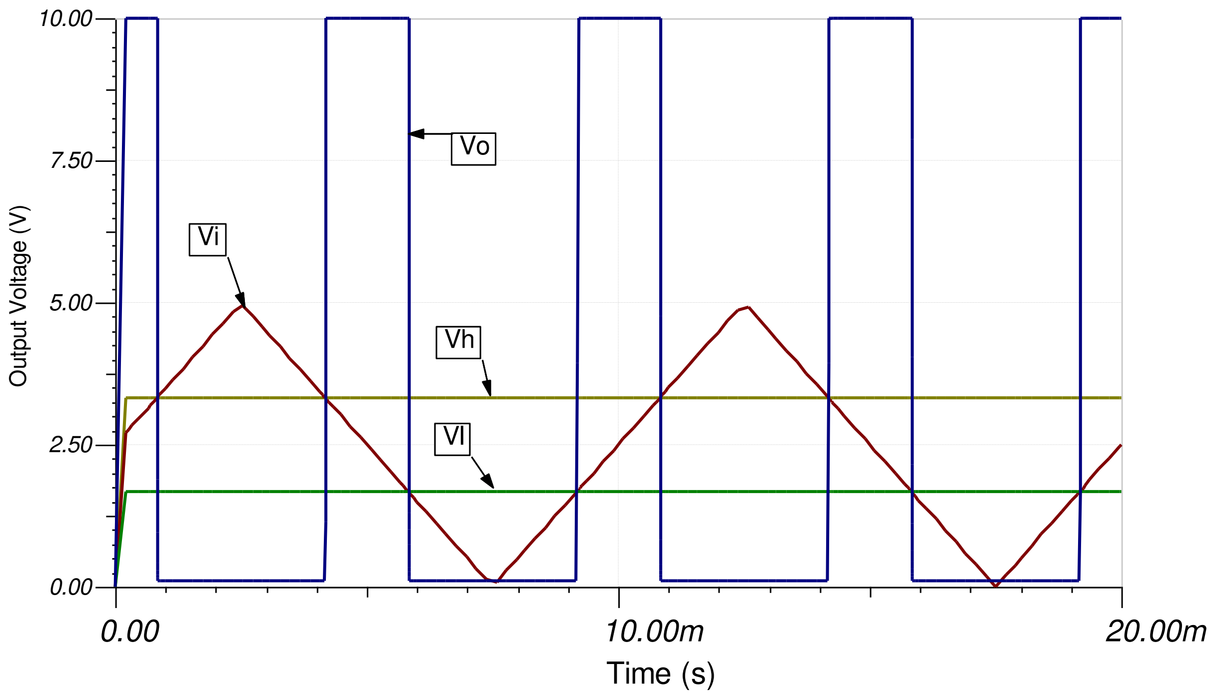
$$R_1 = R_2 = 10\text{k}\Omega\text{ (Selected standard values)}$$

$$R_3 = \frac{R_1 \times V_{cc}}{V_L} - \left(R_1 + R_2\right)$$

$$R_3 = \frac{10\text{k}\Omega \times 5\text{V}}{1.66\text{V}} - 20\text{k}\Omega = 10.12\text{ k}\Omega \approx 10\text{k}\Omega\text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC516.

See TIPD178.

Design Featured Op Amp

TLV1702	
V_{cc}	2.2 V to 36 V
V_{inCM}	Rail-to-rail
V_{out}	Open Collector (36 V Maximum)
V_{os}	2.5 mV
I_q	75 µA/Ch
I_b	15 nA
Rise Time	365 ns
Fall Time	240 ns
#Channels	1, 2, and 4
TLV1702	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 6, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file.	1

Analog Engineer's Circuit

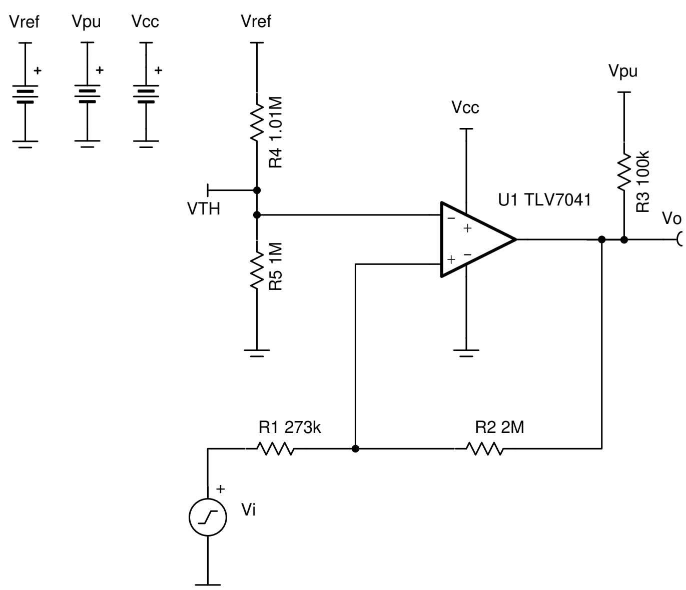
Non-Inverting Comparator with Hysteresis Circuit

Design Goals

Output		Thresholds			Supply		
V_o = HIGH	V_o = LOW	V_H	V_L	V_{HYS}	V_{cc}	V_{pu}	V_{ref}
$V_i > V_H$	$V_i < V_L$	1.7 V	1.3 V	400 mV	3 V	3 V	3 V

Design Description

Comparators are used to differentiate between two different signal levels. With noise, signal variation, or slow-moving signals, undesirable transitions at the output can be observed with a constant threshold. Setting upper and lower hysteresis thresholds eliminates these undesirable output transitions. This circuit example will focus on the steps required to design the positive feedback resistor network necessary to obtain the desired hysteresis for a non-inverting comparator application.

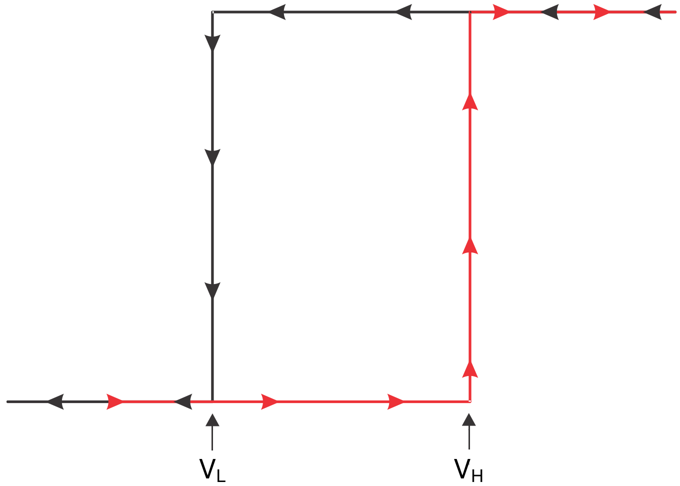


Design Notes

1. The accuracy of the hysteresis threshold voltages are related to the tolerance of the resistors used in the circuit, the selected comparator's input offset voltage specification, and any internal hysteresis of the device.
2. The TLV7041 has an open-drain output stage, so a pull-up resistor is needed.

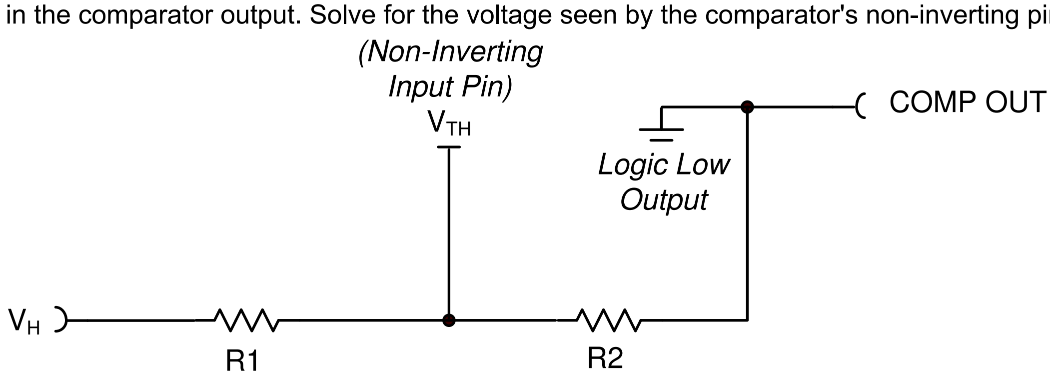
Design Steps

1. Select the switching thresholds for when the comparator will transition from high to low (V_L) and low to high (V_H). V_L is the necessary input voltage for the comparator output to transition low and V_H is the required input voltage for the comparator to output high.



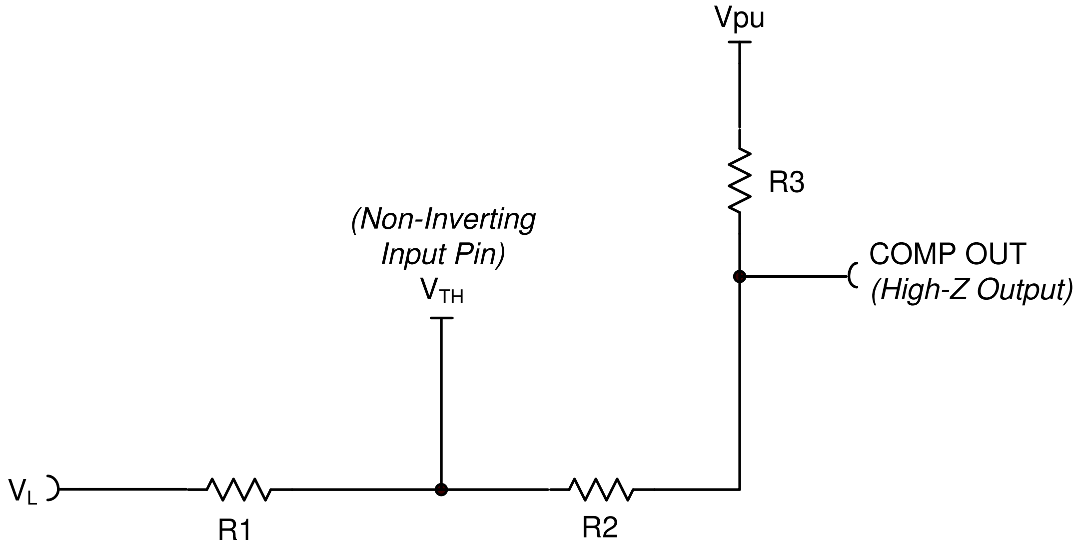
$$V_L = 1.3V \text{ and } V_H = 1.7V$$

2. Analyze the circuit when the input voltage is V_H. At this point, V_o=0V and the transition to a logic high is initiated in the comparator output. Solve for the voltage seen by the comparator's non-inverting pin, V_{TH}.



$$V_{TH} = V_H \times \left(\frac{R_2}{R_1 + R_2}\right)$$

3. Analyze the circuit when the input voltage is V_L. At this point, V_o=V_{pu} (or V_o=V_{cc} if the comparator has a push-pull output stage) and the transition to a logic low is initiated in the comparator output. Using superposition, solve for V_{TH}.



$$V_{TH} = V_L \times \left(\frac{R_2 + R_3}{R_1 + R_2 + R_3}\right) + V_{pu} \times \left(\frac{R_1}{R_1 + R_2 + R_3}\right)$$

4. Set R_2 to be large for power conservation. This resistance can be changed to meet certain design specifications but it was selected to be 2 MΩ. Now set the two V_{TH} equations equal and solve for R_1.

$$0 = (V_{PU}) \times {R_1}^2 + [V_{PU} \times R_2 + V_L \times (R_2 + R_3) - V_H \times R_2] \times R_1 + (V_L - V_H) \times \left({R_2}^2 + R_2 \times R_3\right)$$

$$R_1 = 273.19\text{k}\Omega \cong \mathbf{273k\Omega}$$

5. Calculate V_{TH} using the equation derived in step 2.

$$V_{TH} = V_H \times \left(\frac{R_2}{R_1 + R_2}\right)$$

$$V_{TH} = \mathbf{1.4958V}$$

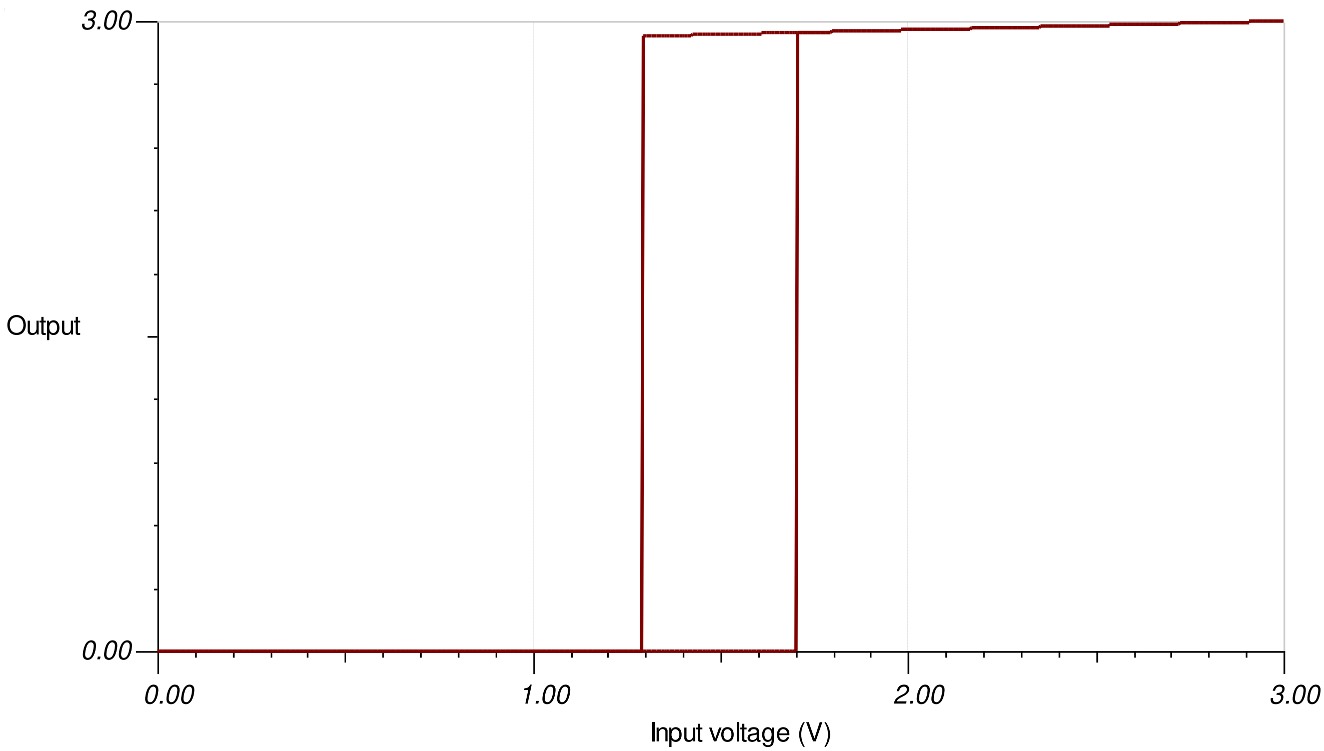
6. Assuming a value for R_5 of 1 MΩ for reduced power consumption, calculate R_4 using the following relationship developed from a basic voltage divider of the reference voltage V_{REF}. The voltage at the inverting terminal is V_{TH}.

$$V_{TH} = V_{REF} \times \left(\frac{R_5}{R_4 + R_5}\right)$$

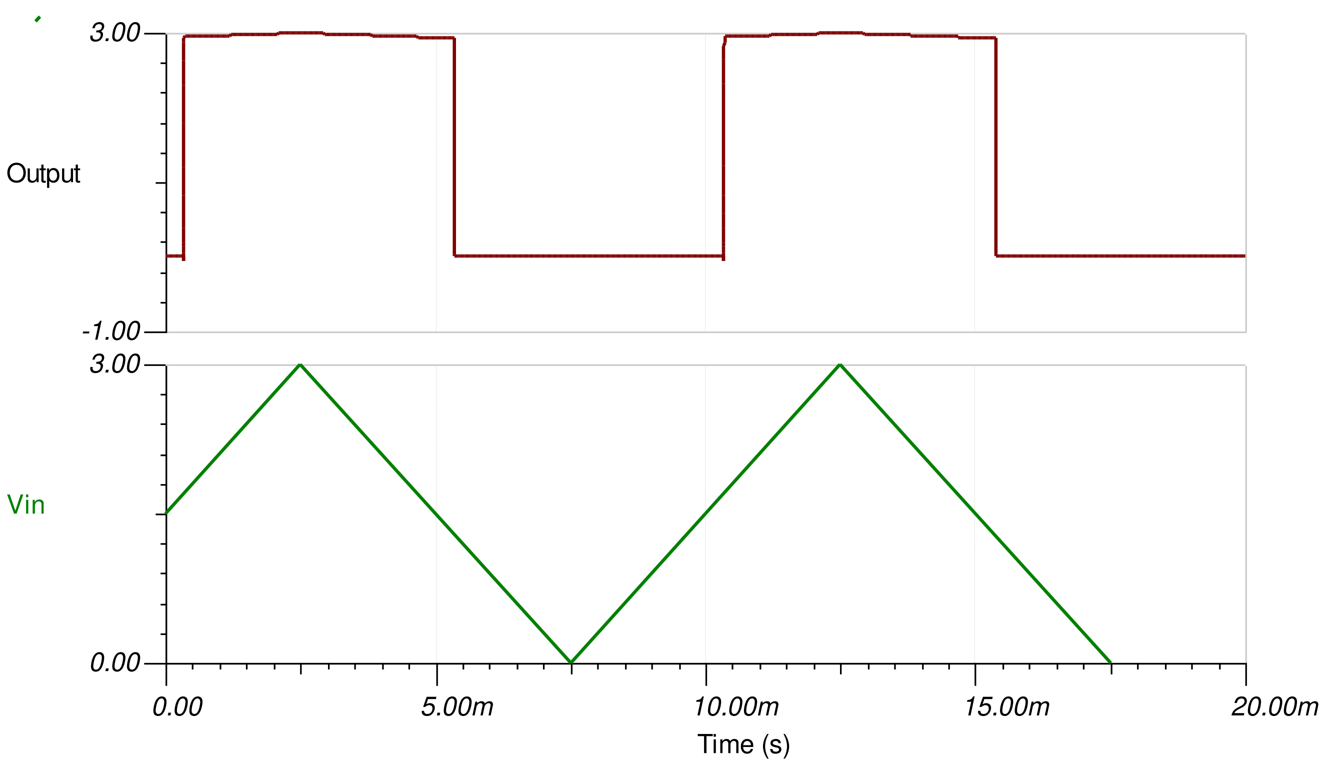
$$\Rightarrow R_4 = 1.0056\text{M}\Omega \cong \mathbf{1.01M\Omega}$$

Design Simulations

DC Transfer Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File SLVMCR2.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see TI Precision Labs - Op amps.

Design Featured Comparator

TLV7031, TLV7041	
Output Type	PP (7031), OD (7041)
V_{cc}	1.6 V to 6.5 V
V_{inCM}	Rail-to-rail
V_{os}	±100 µV
V_{HYS}	7 mV
I_q	335 nA/Ch
t_{pd}	3 µs
#Channels	1 and 2
TLV7041 Product Page	

Design Alternate Comparator

	TLV1701	TLV7011, TLV7011
Output Type	Open Collector	PP (7011), OD (7021)
V_{cc}	2.2 V to 36 V	1.6 V to 5.5 V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{HYS}	N/A	4.2 mV
V_{os}	±500 µV	±500 µV
I_q	55 µA/Ch	335 nA/Ch
t_{pd}	560 ns	3 µs
#Channels	1, 2, and 4	1 and 2
	TLV1701 Product Page	TLV7011 Product Page

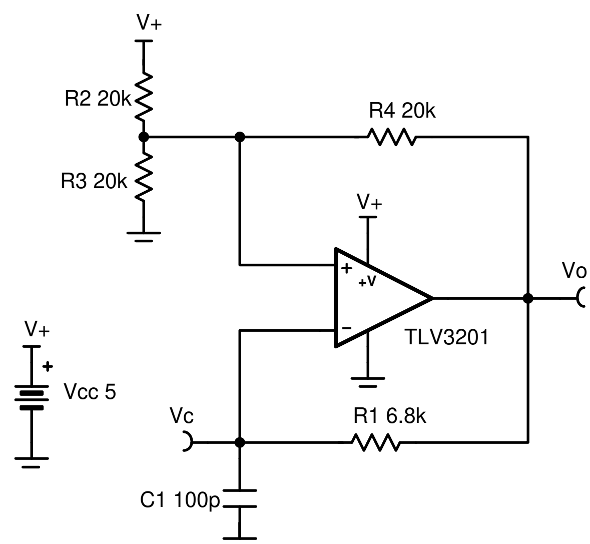
Relaxation Oscillator Circuit

Design Goals

Supply		Oscillator Frequency
V_{cc}	V_{ee}	f
5 V	0 V	1 MHz

Design Description

The oscillator circuit generates a square wave at a selected frequency. This is done by charging and discharging the capacitor, C_1 through the resistor, R_1. The oscillation frequency is determined by the RC time constant of R_1 and C_1, and the threshold levels set by the resistor network of R_2, R_3, and R_4. The maximum frequency of the oscillator is limited by the toggle rate of the comparator and the capacitance load at the output. This oscillator circuit is commonly used as a time reference or a supervisor clock source.



Design Notes

1. Comparator toggle rate and output capacitance are critical considerations when designing a high-speed oscillator.
2. Select C_1 to be large enough to minimize the errors caused by stray capacitance.
3. If using a ceramic capacitor, select a COG or NPO type for best stability over temperature.
4. Select lower value resistors for the R_2, R_3, R_4 resistor network to minimize the effects of stray capacitance.
5. R_2, R_3, and R_4 can be adjusted in order to create a duty cycle other than 50%.

Design Steps

1. When $R_2 = R_3 = R_4$, the resistor network sets the oscillator trip points of the non-inverting input at one-third and two-thirds of the supply.
2. When the output is high, the upper trip point will be set at two-thirds of the supply to bring the output back low.

$$V_o = V_s\left(\frac{R_3}{(R_2 \| R_4)+R_3}\right) = \frac{2}{3}V_s = 3.33V$$

3. When the output is low, the lower trip point will be set at one-third of the supply in order to bring the output back high.

$$V_o = V_s\left(\frac{R_3 \| R_4}{(R_3 \| R_4)+R_2}\right) = \frac{1}{3}V_s = 1.67V$$

4. The timing of the oscillation is controlled by the charging and discharging rate of the capacitor C_1 through the resistor R_1. This capacitor sets the voltage of the inverting input of the comparator. Calculate the time to discharge the capacitor.

$$V_c = V_i e^{-\frac{t}{R_1C_1}}$$

$$\frac{1.67}{3.33} = e^{-\frac{t}{R_1C_1}}$$

$$t = 0.69R_1C_1$$

5. Calculate the time to charge the capacitor.

$$V_i = V_c\left(1\text{-}e^{-\frac{t}{RC}}\right)$$

$$1.67 = 3.33\left(1\text{-}e^{-\frac{t}{RC}}\right)$$

$$\frac{1.67}{3.33} = e^{-\frac{t}{RC}}$$

$$t = 0.69R_1C_1$$

6. The time for the capacitor to charge or discharge is given by $0.69R_1C_1$. With a target oscillator frequency of 1 MHz, the time to charge or discharge should be 500 ns.

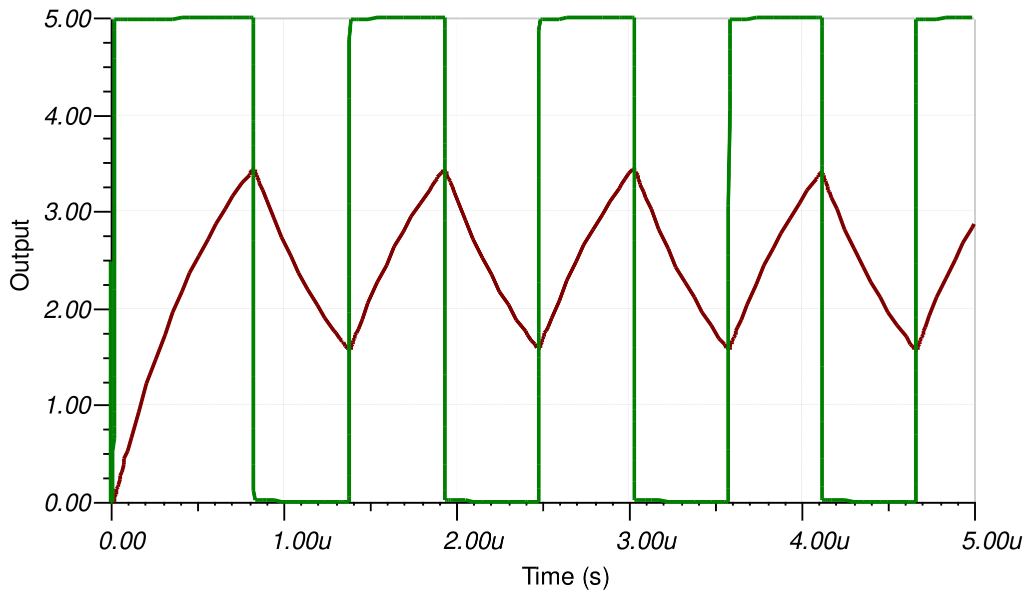
$$0.69R_1C_1 = 500ns$$

$$R_1C_1 = 724ns$$

7. Select C_1 as 100 pF and R_1 as 6.8 kΩ (the closest real world value).

Design Simulations

Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit spice simulation file, SBOMAO3.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, TI Precision Labs.

Design Featured Comparator

TLV3201	
V_{ss}	2.7 V to 5.5 V
V_{inCM}	Rail-to-rail
t_{pd}	40 ns
V_{os}	1 mV
V_{HYS}	1.2 mV
I_q	40 µA
Output Type	Push-Pull
#Channels	1
TLV3201	

Design Alternate Comparator

TLV7011	
V_{ss}	1.6 V to 5.5 V
V_{inCM}	Rail-to-rail
t_{pd}	260 ns
V_{os}	0.5 V
V_{HYS}	4 mV
I_q	5 µA
Output Type	Push-Pull
#Channels	1
TLV7011	

Inverting Comparator With Hysteresis Circuit

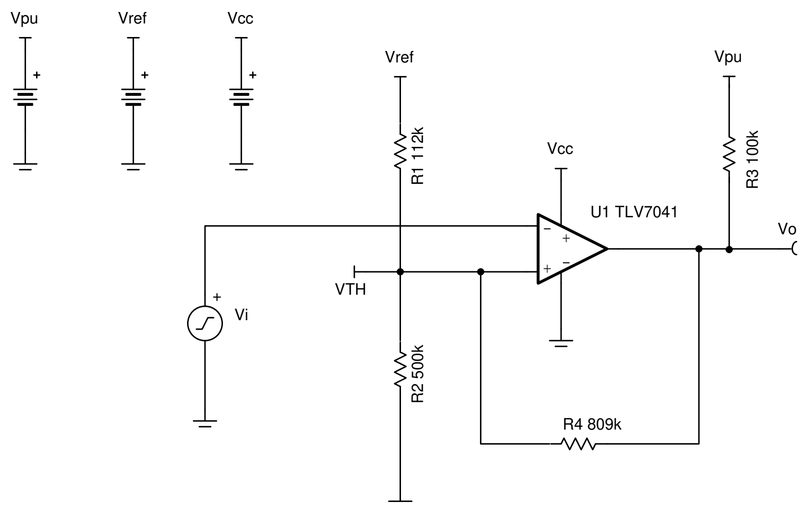
TEXAS INSTRUMENTS

Design Goals

Output		Thresholds			Supply		
V_0 = HIGH	V_o = LOW	V_H	V_L	V_{HYS}	V_{cc}	V_{PU}	V_{ref}
$V_i < V_L$	$V_i > V_H$	2.5 V	2.2 V	300 mV	3 V	3 V	3 V

Design Description

Comparators are used to differentiate between two different signal levels. With noise, signal variation, or slow-moving signals, undesirable transitions at the output can be observed with a constant threshold. Setting upper and lower hysteresis thresholds eliminates these undesirable output transitions. This circuit example will focus on the steps required to design the positive feedback resistor network necessary to obtain the desired hysteresis for an inverting comparator application.



Design Notes

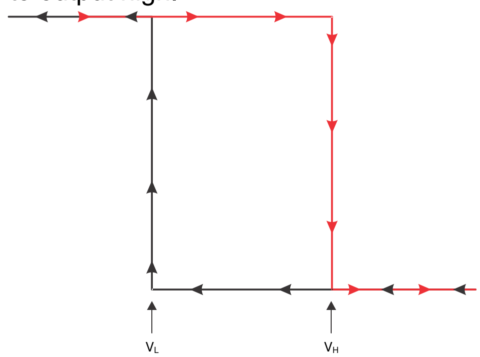
1. The accuracy of the hysteresis threshold voltages are related to the tolerance of the resistors used in the circuit, the selected comparator’s input offset voltage specification, and any internal hysteresis of the device.
2. The TLV7041 has an open-drain output stage, so a pull-up resistor is needed.

Design Steps

1. Select the lower biasing resistor, R_2. This resistor can be modified for any design. In this case, it is assumed that power conservation is necessary, therefore, R_2 is selected to be large.

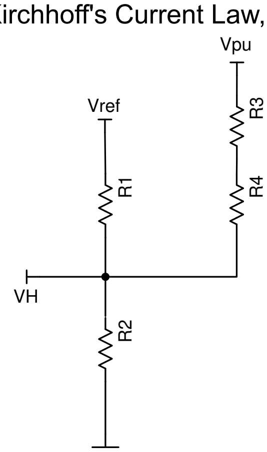
$$R_2 = 500k\,\Omega$$

2. Select the switching thresholds for when the comparator will transition from high to low (V_L) and low to high (V_H). V_L is the necessary input voltage for the comparator output to transition low and V_H is the required input voltage for the comparator to output high.



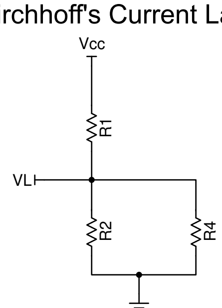
$$V_L\text{=2.2V and } V_H\text{= 2.5V}$$

3. Analyze the circuit when the input voltage is V_H. At this point, V_o=3 V=V_{PU} and the transition to a logic low is initiated in the comparator output. Using Kirchhoff's Current Law, solve for an equation for R_1.



$$\frac{V_{PU} - V_H}{R_3 + R_4} + \frac{V_{REF} - V_H}{R_1} = \frac{V_H}{R_2} \Rightarrow R_1 = \frac{V_{REF} - V_H}{\frac{V_H}{R_2} - \frac{V_{PU} - V_H}{R_3 + R_4}}$$

4. Analyze the circuit when the input voltage is V_L. At this point, V_o=0 V and the transition to a logic high is initiated in the comparator output. Using Kirchhoff's Current Law, solve for an equation for R_1.



$$\frac{V_{REF} - V_L}{R_1} = \frac{V_L}{R_2} + \frac{V_L}{R_4} \Rightarrow R_1 = \frac{V_{REF} - V_L}{V_L \times \left(\frac{R_2 + R_4}{R_2 R_4}\right)}$$

5. After defining some constants, set the two equations for R_1 equal to obtain a quadratic equation for R_4.
   a. **Constants:**

$$A = \frac{V_{REF}}{V_L} - 1$$

$$B = V_{REF} - V_H$$

$$C = \frac{V_H}{R_2}$$

$$D = V_{PU} - V_H$$

Simplified Quadratic for R_4:

$$\left(\frac{B}{A} - C \times R_2\right) \times {R_4}^2 + \left[\frac{B}{A} \times (R_2 + R_3) - C \times R_2 \times R_3 + D \times R_2\right] \times R_4 + \left(\frac{B}{A} \times R_2 \times R_3\right) = 0$$

   b. If the output stage is push-pull, then make the following modifications to the above equations:

$$R_3 = 0$$

$$V_{PU} = V_{CC}$$

$$D = V_{CC} - V_H$$

6. Solve the quadratic equation for R_4 and pick the most logical result.

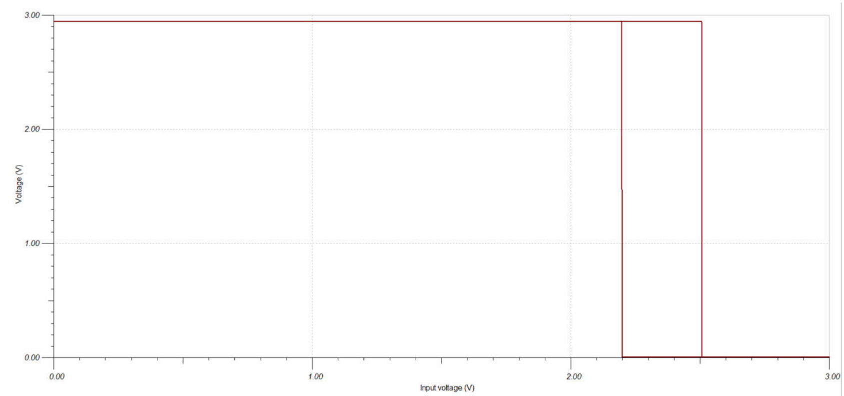
$$R_4 = 808.88\text{k}\Omega \cong 809\text{k}\Omega$$

7. Calculate R_1 by substituting the value for the *A* constant into the equation for R_1 found in step 4.

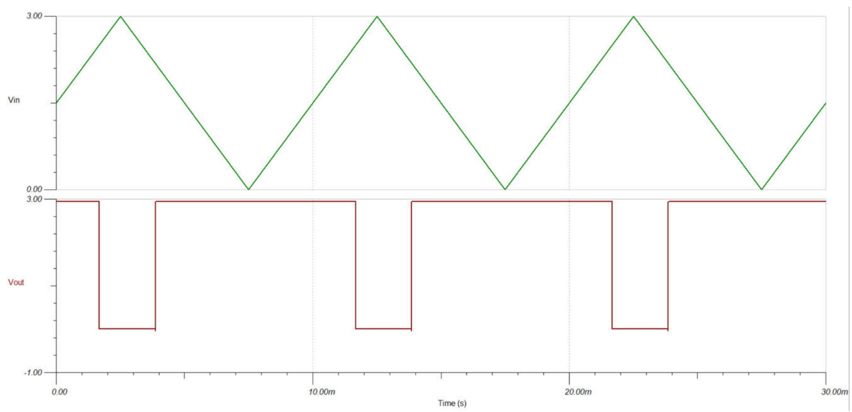
$$R_1 = \frac{V_{REF} - V_L}{V_L \times \left(\frac{R_2 + R_4}{R_2 R_4}\right)} = \left(\frac{V_{REF}}{V_L} - 1\right) \times \left(\frac{R_2 \times R_4}{R_2 + R_4}\right) = A \times \left(\frac{R_2 \times R_4}{R_2 + R_4}\right)$$

$$R_1 = 112.36\text{k}\Omega \cong 112\text{k}\Omega$$

DC Transfer Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Comparator with Hysteresis Reference Design TIPD144.

See Circuit SPICE Simulation File SLVMCQ0, Inverting Comparator with Hysteresis Circuit Reference Design.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see TI Precision Labs – Op amps.

Design Featured Comparator

TLV7031 / TLV7041	
Output Type	PP (7031) / OD (7041)
V_{cc}	1.6V to 6.5V
V_{inCM}	Rail-to-rail
V_{os}	±100 µV
V_{HYS}	7 mV
I_q	335 nA/Ch
t_{pd}	3 µs
#Channels	1 and 2
TLV7041	

Design Alternate Comparator

	TLV1701	TLV7011 / TLV7021
Output Type	Open Collector	PP (7011) / OD (7021)
V_{cc}	2.2 V to 36 V	1.6 V to 5.5 V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{HYS}	N/A	4.2 mV
V_{os}	±500 µV	±500 µV
I_q	55 µA/Ch	5 µA
t_{pd}	560 ns	260 ns
#Channels	1, 2, and 4	1 and 2
	TLV1701	TLV7011

Overvoltage Protection with Comparator Circuit

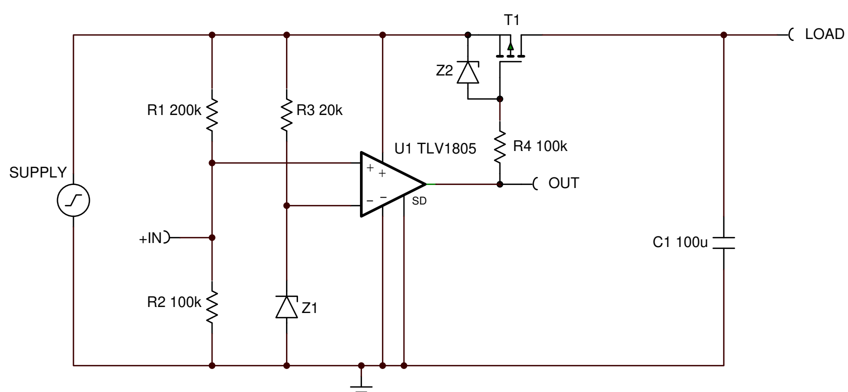
TEXAS INSTRUMENTS

Design Goals

Supply	Load	Comparator Output Status (OUT)	
Operating Voltage Range	MAX Operating Voltage (V_{OVER})	SUPPLY < V_{OVER}	SUPPLY ≥ V_{OVER}
12 V to 36 V	30 V	V_{OL} < 0.4 V	V_{OH} = SUPPLY

Design Description

This overvoltage protection circuit uses a high-voltage comparator with a push-pull output stage to control a P-Channel MOSFET that connects the SUPPLY to the LOAD. When the SUPPLY voltage exceeds the overvoltage threshold (V_{OVER}), the output of the comparator goes HIGH and disconnects the LOAD from the SUPPLY by opening the P-Channel MOSFET. Likewise, when the SUPPLY voltage is below V_{OVER}, the output of the comparator is LOW and connects the LOAD to the SUPPLY.



Design Notes

1. Select a high-voltage comparator with a push-pull output stage.
2. Select a reference voltage that is below the lowest operating voltage range for the SUPPLY.
3. Calculate values for the resistor divider so the critical overvoltage level occurs when the input to the comparator (+IN) reaches the comparator's reference voltage.
4. Limit the source-gate voltage of the P-Channel MOSFET so that it remains below the device's maximum allowable value.

Design Steps

1. Select a high-voltage comparator with a push-pull output stage that can operate at the highest possible SUPPLY voltage. In this application, the highest SUPPLY voltage is 36 V.
2. Determine an appropriate reference level for the overvoltage detection circuit. Since the lowest operating voltage for the SUPPLY is 12 V, a 10 V zener diode (Z_1) is selected for the reference (V_{REF}).
3. Calculate value of R3 by considering the minimum bias current to keep the Z_1 regulating at 10V. A minimum bias current of 100 µA is used along with the minimum SUPPLY voltage of 12 V.

$$R_3 = \frac{\text{SUPPLY}\ \ (\min) - V_{ZENER}}{I_{BIAS}\ \ (\min)} = \frac{12V - 10V}{100\mu A} = 20\ \ k\Omega$$

4. Calculate the resistor divider ratio needed so the input to the comparator (+IN) crosses the reference voltage (10 V) when the SUPPLY rises to the target overvoltage level (V_{OVER}) of 30 V.

$$V_{REF} = V_{OVER} \times \left(\frac{R_2}{R_1 + R_2}\right)$$

$$\left(\frac{R_2}{R_1 + R_2}\right) = \frac{V_{REF}}{V_{OVER}} = \frac{10V}{30V} = 0.333$$

5. Select values for R_1 and R_2 that yield the resistor divider ratio of 0.333 V by using the following equation or using the online at *Voltage Divider Calculator*.
   If using the following equation, choose a value for R_2 in the 100 kΩ range and calculate for R_1. In this example, a value of 100 k was chosen for R_2.

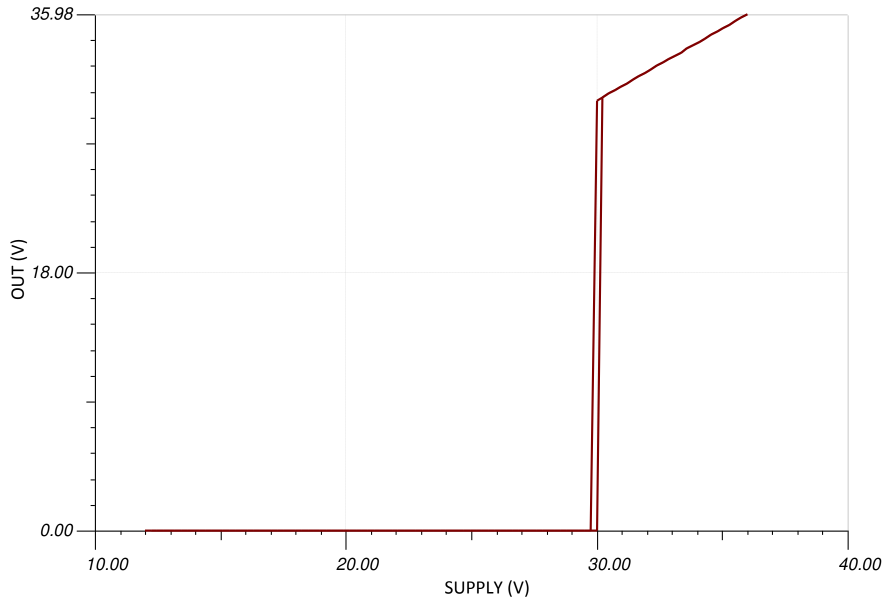
$$R_1 = R_2\left(\frac{V_{OVER}}{V_{REF}} - 1\right) = 100\ \ k\Omega\ \ \left(\frac{30V}{10V} - 1\right) = 200\ \ k\Omega$$

6. Note that the TLV1805 which is used in application circuit has 15 mV of hysteresis. This means that the actual switching threshold will be 7.5 mV higher than the switching threshold (VREF) when the SUPPLY is rising and 7.5 mV lower when the SUPPLY is falling. The result of the hysteresis is most easily seen in the DC Simulation curve. Since SUPPLY is resistor divided down by a factor of 3, the net impact to the SUPPLY switching threshold is 3 times this amount.
7. Verify that the current through the resistor divider is at least 100 times higher than the input bias current of the comparator. The resistors can have high values to minimize power consumption in the circuit without adding significant error to the resistor divider.
8. Select a zener diode (Z_2) to limit the source-gate voltage (V_{SG}) of the P-Channel MOSFET so that it remains below the device's maximum allowable value. It is common for P-Channel, power MOSFETs to have a V_{SG} max value of 20 V, so a 16 V zener is placed from source to gate.
9. Calculate a value for the current limiting resistor (R_4). When SUPPLY rises above 16 V and Z_2 begins to conduct, R_4 limits the amount of current that the comparator output will sink when its output is LOW. With a nominal SUPPLY voltage of 24 V, the sink current is limited to 80 µA.

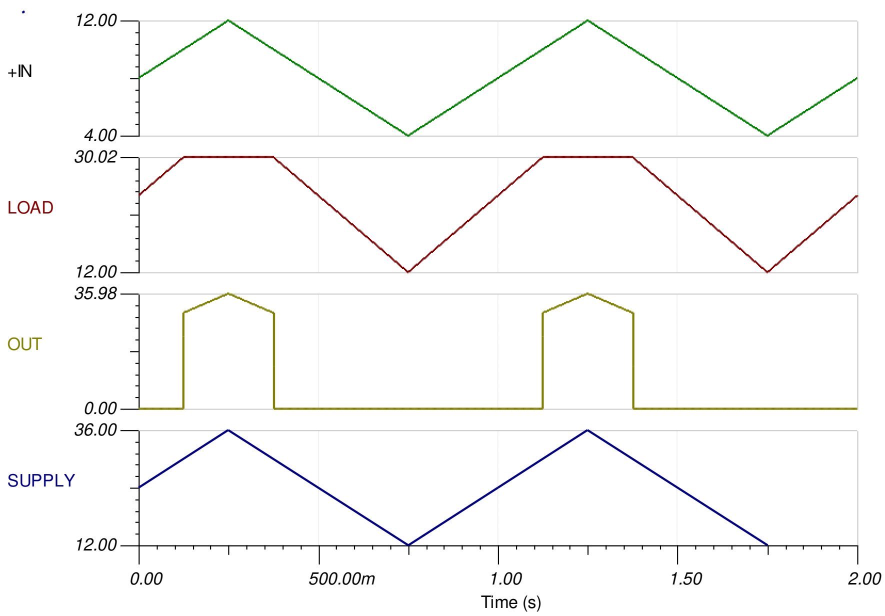
$$I_{SINK} = \left(\frac{\text{SUPPLY}\ \ -\ \ V_{Z2}}{R_4}\right) = \left(\frac{24V - 16V}{100\ \ k\Omega}\right) = 80\ \ \mu A$$

Design Simulations

DC Simulation Results



Transient Simulation Results



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SNOAA20
3. TI Precision Labs

Design Featured Comparator

TLV1805-Q1 / TLV1805	
V_S	3.3 V to 40 V
V_{inCM}	Rail-to-rail
V_{OUT}	Push-Pull
V_{OS}	500 µV
Hysteresis	15 mV
I_Q	135 µA
$t_{PD(HL)}$	250 ns
TLV1805	

Design Alternate Comparator

	TLV3701 / TLV370x-Q1	TLC3702 / TLC3702-Q1
V_S	2.5 V to 16 V	4 V to 16 V
V_{inCM}	Rail-to-rail	-1 V from VDD
V_{OUT}	Push-Pull	Push-Pull
V_{OS}	250 µV	1.2 mV
Hysteresis	n/a	n/a
I_Q	0.56 µA	9.5 µA/Ch
$t_{PD(HL)}$	36 µs	0.65 µs
	TLV3701	TLC3702

Analog Engineer's Circuit
Comparator with and without Hysteresis Circuit

TEXAS INSTRUMENTS

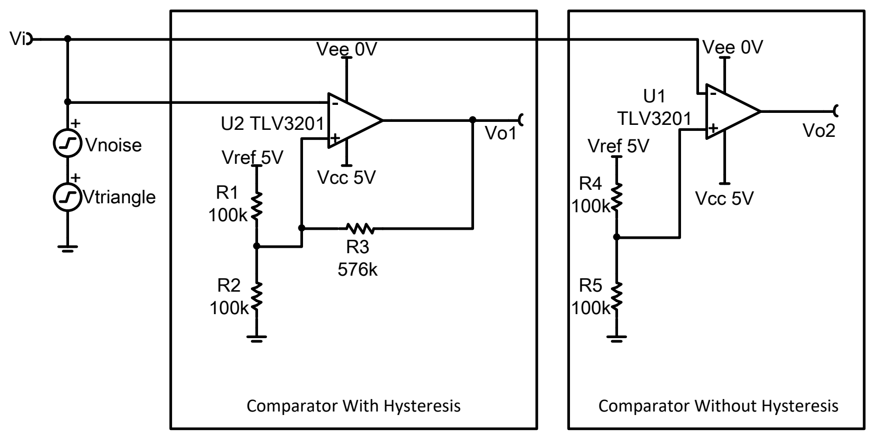
Design Goals

Input		Output		Supply		
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
0 V	5 V	0 V	5 V	5 V	0 V	5 V

V_L (Lower Threshold)	V_H (Upper Threshold)	$V_H - V_L$
2.3 V	2.7 V	0.4 V

Design Description

Comparators are used to compare two different signal levels and create an output based on the input with the higher input voltage. Noise or signal variation at the comparison threshold will cause the comparator output to have multiple output transitions. Hysteresis sets upper- and lower-threshold voltages to eliminate the multiple transitions caused by noise.



Design Notes

1. Use a comparator with low quiescent current to reduce power consumption.
2. The accuracy of the hysteresis threshold voltages are related to the tolerance of the resistors used in the circuit.
3. The propagation delay is based on the specifications of the selected comparator.

Design Steps

1. Select components for the comparator with hysteresis.
   a. Select V_L, V_H, and R_1.

   $$V_L = 2.3V$$

   $$V_H = 2.7V$$

   $$R_1 = 100k\Omega \text{ (Standard Value)}$$

   b. Calculate R_2.

   $$R_2 = \frac{V_L}{V_{cc} - V_H} \times R_1 = \frac{2.3V}{5V - 2.7V} \times 100k\Omega = 100k\Omega \text{ (Standard Value)}$$

   c. Calculate R_3.

   $$R_3 = \frac{V_L}{V_H - V_L} \times R_1 = \frac{2.3V}{2.7V - 2.3V} \times 100k\Omega = 575k\Omega \approx 576k\Omega \text{ (Standard Value)}$$

   d. Verify hysteresis width.

   $$V_H - V_L = \frac{R_1 \times R_2}{(R_3 \times R_1) + (R_3 \times R_2) + (R_1 \times R_2)} \times V_{cc}$$

   $$= \frac{100k\Omega \times 100k\Omega}{(576k\Omega \times 100k\Omega) + (576k\Omega \times 100k\Omega) + (100k\Omega \times 100k\Omega)} \times 5V = 0.399V$$

2. Select components for comparator without hysteresis.
   a. Select V_{th} and R_4 .

   $$V_{th} = 2.5V$$

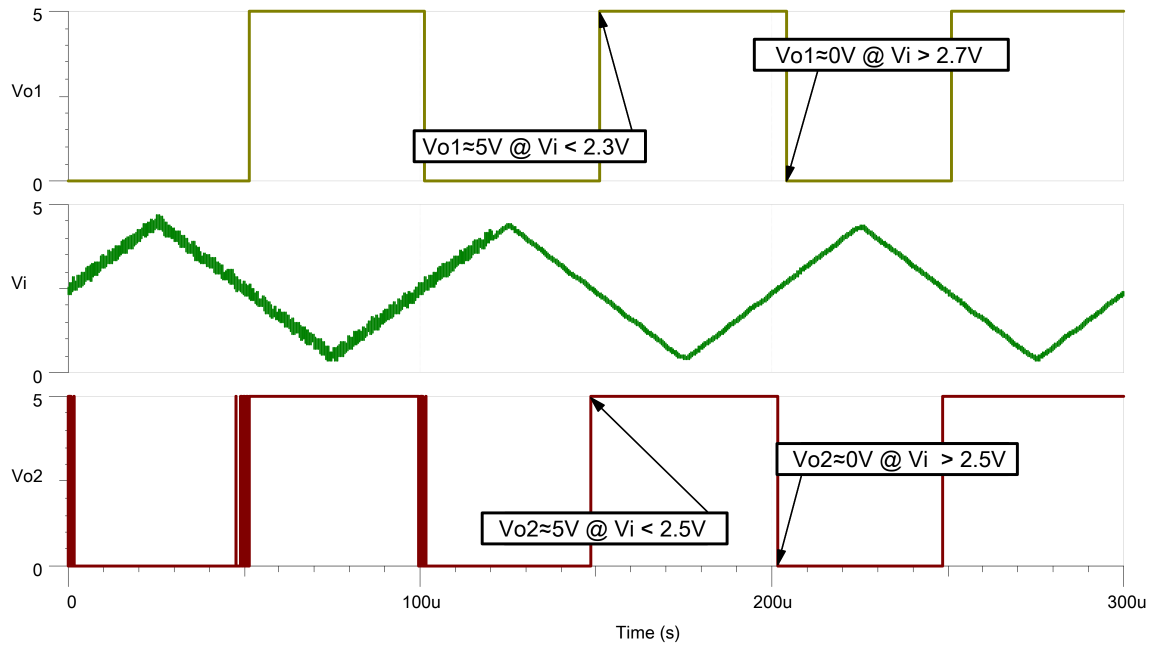
   $$R_4 = 100k\Omega \text{ (Standard Value)}$$

   b. Calculate R_5.

   $$R_5 = \frac{V_{th}}{V_{cc} - V_{th}} \times R_4 = \frac{2.5V}{5V - 2.5V} \times 100k\Omega = 100k\Omega \text{ (Standard Value)}$$

Design Simulations

Transient Simulation Results



Noise Only Present From 0 s to 120 µs

Zoomed in From 40µs to 110µs

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC515.

See TIPD144.

Design Featured Comparator

TLV3201	
V_{cc}	2.7 V to 5.5 V
V_{inCM}	Extends 200 mV beyond either rail
V_{out}	(V_{ee}+230 mV) to (V_{cc}–210 mV) at 4 mA
V_{os}	1 mV
I_q	40 µA
I_b	1 pA
UGBW	—
SR	—
#Channels	1 and 2
www.ti.com/product/tlv3201	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019	Page
• Downscale the title and changed title role to 'Amplifiers'. Added links to circuit cookbook landing page and SPICE simulation file	1

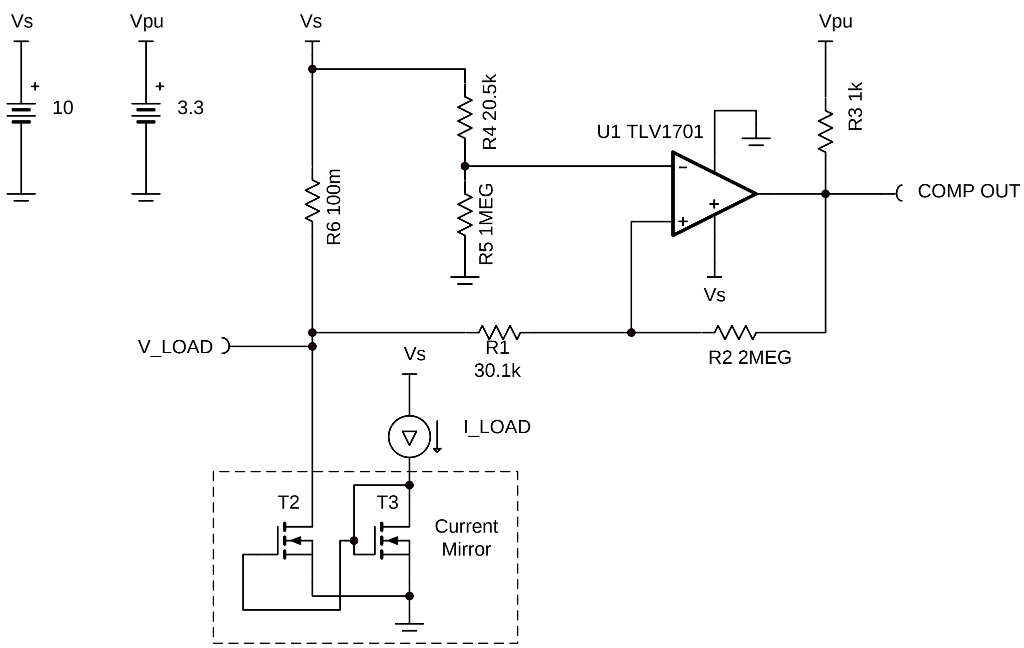
High-side current sensing with comparator circuit

Design Goals

Load Current (I_L)		System Supply (V_S)	Comparator Output Status	
Over Current (I_{OC})	Recovery Current (I_{RC})	Typical	Over Current	Normal Operation
1 A	0.5 A	10 V	V_{OL} < 0.4 V	V_{OH} = V_{PU} = 3.3 V

Design Description

This high-side, current sensing solution uses one comparator with a rail-to-rail input common mode range to create an over-current alert (OC-Alert) signal at the comparator output (COMP OUT) if the load current rises above 1A. The OC-Alert signal in this implementation is active low. So when the 1A threshold is exceeded, the comparator output goes low. Hysteresis is implemented such that OC-Alert will return to a logic high state when the load current reduces to 0.5A (a 50% reduction). This circuit utlizes an open-drain output comparator in order to level shift the output high logic level for controlling a digital logic input pin. For applications needing to drive the gate of a MOSFET switch, a comparator with a push-pull output is preferred.



Design Notes

1. Select a comparator with rail-to-rail input common mode range to enable high-side current sensing.
2. Select a comparator with an open-drain output stage for level-shifting.
3. Select a comparator with low input offset voltage to optimize accuracy.
4. Calculate the value for the shunt resistor (R_6) so the shunt voltage (V_{SHUNT}) is at least ten times larger than the comparator offset voltage (V_{IO}).

Design Steps

1. Select value of R_6 so V_{SHUNT} is at least 10x greater than the comparator input offset voltage (V_{IO}). Note that making R_6 very large will improve OC detection accuracy but will reduce supply headroom.

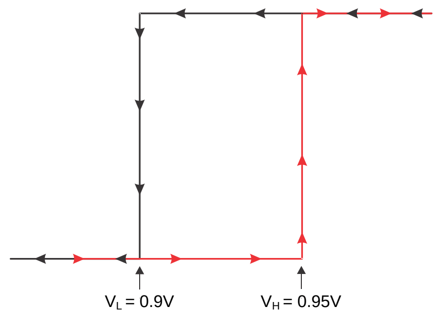
   $V_{SHUNT} = (I_{OC} \times R_6) \geq 10 \times V_{IO} = 55mV$

   $\text{set} \quad R_6 = 100m\Omega \quad \text{for} \quad I_{OC} = 1A \quad \& \quad V_{IO} = 5.5mV$

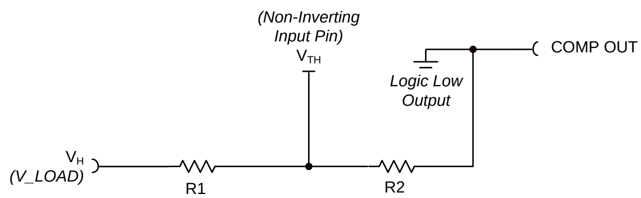
2. Determine the desired switching thresholds for when the comparator output will transition from high-to-low (V_L) and low-to-high (V_H). V_L represents the threshold when the load current crosses the OC level, while V_H represents the threshold when the load current recovers to a normal operating level.

   $V_L = V_S - (I_{OC} \times R_6) = 10 - (1 \times 0.1) = 0.9V$

   $V_H = V_S - (I_{RC} \times R_6) = 10 - (0.5 \times 0.1) = 0.95V$

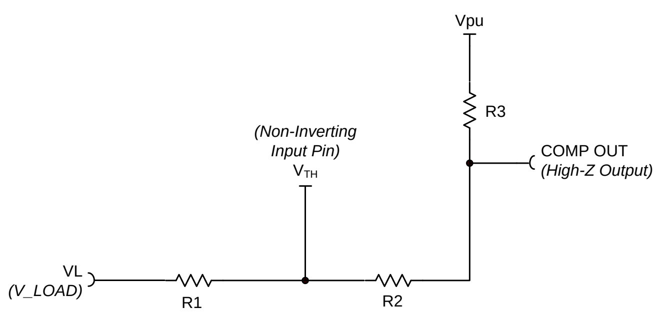


3. With the non-inverting input pin of the comparator labeled as V_{TH} and the comparator output in a logic low state (ground), derive an equation for V_{TH} where V_H represents the load voltage (V_{LOAD}) when the comparator output transitions from low to high. Note that the simplified diagram for deriving the equation shows the comparator output as ground (logic low).



   $V_{TH} = V_H \times \left(\frac{R_2}{R_1 + R_2}\right)$

4. With the non-inverting input pin of the comparator labeled as V_{TH} and the comparator output in a high-impedance state, derive an equation for V_{TH} where V_L represents the load voltage (V_{LOAD}) when the comparator output transitions from high to low. Applying "superposition" theory to solve for V_{TH} is recommended.



   $V_{TH} = V_L \times \left(\frac{R_2 + R_3}{R_1 + R_2 + R_3}\right) + V_{PU} \times \left(\frac{R_1}{R_1 + R_2 + R_3}\right)$

5. Eliminate variable V_{TH} by setting the two equations equal to each other and solve for R_1. The result is the following quadratic equation. Solving for R_2 is less desirable since there are more standard values for small resistor values than the larger ones.

   $0 = (V_{PU}) \times R_1^2 + (V_{PU} \times R_2 + V_L \times (R_3 + R_2) - V_H \times R_2) \times R_1 + (V_L - V_H) \times (R_2^2 + R_2 \times R_3)$

6. Calculate R_1 after substituting in numeric values for V_{PU}, R_2, V_L, V_H, and R_3. For this design, set V_{PU}=3.3, R_2=2M, V_L=9.9, V_H=9.95, and R_3=1k. Please note that R_3 is significantly smaller than R_2 (R_3<<R_2). Increasing R_3 will cause the comparator logic high output level to increase beyond V_{PU} and should be avoided. For example, increasing R_3 to a value of 100k can cause the logic high output to be 3.6V.

   $$0 = (3.3) \times R_1^2 + (6.591M) \times R_1 - (200.1G)$$
   $$\text{the positive root for } R_1 = 29.9k\Omega$$
   $$\text{using standard 1\% resistor values, } R_1 = 30.1k\Omega$$

7. Calculate V_{TH} using the equation derived in Design Step 3; use the calculated value for R_1. Note that V_{TH} is less than V_L since V_{PU} is less that V_L.

   $$V_{TH} = V_H \times \left(\frac{R_2}{R_1 + R_2}\right) = 9.802V$$

8. With the inverting terminal labeled as V_{TH}, derive an equation for V_{TH} in terms of R_4, R_5, and V_S.

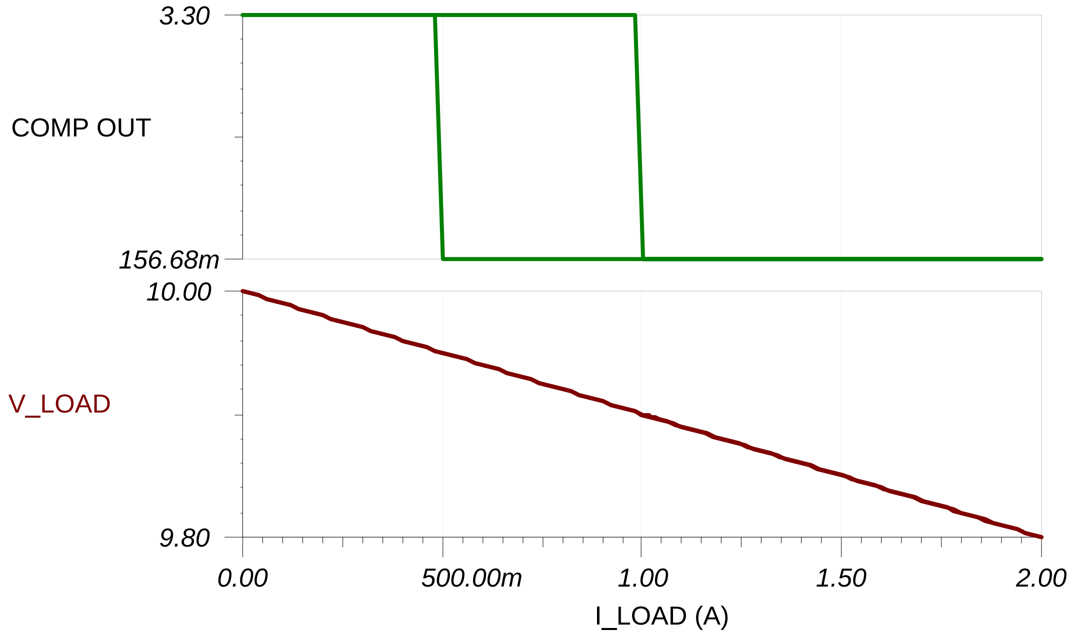
   $$V_{TH} = V_S \times \left(\frac{R_5}{R_4 + R_5}\right)$$

9. Calculate R_4 after substituting in numeric values R_5=1M, V_S=10, and the calculated value for V_{TH}.

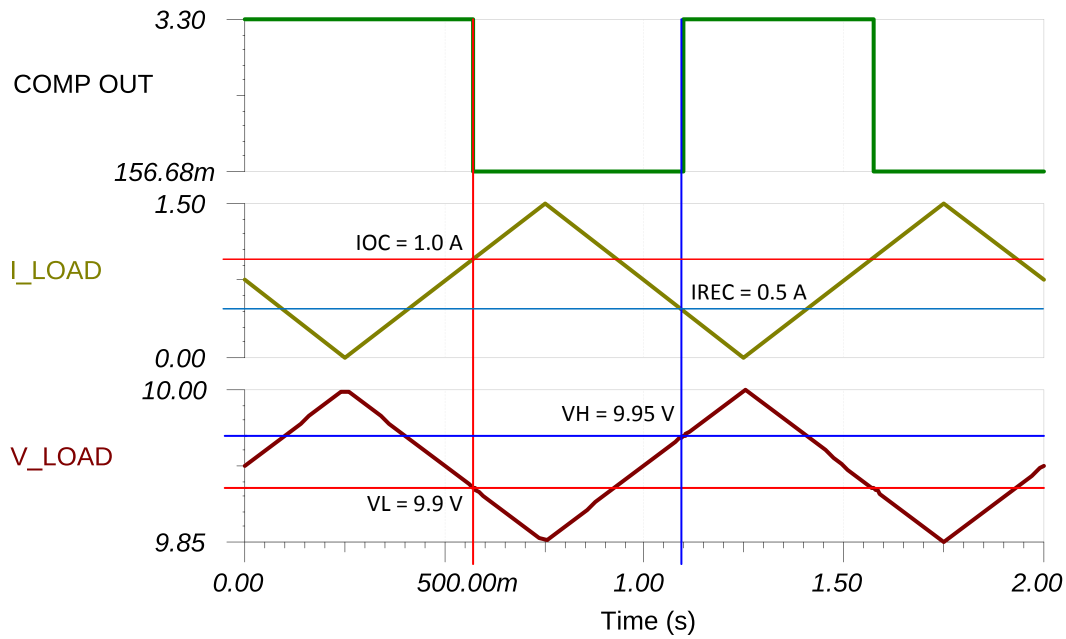
   $$R_4 = \left(\frac{R_5 \times (V_S - V_{TH})}{V_{TH}}\right) = 20.15k\Omega$$
   $$\text{using standard 1\% resistor values, } R_4 = 20.5k\Omega$$

Design Simulations

DC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File SLOM456, http://www.ti.com/lit/zip/slom456.

Design Featured Comparator

TLV170x-Q1, TLV170x	
V_S	2.2 V to 36 V
V_{inCM}	Rail-to-rail
V_{OUT}	Open-Drain, Rail-to-rail
V_{OS}	500µV
I_Q	55 µA/channel
$t_{PD(HL)}$	460 ns
#Channels	1, 2, 4
www.ti.com/product/tlv1701-q1	

Design Alternate Comparator

	TLV7021	TLV370x-Q1, TLV340x
V_S	1.6 V to 5.5 V	2.7 V to 16 V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{OUT}	Open-Drain, Rail-to-rail	Push-Pull, Rail-to-rail
V_{OS}	500 µV	250 µV
I_Q	5 µA	560 µA/Ch
$t_{PD(HL)}$	260 ns	36 µs
#Channels	1	1, 2, 4
	www.ti.com/product/tlv7021	www.ti.com/product/tlv3701-q1

Analog Engineer's Circuit

High-Side Current Sensing with Comparator Circuit

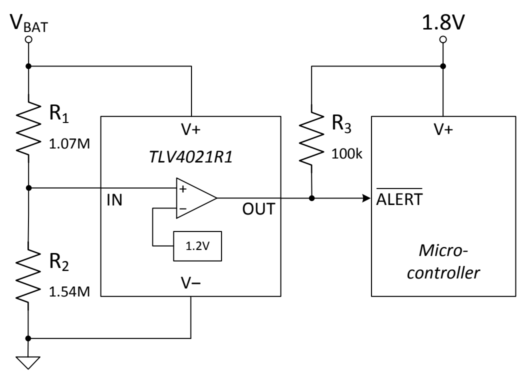
TEXAS INSTRUMENTS

Design Goals

Battery Voltage Levels (V_{BAT})		Comparator Output Status (OUT)	
Undervoltage (V_{LOW})	Start-Up Operating Voltage (V_{HIGH})	Low Battery	Normal Operation
< 2.000 V	> 2.034 V	V_{OL} < 0.4 V	V_{OH} = V_{PU} = 1.8 V

Design Description

This undervoltage, protection circuit uses one comparator with a precision, integrated reference to create an alert signal at the comparator output (OUT) if the battery voltage sags below 2.0 V. The undervoltage alert in this implementation is ACTIVE LOW. So when the battery voltage drops below 2.0 V, the comparator output goes low, providing as an alert signal to whatever device is monitoring the output. Hysteresis is integrated in the comparator such that the comparator output will return to a logic high state when the battery voltage rises above 2.034 V. This circuit utilizes an open-drain output comparator in order to level shift the output high logic level for controlling a digital logic input pin. For applications needing to drive the gate of a MOSFET switch, a comparator with a push-pull output is preferred.



Design Notes

1. Select a comparator with a precision, integrated reference.
2. Select a comparator with an open-drain output stage for level-shifting.
3. Select values for the resistor divider so the critical undervoltage level occurs when the input to the comparator (IN) reaches the comparator's negative-going input threshold voltage (V_{IT-}).

Design Steps

1. Calculate the resistor divider ratio needed so the input to the comparator crosses V_{IT-} when V_{BAT} sags to the target undervoltage level (V_{LOW}) of 2.0 V. V_{IT-} from the TLV4021R1 data sheet is 1.18V.

$$V_{IT-} = \frac{R_2}{(R_1 + R_2)} \times V_{LOW}$$

$$\frac{R_2}{(R_1 + R_2)} = \frac{V_{IT-}}{V_{LOW}} = \frac{1.18 \text{ V}}{2.00 \text{ V}} = 0.59$$

2. Confirm that the value of V_{LOW}, the voltage level where the undervoltage alert signal is asserted, is 2.0 V.

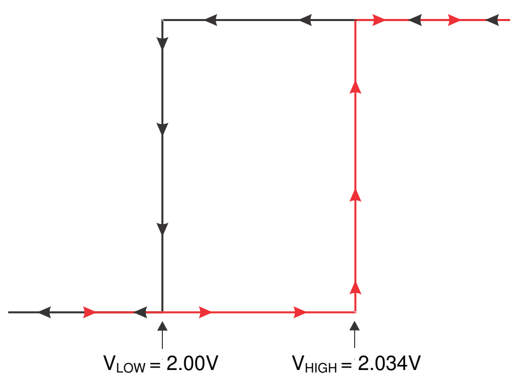
$$V_{LOW} = \frac{R_1 + R_2}{R_2} \times V_{IT-} = \frac{1}{0.59} \times 1.18 \text{ V} = 2.0 \text{ V}$$

3. Select values for R_1 and R_2 that yield the resistor divider ratio of 0.59 by using the following equation or using the online tool *Voltage Divider Calculator*.
   If using the following equation, choose a value for R_2 in the Mega-ohm range and calculate for R1. In this example, a value of 1.54 M was chosen for R_2.

$$R_1 = R_2\left(\frac{V_{LOW}}{V_{IT-}} - 1\right) = 1.54 \text{ M}\Omega\left(\frac{2 \text{ V}}{1.18 \text{ V}} - 1\right) = 1.07 \text{ M}\Omega$$

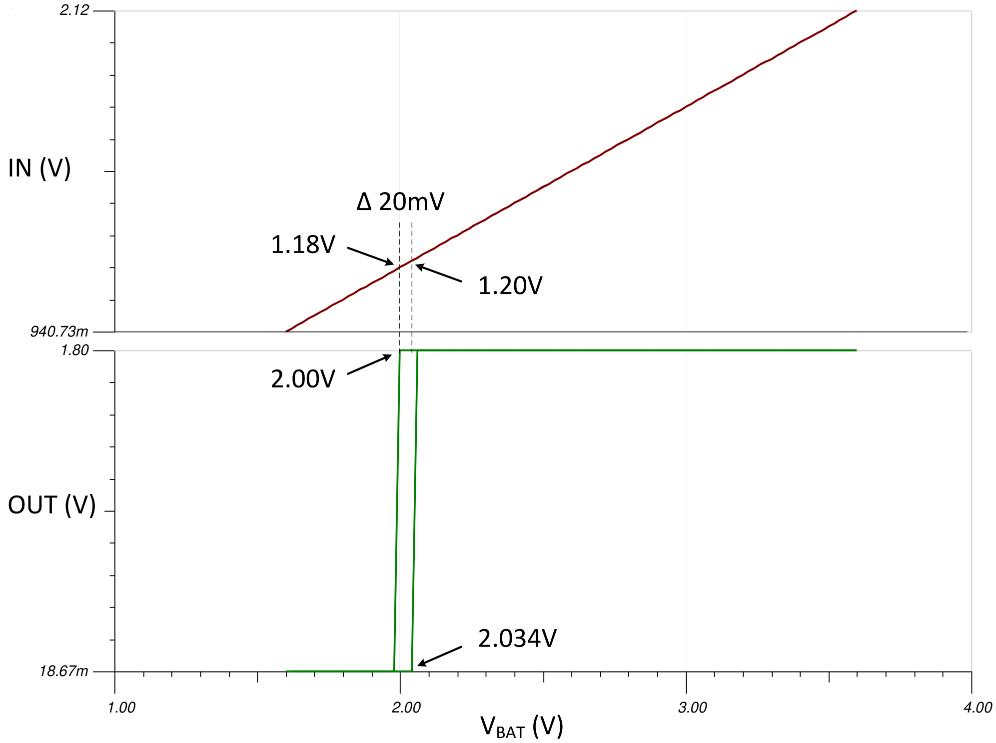
4. Verify that the current through the resistor divider is at least 100 times higher than the input bias current of the comparator. The resistors can have high values to minimize power consumption in the circuit without adding significant error to the resistor divider.
5. Calculate V_{HIGH}, the battery voltage where the undervoltage alert signal is de-asserted (returns to a logic high value). When the battery voltage reduces below the 2.0 V level or is ramping up at initial start-up, the comparator input needs to exceed (V_{IT+}), the positive-going input threshold voltage for the output to return to a logic high. V_{IT+} from the TLV4021R1 data sheet is 1.20 V.

$$V_{HIGH} = \frac{R_1 + R_2}{R_2} \times V_{IT+} = \frac{1.07 \text{ M}\Omega + 1.54 \text{ M}\Omega}{1.54 \text{ M}\Omega} \times 1.20\text{V} = 2.034 \text{ V}$$

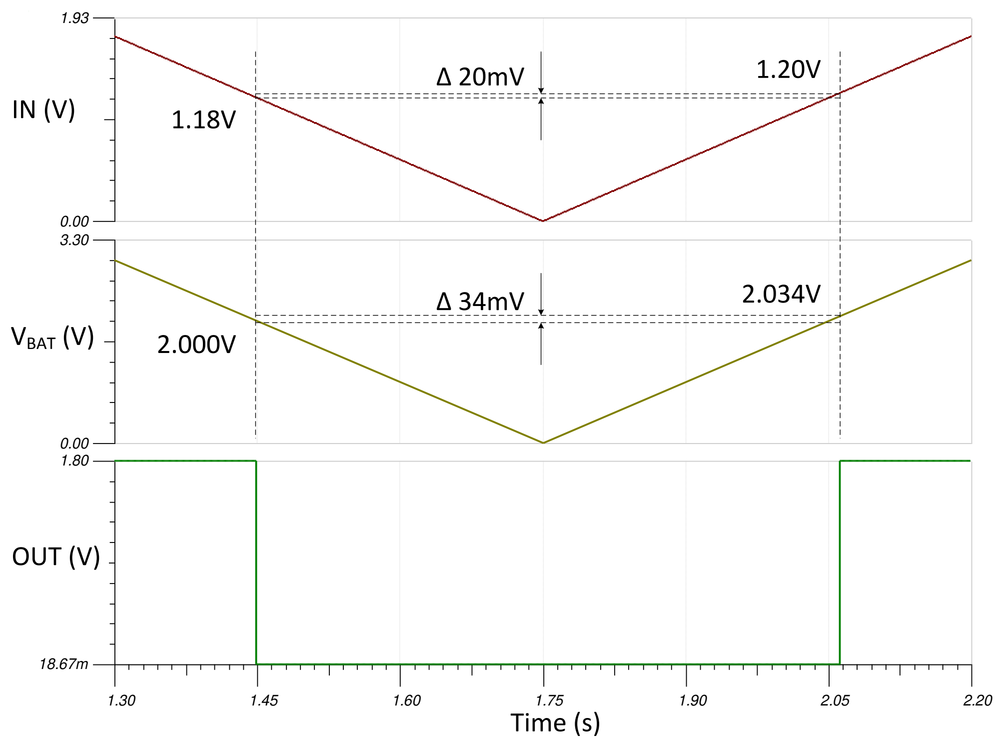


Design Simulations

DC Simulation Results



Transient Simulation Results



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File – SNOAA18
3. TI Precision Labs

Design Featured Comparator

TLV4021R1	
V_S	1.6 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{OUT}	Open Drain
Integrated Reference	1.2 V ±1% over temperature
Hysteresis	20 mV
I_Q	2.5 µA
$t_{PD(HL)}$	450 ns
TLV4021R1	

Design Alternate Comparator

	TLV4041R1	TLV3011
V_S	1.6 V to 5.5 V	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{OUT}	Push-Pull	Open Drain
Integrated Reference	1.2 V ±1% over temperature	1.242 ±1% room temperature
Hysteresis	20 mV	NA
I_Q	2.5 µA	2.8 µA
$t_{PD(HL)}$	450 ns	6 µs
	TLV4041R1	TLV3011

ORing MOSFET Controller with Comparator Circuit

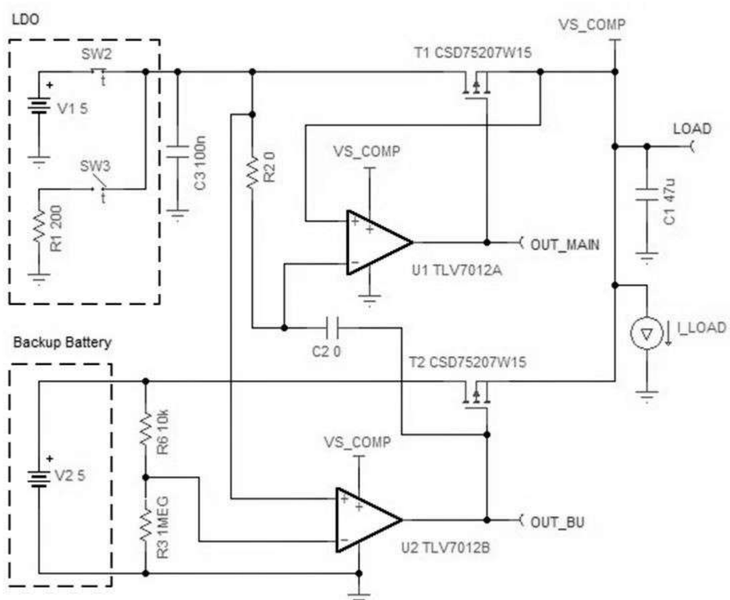
TEXAS INSTRUMENTS

Design Goals

LDO Output			Supply Voltages		Resistors		
R_1	C_1	C_3	V_1	V_2	R_2	R_3	R_6
200 Ω	47 µF	100 nF	5 V	5 V	1 kΩ	1 MΩ	10 kΩ

Design Description

Comparators can be used in an ORing configuration to choose between different sources. With a relatively simple circuit and smart switches, the comparator can be used to always maintain a supply voltage to the load. For low voltage applications, comparators have a better edge over diodes because there is no voltage drop. This circuit is designed for a system connected to a wall outlet with an incorporated backup battery. If the main power is ever cut, then the back up battery will supply power to the load to ensure the device is always on. The switch network on the left side of the circuit is used to model the LDO output.

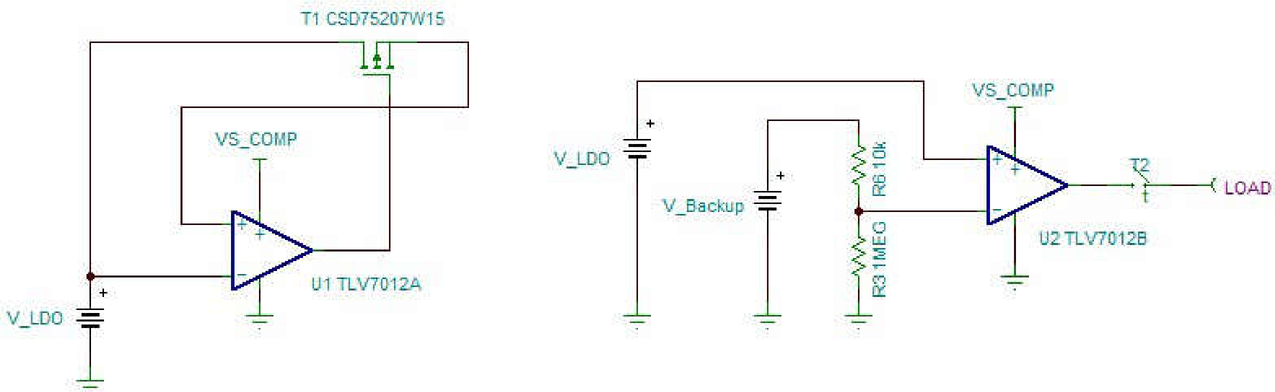


Design Notes

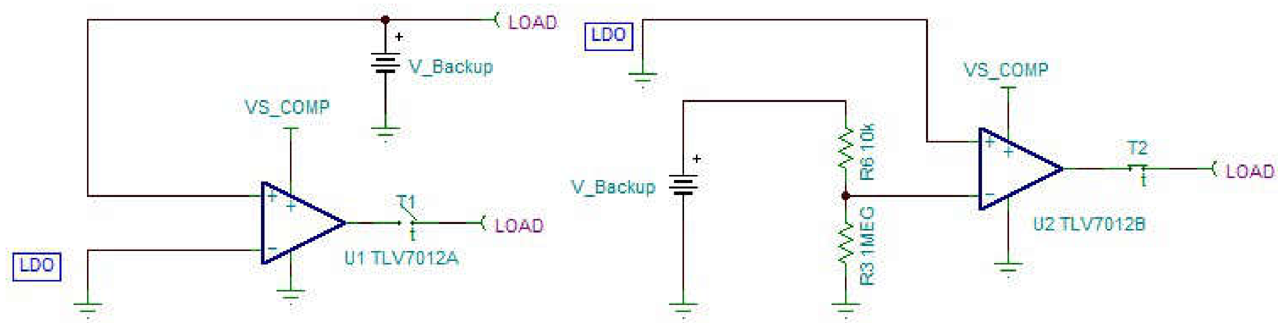
1. Use a push-pull comparator that has rail-to-rail input range.
2. Use a dual PMOS with common source configuration such as CSD75207W15.
3. Ensure the V_{th} of the PMOS is lower than the voltage at the output of the comparator.
4. Follow the data sheet recommendations for power filtering and stability at the output of the LDO for C_1 and C_3.
5. Use the LDO data sheet to determine the R1 value. It may be specified as the resistor used to connect the output to GND in the case of an undervoltage event.

Design Steps

1. The box highlighting R1, V1, and SW3 are used to model the LDO output behavior. R1 signifies the impedance of the LDO which can be found in the data sheet. V1 is the LDO output voltage, so set V1 accordingly. SW3 is used for modeling the case when the LDO suddenly loses power and the output will be pulled to ground through R1. It is also used for modeling the case when the LDO is powered back up and supplying a voltage. C3 is added to the circuit because it is the typically recommended capacitor value to help with loop stability that should be right next to the output. Set this value according to the LDO data sheet recommendations. C1 is added at the load because the larger capacitor value does not need to be right at the LDO output node. Set this value according to the LDO data sheet recommendations.
2. During the initialization of the circuit, as the comparator powers on, the current will flow through the body diodes of T1 to supply power to the load. Current will stop flowing through the diode when the drop across the diode is less than approximately 0.7 V. Then, the comparator will output low and turn on the PMOS switch.
3. Under normal or typical conditions, the LDO is used as the main power supply. In the following image, there is a simplified circuit model to explain the function of U1 and U2. The (-) node sees the LDO voltage, and the (+) node sees the source node of T1. The comparator output will stay low because the (+) node is slightly smaller than the drain node from the $R_{DS(on)}$ drop of T1. Since the comparator pulls the gate low, T1 will act like a closed switch, allowing the LDO to power the load.
   During this time, U2 will be controlling T2, making it act like an open switch. The box highlighting V2 models the back up battery. V2 is the back up battery voltage, so set V2 accordingly. R3 and R6 form a voltage divider, so that the (-) node sees a 0.99 × V2. When the LDO is on and providing power, if the back up battery and the LDO are at the same potential, T2 must act like an open switch to prevent both sources from being loaded. The (-) node sees a divided down voltage of V2 and the (+) node sees the LDO voltage. To make sure that the comparator output is high so that T2 is turned off, then the (-) node < (+) node.



4. When the LDO loses power, the back up battery is connected to the load so that there is always a constant source of power. In the following image, there is a simplified circuit model to explain the function of U1 and U2. Now that the LDO output is pulled to low, the (+) node of U2 sees ground and the (-) node of U2 sees a divided down version of the back up battery. This will force the comparator output low and close the switch so that the back up battery can source to the load. During this time, U1 will be disconnected from the load. In the following image, there is a simplified circuit model to explain the function of U1. The (-) node sees ground since the LDO output is pulled low, and the (+) node sees the back up battery. The comparator output will transition high and turn off T1 so it acts like an open switch.



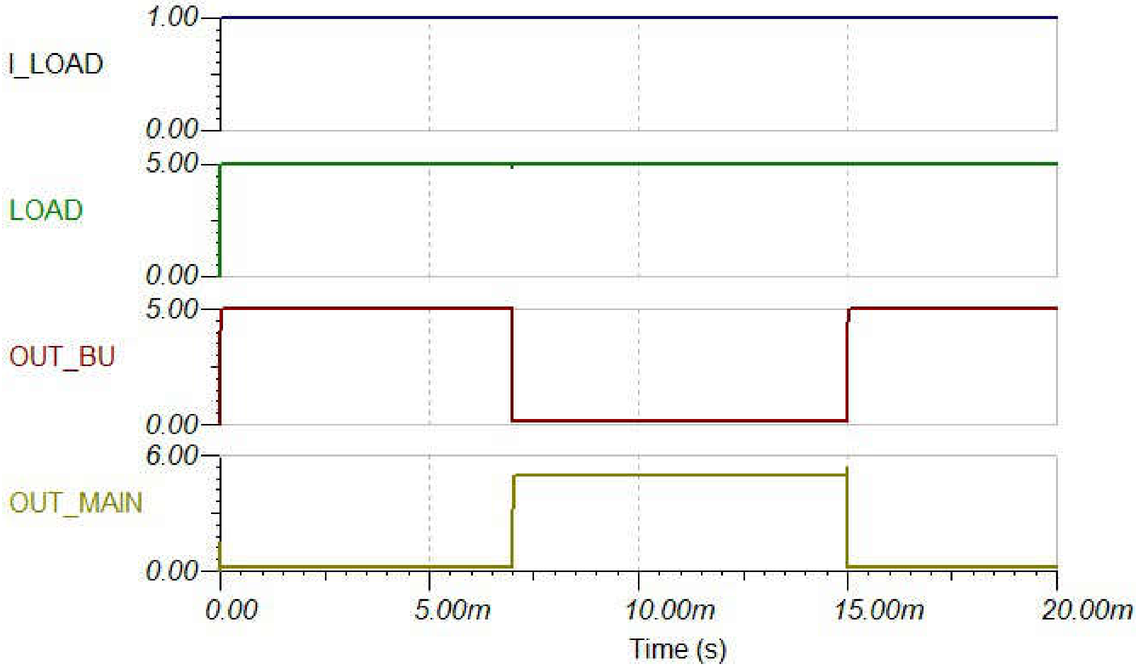
5. Set the voltage divider created by R_3 and R_6 for a ratio of 1%. Set the ratio for 1% so that U2 can quickly switch once the LDO loses power. During normal operation, OUT_BU will stay high because the inverting input will be 1% less than inverting input. When the main supply loses power, OUT_BU will go high because the non-inverting input is connected to the output of the LDO.
   The R_{total} (R_3 + R_6) should be such that the current through the divider is at least 100 times higher than the input bias current (I_{bias}). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

$$\frac{R_3}{R_3 + R_6} = 1\,\%$$

6. Now looking at the details, R2 and C2 functionality is described. R2 is used here to isolate the LDO output from the (-) node of U1. When the LDO loses power, SW3 closes and pulls the LDO output to GND. If R2 is shorted, then T1 always stays on because there is contention between both sides of C2. As the LDO output tries to sink to ground, the output of U2 is also transitioning low. Because there is some delay to the LDO output, the (-) node of U1 will struggle and the node will oscillate around the load voltage. Setting R2 to 1 kΩ is sufficient enough to isolate the node. If R2 is too small, there will be wasted power. If R2 is too large, the (-) node of U1 transitions too slowly so that it is not able to switch T1 on. U1 never turns on T1 and the power to the load is supplied through the body diode instead. When the LDO output transitions (either losing power or regaining power), C2 is used to yank the (-) node of U1 so that it is able to transition quickly and turn U1 on or off. Without C2, the delay from the LDO transitioning causes U1 to never switch. Set C2 to the same value as C3.

Design Simulations

Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File: SBOR017.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range see TI Precision Labs - Op amps.

Design Featured Comparator

TLV7011, TLV7012	
Output Type	PP
V_{cc}	1.6 V to 6.5 V
V_{inCM}	Rail-to-rail
V_{os}	±.5 mV
V_{HYS}	4.2 mV
I_q	5 µA/Ch
t_{pd}	260 ns
#Channels	1 and 2
TLV7011 Product Page, TLV7012 Product Page	

Design Alternate Comparator

TLV1805	
Output Type	PP
V_{cc}	3.3 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{HYS}	14 mV
V_{os}	±500 µV
I_q	135 µA
t_{pd}	250 ns
#Channels	1
TLV1805 Product Page	

TLV7031, TLV7032	
Output Type	PP
V_{cc}	1.6 V to 6.5 V
V_{inCM}	Rail-to-rail
V_{HYS}	7 mv, 10 mV
V_{os}	±1 mV
I_q	335 nA, 315 nA
t_{pd}	3 µs
#Channels	1 and 2
TLV7031 Product Page, TLV7032 Product Page	

Analog Engineer's Circuit

Window Comparator with Integrated Reference Circuit

TEXAS INSTRUMENTS

Design Goals

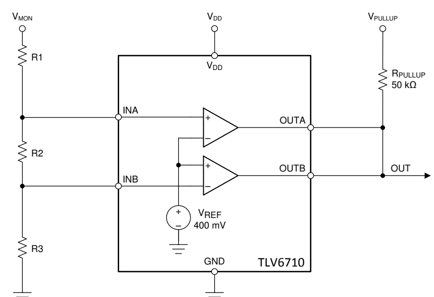
Input		Output		Supply	
$V_{MON\ Min}$	$V_{MON\ Max}$	$V_{OUT\ Min}$	$V_{OUT\ Max}$	V_{DD}	V_{REF}
0 V	6 V	0 V	3.3 V	3.3 V	400 mV

Lower Threshold (V_L)	Upper Threshold (V_H)	Divider Load Current (I_{MAX}) at V_H
3.2 V	4.1 V	10 µA

Design Description

This circuit utilizes the TLV6710, which contains two comparators and a precision internal reference of 400mV. The monitored voltage (V_{MON}) is divided down by R_1, R_2, and R_3. The voltage across R_2 and R_3 is compared to the 400 mV internal reference voltage (V_{REF}). If the input signal (V_{MON}) is within the window, the output is high. If the signal level is outside of the window, the output is low.

The TLV6710 will be utilized for this example, which conveniently contains two comparators and a common precision internal reference trimmed to a 400 mV threshold. Two discrete comparators and an external reference may also be used.



Design Notes

1. Make sure the comparator input voltage range is not violated at the highest expected V_{MON} voltage.
2. If the outputs are to be combined together (ORed), open collector or open drain output devices *must* be used.
3. It is also recommended to repeat the following calculations using the minimum and maximum resistor tolerance values and comparator positive and negative offset voltages.
4. The TLV6710 has built-in asymmetrical hysteresis, resulting in the rising edge V_L and falling edge V_H being slightly shifted. Comparators without hysteresis will meet the calculated thresholds.

Design Steps

The resistor divider will be calculated in separate V_H and V_L segments to create 400 mV at the appropriate comparator input at the desired threshold voltage.

1. The total divider resistance R_{TOTAL} is calculated from the upper threshold voltage and divider current:

$$R_{TOTAL} = R_1 + R_2 + R_3 = \frac{V_H}{I_{MAX}} = \frac{4.1V}{10\mu A} = 410k\Omega$$

2. The upper threshold voltage is set by the *bottom* divider resistor R_3 going into the INB pin. From the reference voltage and the divider current, the value of R_3 is calculated from:

$$R_3 = \frac{V_{REF}}{I_{MAX}} = \frac{400mV}{10\mu A} = 40k\Omega$$

3. The *middle* resistor R_2 is found by looking at R_2 and R_1 as one resistor, and calculating the value for that total resistance for V_{REF} at V_L, then subtracting out the known R_3:

$$R_2 = \left(\left(\frac{R_{TOTAL}}{V_L} \times V_{REF}\right) - R_3\right) = \left(\left(\frac{410k\Omega}{3.2V} \times 400mV\right) - 40k\Omega\right) = 11.25k\Omega$$

4. R_1 is found by taking the total resistance and subtracting the sum of R_2 and R_3:

$$R_1 = R_{TOTAL} - (R_2 + R_3) = 410k\Omega - (11.25k\Omega + 40k\Omega) = 358.75k\Omega$$

Because these are calculated ideal resistor values, the next closest 0.1% standard resistor values will be used. The following table summarizes the changes due to the resistor value changes and the resulting trip point voltage change.

Nearest 0.1% Resistor Values

Resistor	Calculated Ideal Value	Nearest Standard 0.1% (E192) Value
R_1	358.750 kΩ	361 kΩ
R_2	11.25 kΩ	11.3 kΩ
R_3	40 kΩ	40.2 kΩ

Because the values of the divider string resistors were changed, the resulting new threshold voltages must be calculated. The thresholds are found by multiplying the divider ratio by the reference voltage:

$$V_H = \left(\frac{R1 + R2 + R3}{R3}\right) \times V_{REF} = \left(\frac{361k\Omega + 11.3k\Omega + 40.2k\Omega}{40.2k\Omega}\right) \times 0.4V = 10.26119 \times 0.4V = 4.1045 \quad V$$

$$V_L = \left(\frac{R1 + R2 + R3}{R2 + R3}\right) \times V_{REF} = \left(\frac{361k\Omega + 11.3k\Omega + 40.2k\Omega}{11.3k\Omega + 40.2k\Omega}\right) \times 0.4V = 8.0097 \times 0.4V = 3.2039 \quad V$$

Ideal and Standard Resistor Thresholds

Threshold	Using Ideal Resistors	Using Standard Resistors	Percent Change
V_H	4.1 V	4.1045 V	+0.109%
V_L	3.2 V	3.2039 V	+0.121%

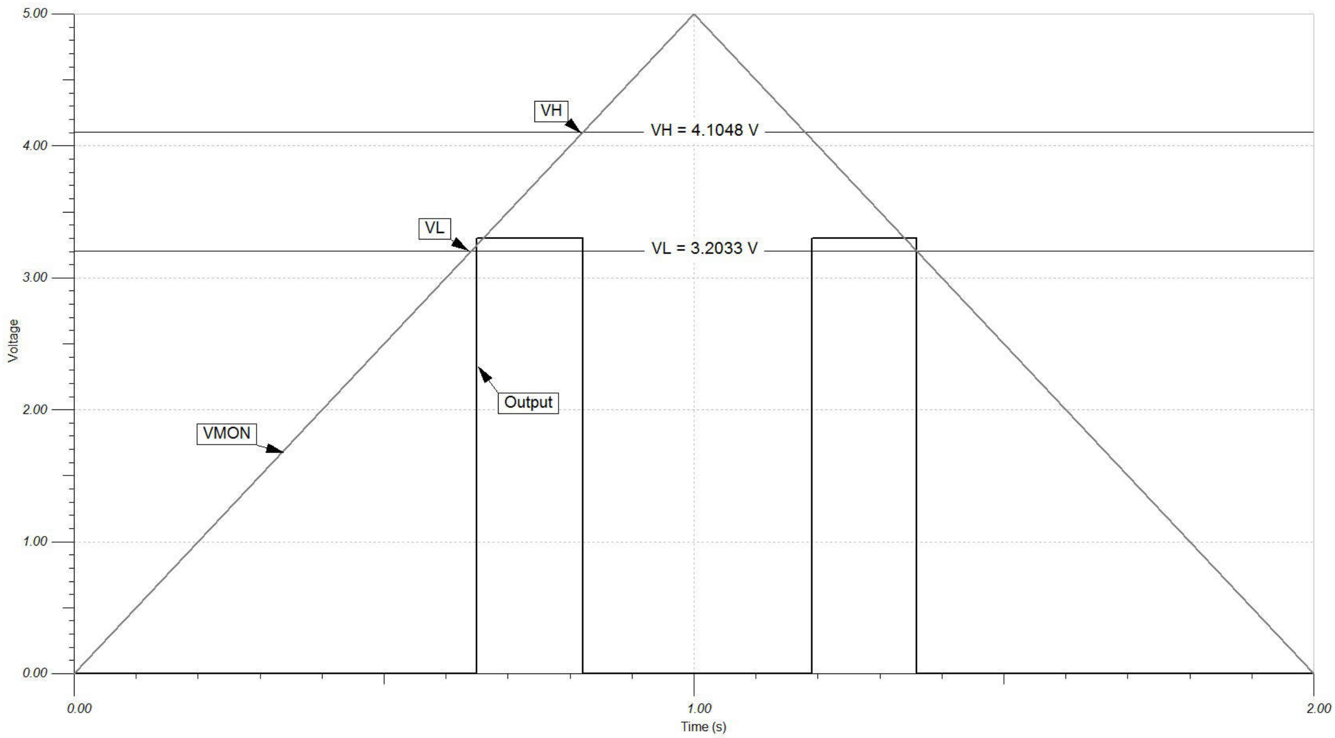
To ensure that the maximum 6V V_{MON} voltage does not violate the TLV6710 1.7 V maximum input voltage rating, the V_{MON_MAX} and the V_L division ratio found in step 4 above are used to calculate the maximum voltage at the TLV6710 input:

$$V_{INPUT\_MAX} = \frac{V_{MON\_MAX}}{V_{L\_RATIO}} = \frac{6 \quad V}{8.0097} = 749.1 \quad mV$$

The value 749 mV is less than 1.7 V, so the input voltage is well below the input maximum. If using discrete comparators, make sure the voltage is within the specified input common mode range (V_{ICR}) of the device used.

Design Simulations

Transient Simulation Results



Note: The Rising edge V_L and falling edge V_H thresholds are slightly shifted due to the built-in asymmetrical hysteresis of the TLV6710. Comparators without hysteresis will meet the calculated thresholds.

Design References

For more information on many comparator topics including input voltage range, output types and propagation delay, please visit TI Precision Labs - Comparator Applications.

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See TINA-TI™ TLV6710 Reference Design circuit simulation file, Literature Number SNVMB09.

Design Featured Comparator

TLV6710	
V_{ss}	2 V to 36 V
V_{inCM}	0 V to 1.7 V
V_{out}	0 V to 25 V
Vref	400 mV ±0.25%
I_q	11 µA
I_b	1 nA
Prop Delay	10 µs
#Channels	2
TLV6710	

Design Alternate Comparator

TLV6700	
V_{ss}	1.8 V to 18 V
V_{inCM}	0 V to 6.5 V
V_{out}	0 V to 18 V
Vref	400 mV ±0.5%
I_q	5.5 µA
I_b	1 nA
Prop Delay	29 µs
#Channels	2
TLV6700	

Design Alternate Comparator

TLV1702	
V_{ss}	2.7 V to 36 V
V_{inCM}	Rail to Rail
V_{out}	Open Drain to 36 V
V_{os}	±3.5 mV
I_q	75 µA
I_b	15 nA
Prop Delay	0.4 µs
#Channels	2
TLV1702	

Analog Engineer's Circuit

Signal and clock recovery comparator circuit

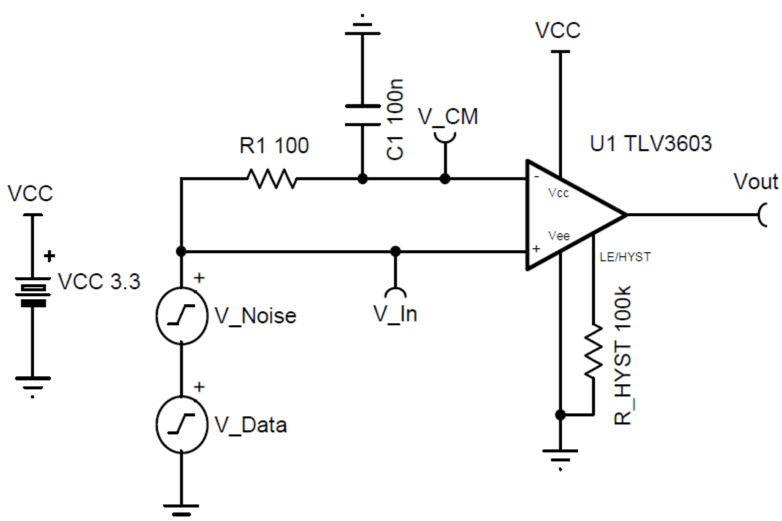
Amplifiers

Design Goals

Supply		Attenuated Input Signal		
V_{cc}	V_{ee}	V_i	V_{cm}	f
3.3V	0V	$50mV_{p\text{-}p}$	1.65V	200MHz

Design Description

The signal recovery circuit is used in digital systems to retrieve distorted clock or data waveforms. These clock and data signals can be attenuated and distorted on long traces due to stray capacitance, stray inductance, or reflections on transmission lines. The comparator is used to sense the attenuated and distorted input signal and convert it to a full scale digital output signal. A dynamic reference voltage will be connected to the inverting terminal of the comparator which is extracting the common-mode voltage from the input signal.



Design Notes

1. Select a comparator with low input offset voltage and fast propagation delay.
2. Use a comparator with a toggle frequency larger than the input signal frequency to properly process the incoming digital signal. A margin of 30% is sufficient to allow for process and temperature variations if a minimum value is not warranted in the data sheet.
3. If level translation is also required, use a comparator with separate input and output supplies.
4. If a differential output is required, use a comparator with a compatible output stage such as the LVDS compatible output on the TLV3605.
5. The signal should be symmetric around the waveform midpoint for the dynamic reference to accurately determine the common mode voltage of the input signal. For signals with duty cycles outside of 30–70%, the dynamic reference must be replaced with an external reference source.

Design Steps

1. Compare the maximum toggle frequency of the comparator to ensure it can process the input signal. This parameter is usually specified in the data sheet of the comparator. If this value is not, see the following section for guidelines on approximation. The toggle frequency of this comparator, TLV3603, is 325MHz.
2. Set the non-inverting input of the comparator to the input data signal.
3. Create a dynamic reference from a low-pass network using a capacitor, C_1, and resistor, R_1. Connect the input of the network to the non-inverting input and the output to the inverting input.
4. Size the values of the dynamic reference so that its cutoff frequency is significantly below the operating frequency of the input signal while ensuring the time constant of the network is small enough for maximum responsivity. Let C_1 = 0.1µF and designing for a time constant τ of 10µs, calculate the needed resistor value:

   $$\tau = R_1 C_1$$

   $$10\mu\text{s} = \text{R}_1(100\text{nF}) \Rightarrow \text{R}_1 = 100\Omega$$

   Using the solved-for resistor value, ensure the cutoff frequency is still significantly below the input signal frequency.

   $$f_{\text{cutoff}} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(100\Omega)(100nF)} = 15.915\text{kHz} \ll 1\text{GHz}$$

   The time constant τ has an inverse relationship with f_{cutoff}. The quicker τ is, the more reactive the dynamic reference output node is to the input while pushing the cutoff frequency higher. However, if the cutoff frequency of the dynamic reference approaches the operating frequency of the input signal, the output of the network is unable to properly filter out the high-frequency component of the input signal, thereby failing to generate a stable DC reference voltage to compare the input signal against.

   A ramification to consider when balancing the accurate filtering of the signal versus τ is the start-up time. As the system starts in an uncharged state, once the system is active, there is a time period (around 5τ) until the voltage level at the inverting input is at an accurate level.
5. If the input signal is noisy in addition to being attenuated, the TLV3603 is able to handle the noise though implementation of its adjustable hysteresis feature. This pin can be driven with a voltage source or be attached to a resistor to VEE and can cause the comparator to have a hysteresis up to 65mV, as well as latching the output depending on the voltage seen at the pin. See the *TLV3601, TLV3603 325MHz High-Speed Comparator with 2.5ns Propagation Delay* data sheet for more information. For this circuit, a hysteresis of 10mV is implemented to counter the noisy input signals by connecting a 600-kΩ resistor to VEE.

Is this comparator fast enough for this input signal?

Toggle frequency, f_{Toggle}, is the metric that measures how fast a comparator can handle input signal speeds. This metric is measured as the input-signal frequency at which the output swing is a certain percentage compared to itself at low-input signal frequencies. The percentage varies by manufacturers and even by products, so it is important to check the data sheet of the part to see how this parameter is being met.

When f_{Toggle} is not included in data sheet of a part, there may be some concern as to whether that part is suitable for use in a system. In that case, here is a general approximation to gauge f_{Toggle} of the part:

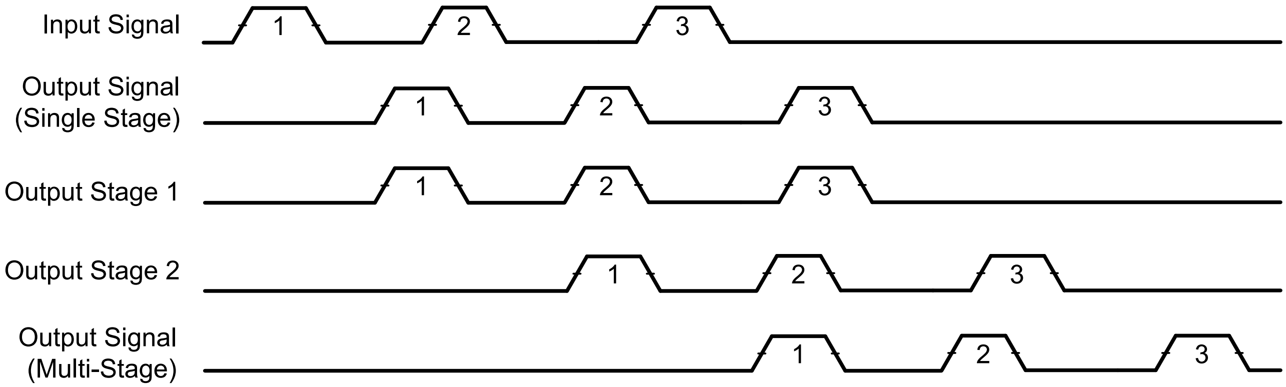
$$\text{f}_{Toggle} = (0.5\text{t}_{rise} + 0.5\text{t}_{fall} + \text{t}_{pd\_hl} + \text{t}_{pd\_lh})^{-1}$$

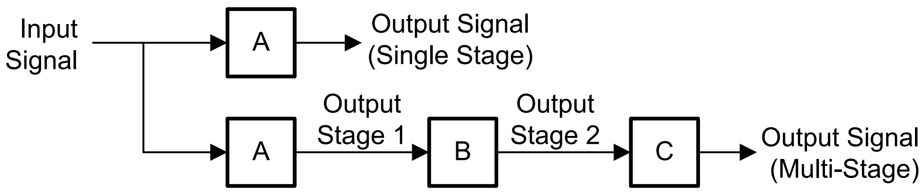
It is important to note that this approximation is conservative and may not completely match a part's f_{Toggle} inside a data sheet if specified, especially when evaluating higher speed comparators as these tend to be multi-stage comparators. Using the values included in TLV3603 data sheet:

$$\text{f}_{Toggle} = (0.375\text{ ns} + 0.375\text{ ns} + 2.5\text{ ns} + 2.5\text{ ns})^{-1} = 173.9\text{ MHz}$$

While the data sheet states that the toggle frequency is 325MHz, this approximation indicates that this product only handles 173.9MHz and lower signals. Why is this the case? This can be due to multiple factors, but an important consideration must be made when evaluating single (or near-single) stage products versus multi-stage products.

When using a near-single stage comparator, the input signal read by the comparator needs to pass through a low number of stages until its output transitions. f_{Toggle} is dependent on the stage with the longest propagation delay in the chain (whether that chain be one or multiple stages), rather than passing all the way through to the output before the next bit is fed in.



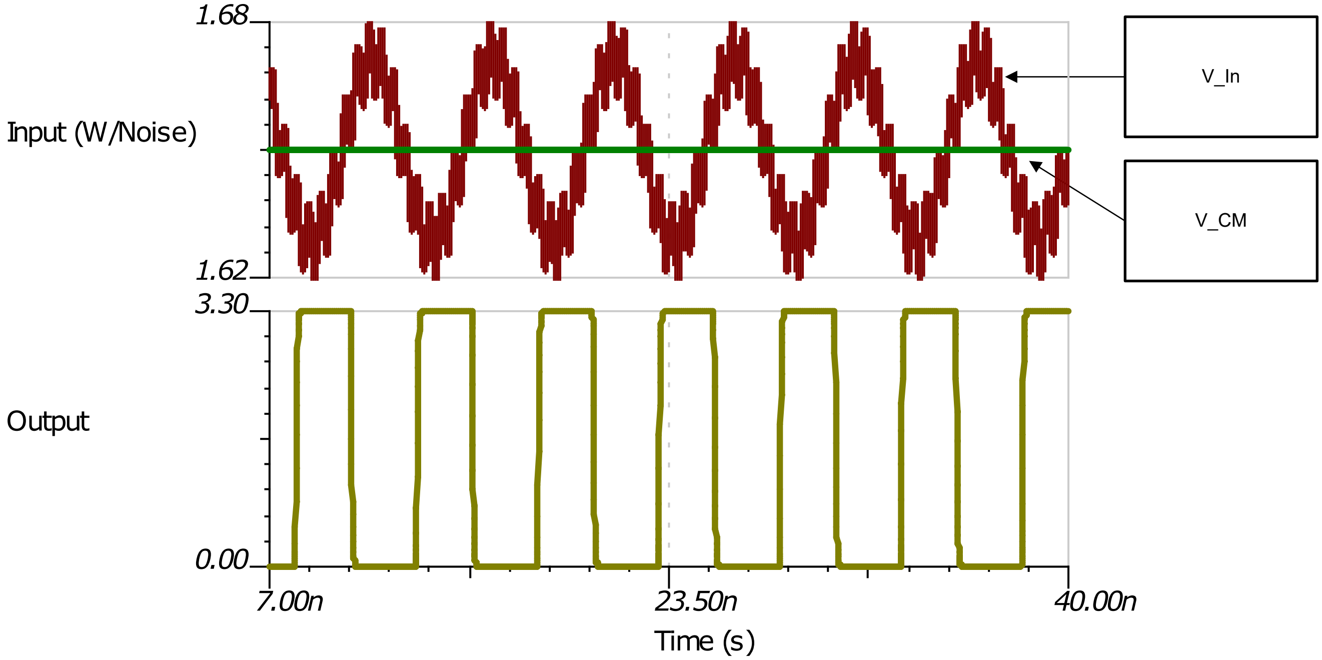


In the previous diagram, an input signal consisting of bits 1, 2, and 3 are both fed into a single stage comparator and a multi-stage comparator. The single stage comparator only has stage A, while the multi-stage comparator consists of stages A, B, and C. When bit 1 enters both comparators, it takes a period of time to get through stage A. Once it gets past stage A, on the single stage comparator, it reaches the output while on the multi-stage comparator, it enters stage B. At that point, bit 2 can begin to enter stage A. After another period of time, bit 2 reflects on the single stage output while also entering Stage B of the multi-stage comparator. Bit 1, at this point, begins to enter stage C.

This illustrates that while the propagation time may differ between a multi-stage and single stage comparator (it may be smaller, larger, or nearly the same depending on the stages), the rate at which each comparator handles these signals is dependent on when the bit clears the stage with the greatest propagation delay so that the next bit can come through the pipeline.

Design Simulations

Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit spice simulation file, SNOM712.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, TI Precision Labs.

Design Featured Comparator

TLV3603-Q1	
V_{ss}	2.4V to 5.5V
V_{inCM}	Rail-to-rail
t_{pd}	2.5ns
V_{os}	0.5mV
V_{HYS}	0–60mV (Adjustable)
I_q	6mA
Output Type	Push-pull
#Channels	1
www.ti.com/product/tlv3603-Q1	

Design Alternate Comparator

	TLV3501	TLV3601
V_{ss}	2.7 to 5.5V	2.4 to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
t_{pd}	4.5ns	2.5ns
V_{os}	1mV	0.5mV
V_{HYS}	6mV	3mV
I_q	3.2mA	6mA
Output Type	Push-pull	Push-pull
#Channels	1	1
	www.ti.com/product/tlv3501	www.ti.com/product/tlv3601

Analog Engineer's Circuit

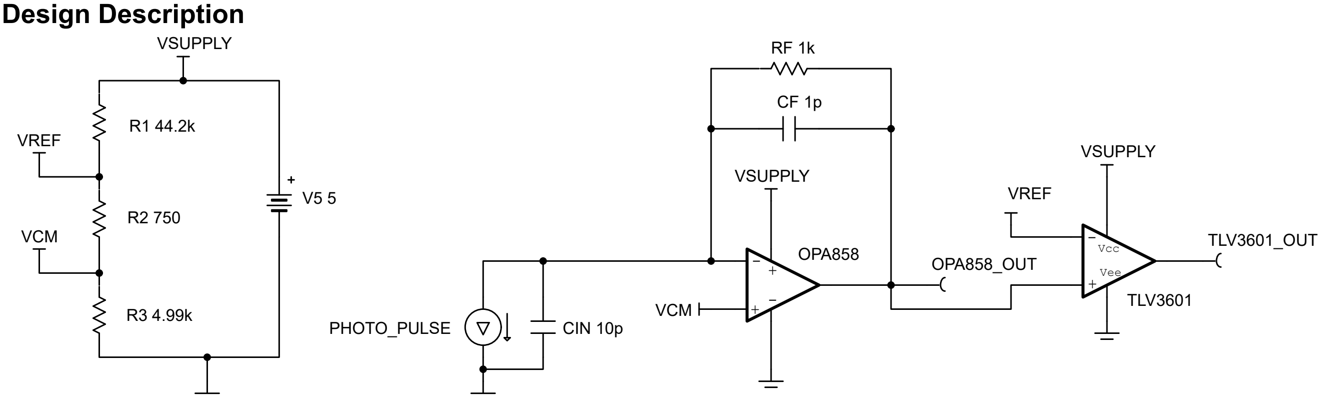
LiDAR Receiver Comparator Circuit

Amplifiers

Design Goals

System Supply	Photodiode Input Current Pulse Width	Transimpedance Amplifier		Output Type	Maximum Propagation Delay
5 V	3 ns	High Bandwidth	100-mV output swing	Single-ended	4 ns

Design Description



LiDAR Receiver Circuit

This circuit must be able to detect a 3-ns pulse received on a photodiode from a light pulse. To do this, a transimpedance amplifier and a high-speed comparator are required. To meet the propagation delay requirement, this design uses the OPA858 5.5-GHz gain bandwidth product, decompensated transimpedance amplifier with FET inputs and the TLV3601 2.5-ns high-speed rail-to-rail comparator with push-pull outputs.

Design Notes

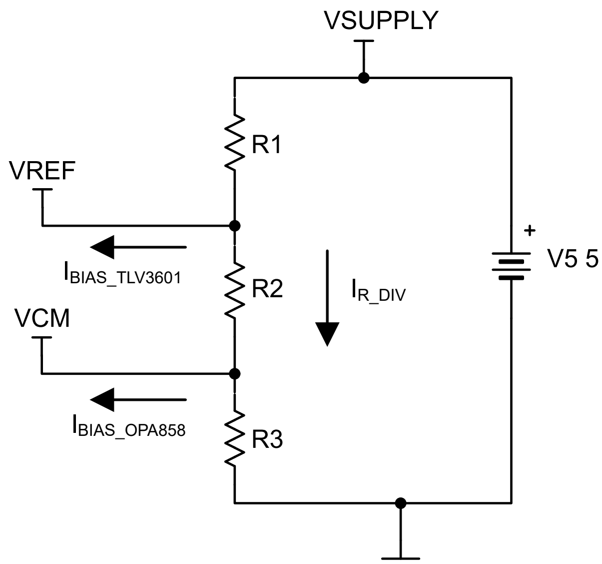
1. Select a high-speed comparator that has narrow pulse width detection capability better than 3 ns
2. Derive the reference for the transimpedance amplifier and comparator from the same voltage source
3. Verify stability of the transimpedance amplifier configuration with selected photodiode

Design Steps

Step 1: Configuring the TIA Common-Mode Voltage and the Comparator Reference Voltage

One of the goals of this design is to operate from a single, 5-V supply. This design uses a three-resistor divider network to establish the common-mode output voltage and the comparator reference voltage.

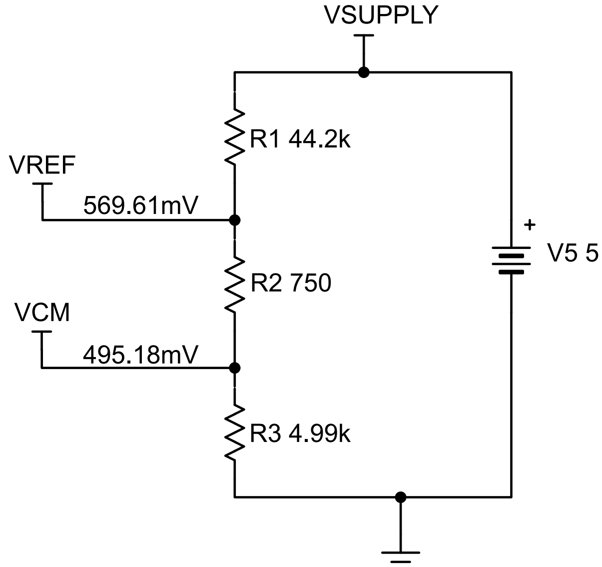
The important thing to note for this resistive divider network is to consider the input bias currents of both the OPA858 and TLV3601 devices. Since the OPA858 has an ultra-low bias current of 10 pA, the largest source of error comes from the TLV3601. The input bias current of the TLV3601 is typically 1 µA which means that the current through the divider network should be at least 100 times larger to maintain the desired reference voltages. With a 5-V supply and a current of 100 µA, the maximum total resistance for this network is 50 kΩ.



Effect of Input Bias Currents on Resistor Divider Network

For this design, the common-mode voltage of the OPA858 is set to 500 mV, a bias voltage within the recommended common-mode range for the OPA858. To do this, divide 500 mV by the 100 µA desired divider current. This gives a value for R3 of 5 kΩ but 4.99 kΩ was used for this design.

To comply with the design requirements, the OPA858 output will swing 100 mV. With the 500-mV output common-mode established, the comparator threshold voltage must be in the range of 500 mV to 600 mV. The TLV3601 threshold is 575 mV for this design. To provide an additional 75 mV from the 500-mV reference, R2 must be 750 Ω with the total branch current still being 100 µA.



Complete Resistor Divider Network With DC Nodal Voltages

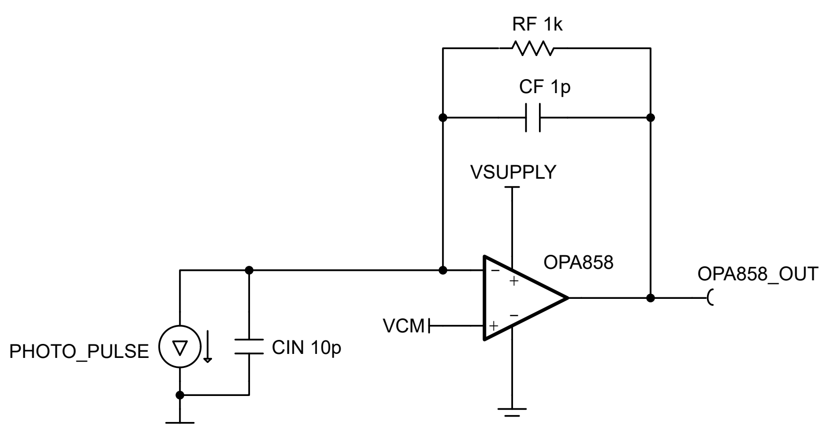
To adhere to the maximum resistance and minimum current requirement, R1 was selected to be 44.2 kΩ. This gives a total resistance of 49.94 kΩ.

Step 2: Configuring the OPA858 Transimpedance Amplifier

With a 100-µA pulse of current through the feedback branch of the OPA858, a 1-kΩ feedback resistance is required to produce a 100-mV swing on the output.

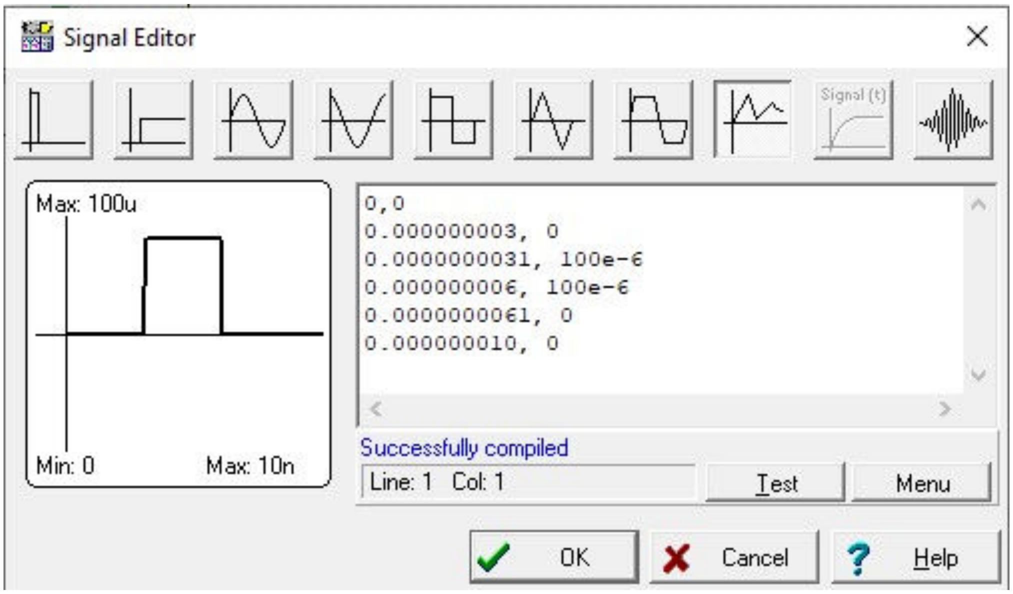
For this application, a 3-ns light pulse is received as a 100-µA current pulse. Assuming at most one, 3-ns pulse in a 10-ns window, the total period of our input is 10 ns. A 10-ns period corresponds to a 100-MHz signal. To select the feedback capacitor, first consider the pole frequency of a feedback network with a capacitor and resistor in parallel. The rough pole frequency is expressed as follows:

$$f_P = \frac{1}{2\pi \times R_F \times C_F}$$



OPA858 and Photodiode Completed Front-End Circuit

With a 1-pF capacitor in the feedback loop and a 1-kΩ feedback resistor, the pole frequency is approximately 159 MHz. The input signal is within the bandwidth of the feedback impedance. Additional stability analysis is also required for the transimpedance amplifier circuit and the metrics used to check for stability were rate of closure (ROC) and phase margin. For further information on stability analysis see the *Op Amps: Stability - Phase Margin* and *Op Amps: Stability - Spice Simulation* TI Precision Labs training videos.

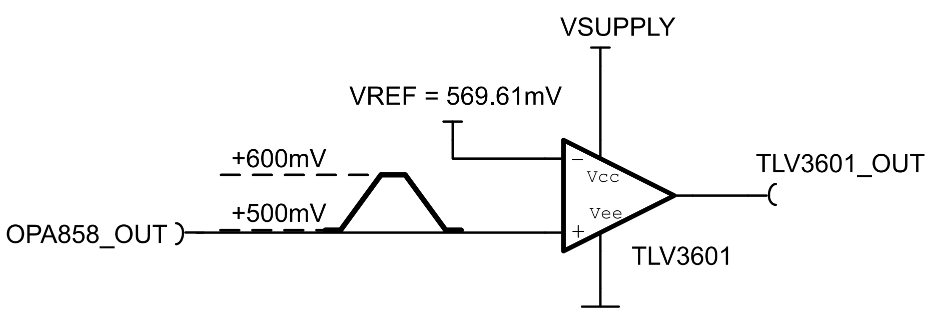


Input Signal Piecewise Configuration for 3-ns, 100-µA Pulse

To mimic the behavior of a photodiode receiving a 3-ns pulse of light, a piecewise current generator is configured to pulse 100 µA for 3 ns in a 10-ns period. The parallel input capacitance is set to 1 pF. For more information on a photodiode equivalent model see the *1 MHz, Single-Supply, Photodiode Amplifier Reference Design*.

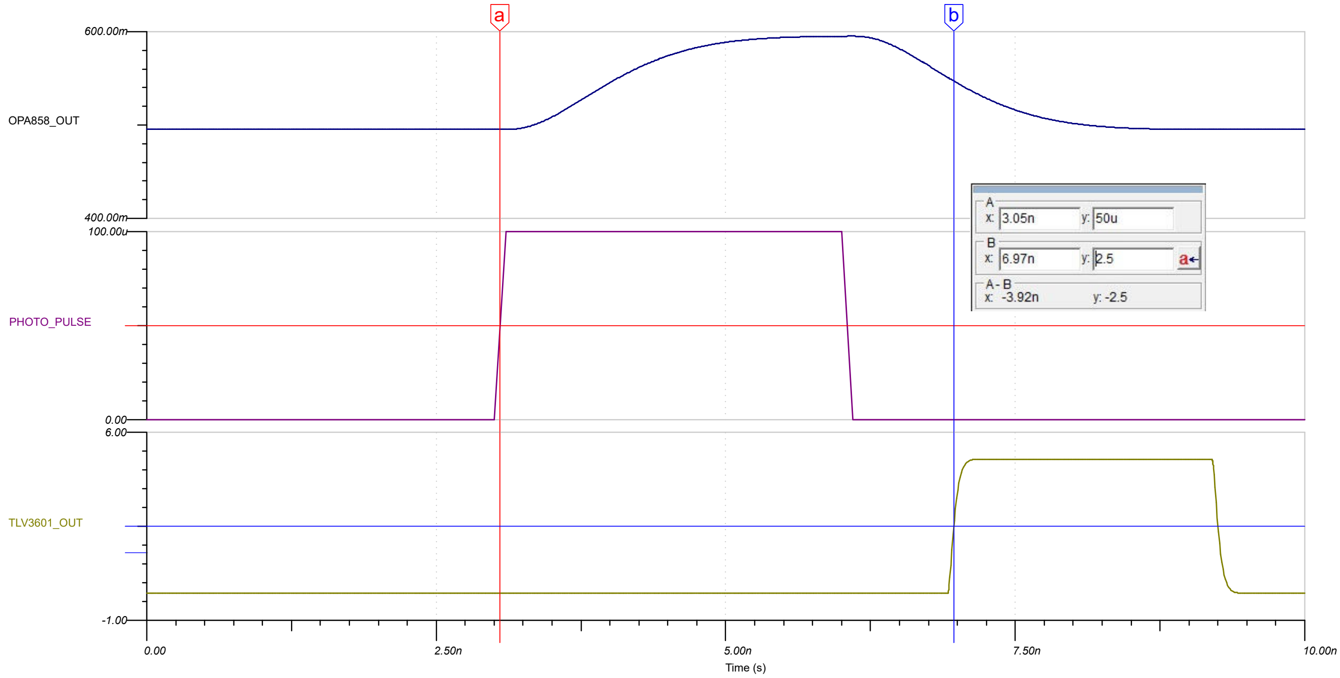
Step 3: Configuring the TLV3601 High-Speed Comparator With Push-Pull Outputs

This design uses the TLV3601 high-speed comparator in a non-inverting configuration. To configure the comparator, connect the voltage node above R2 to the inverting input and designate it VREF. Connect the same 5-V supply used for the OPA858 and connect the VEE pin to ground. The input common-mode range with a 5-V supply is –0.3 V to 5.3 V. With one of the inputs swinging from 500 mV to 600 mV and VREF being 569.6 mV, both inputs adhere to the input common-mode range of the TLV3601. If extra hysteresis is required to avoid output chatter due to noise or input signal conditions, then use the TLV3603. The TLV3603 has an extra hysteresis pin if hysteresis is required for an application.



TLV3601 Inputs and Connections

Simulation Results



Measured Propagation Delay from Input Pulse Measured at 3.92 ns

Design References

See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See the *LVDS GaN Driver Transmitter Circuit With High-Speed Comparator*.

See the *Non-inverting comparator with hysteresis circuit*.

Circuit SPICE simulation file: SNOM742.

For more information on many comparator topics including hysteresis, propagation delay, and input common-mode range, see *TI Precision Labs - Op amps*.

Design Featured Comparator

TLV3601	
V_s	2.4 V to 5.5 V
V_{inCM}	V_{EE} – 0.2 V to VCC + 0.2 V
V_{IO} (input offset voltage at 25°C) (maximum)	±0.5 mV
I_q	4.9 mA
T_{PD}	2.5 ns
Input Bias Current (Typical)	1 µA
Output type	Push-Pull
TLV3601	

Design Alternate Comparator

TLV3603	
V_s	2.4 V to 5.5 V
V_{inCM}	V_{EE} – 0.2 V to VCC + 0.2 V
V_{IO} (input offset voltage at 25°C) (maximum)	±0.5 mV
I_q	5.7 mA
T_{PD}	2.5 ns
Input Bias Current (Typical)	1 µA
Output type	Push-Pull
Features	Adjustable Hysteresis and Latch Function
TLV3603-Q1	

Analog Engineer's Circuit

LVDS GaN Driver Transmitter Circuit With High-Speed Comparator

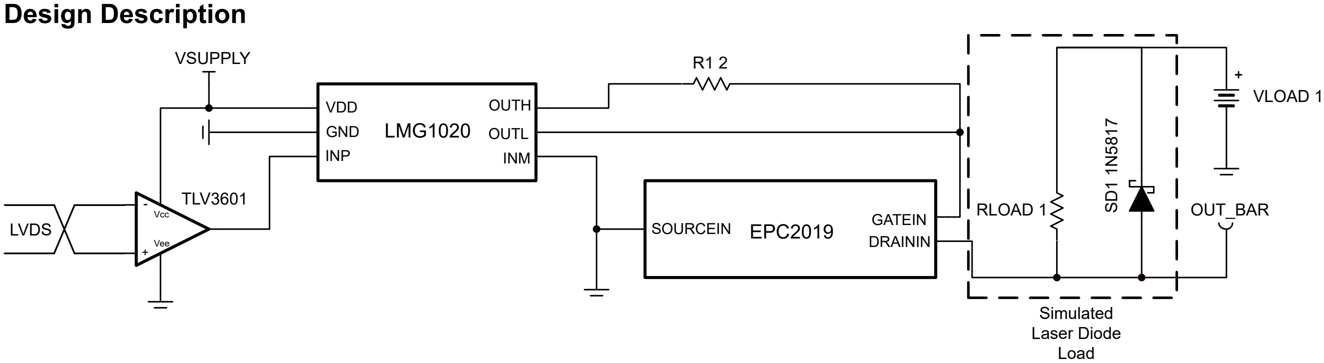
Amplifiers

Design Process

Design Goals

System Supply	Input Type	Output Pulse Width 50% to 50% to Drive LED	FET Switch Type
5 V	LVDS	3 ns ±10%	Low-Side

Design Description



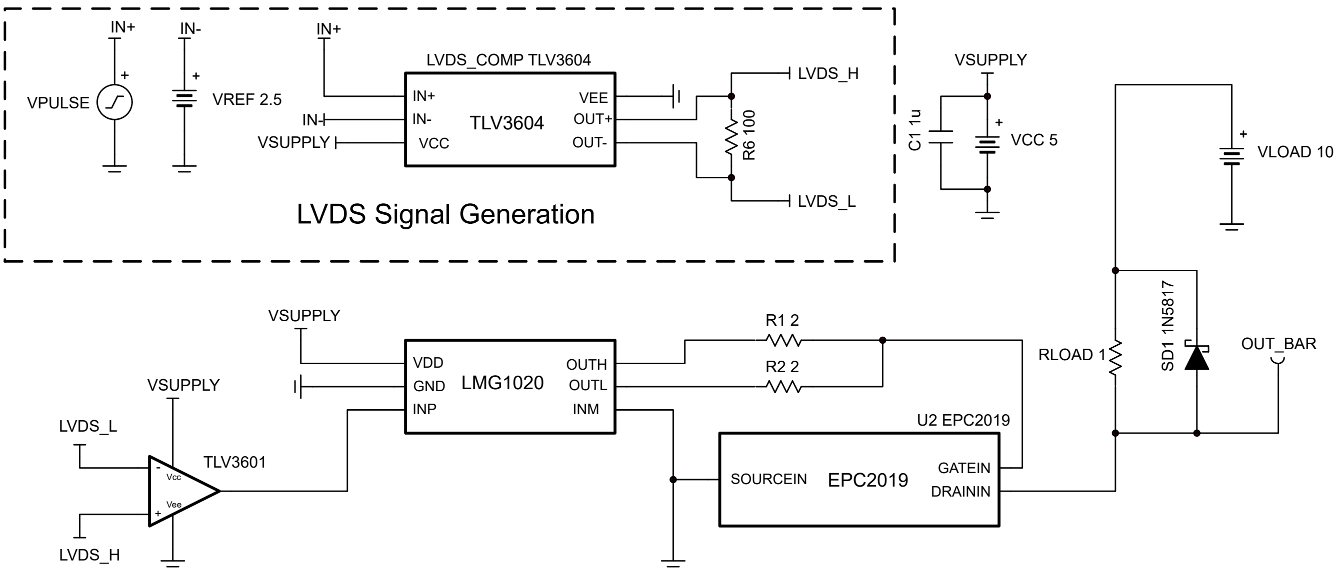
LVDS GaN Driver Transmitter Circuit

For this application, it is crucial to produce as narrow of a pulse as possible when driving a laser diode. For this design, the output of the GaN FET produces a 3-ns wide pulse that can be used to control a low-resistance, 1-Ω load. It is common to use low-voltage differential signal (LVDS) on a long cable or long trace to reduce EMI. The inputs to the GaN FET driver interface circuit must also accept LVDS inputs. To provide speed and accept LVDS input signals, the TLV3601 high-speed comparator is used. The TLV3601 is used to convert an LVDS signal to a single-ended output to drive the input of a GaN FET driver. The EPC2019 GaN FET and the LMG1020 GaN FET driver are also used. The design requirements are reflected in the Design Goals table.

Design Notes

1. Select a high-speed comparator that can be driven differentially by an LVDS signal
2. The low-resistance, 1-Ω load is used in simulation in place of an LED
3. Both the TLV3601 and the LMG1020 devices are powered from a 5-V supply (VSUPPLY)

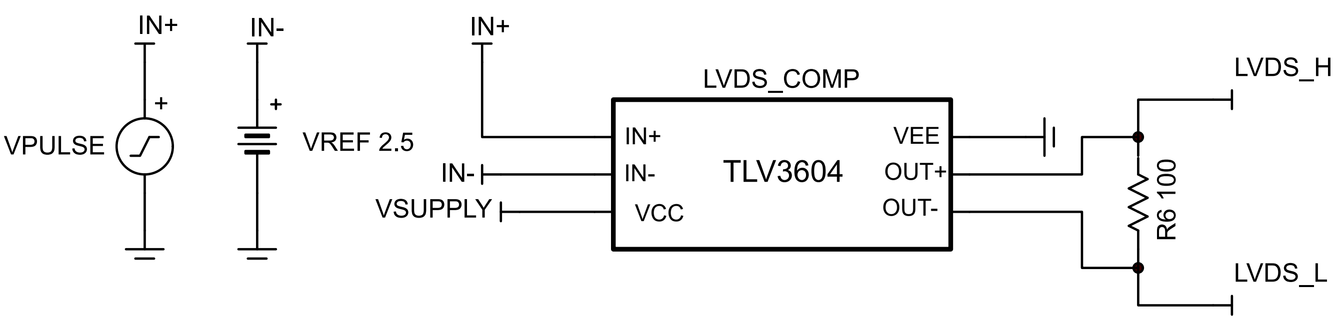
Design Steps



Complete Design Circuit

Step 1: LVDS Generation Using the TLV3604

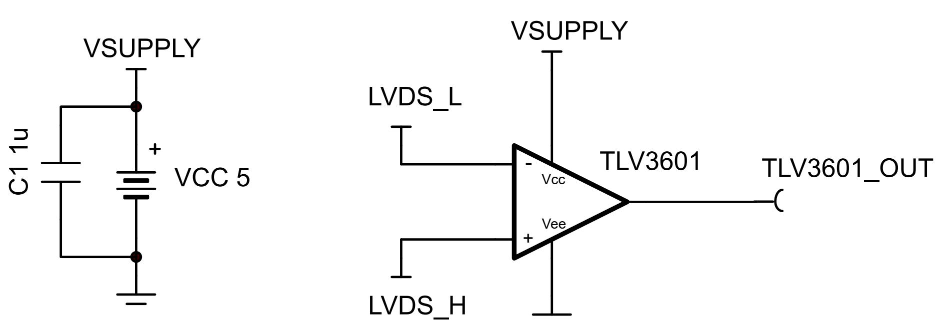
The TLV3604 non-inverting input is driven by a 100-mV, 3-ns pulse with a 2.5-V DC offset (VPULSE).



LVDS Generation Using the TLV3604

Step 2: LVDS to Single-Ended Output Conversion Using the TLV3601

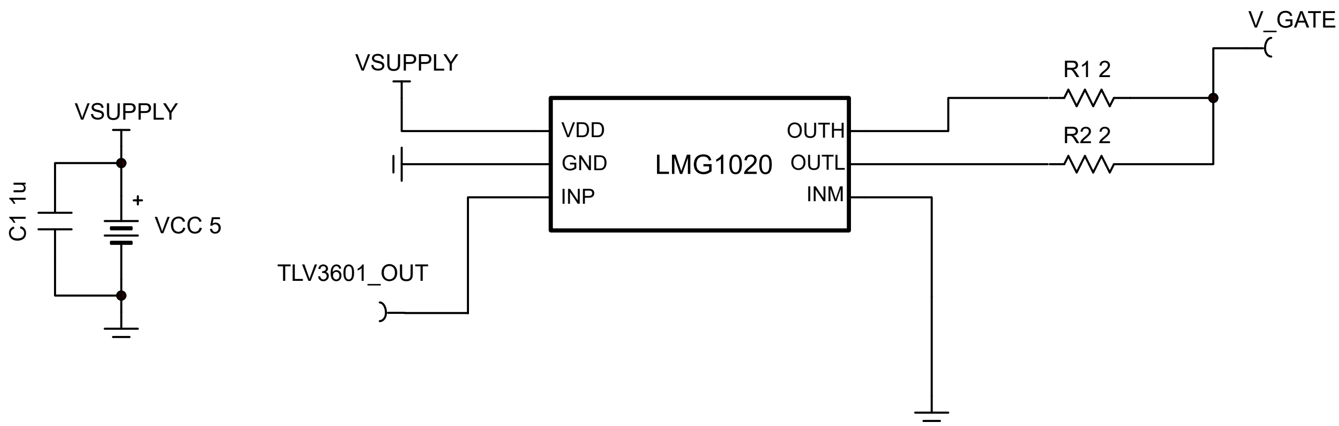
The LVDS outputs of the TLV3604 (LVDS_H and LVDS_L) are used to drive the inputs of the TLV3601. Since the outputs of the TLV3604 are terminated with a 100-Ω load, the voltage across this load can differentially drive the input of the TLV3601.



Connecting the TLV3601

Step 3: Configuring the GaN FET Driver

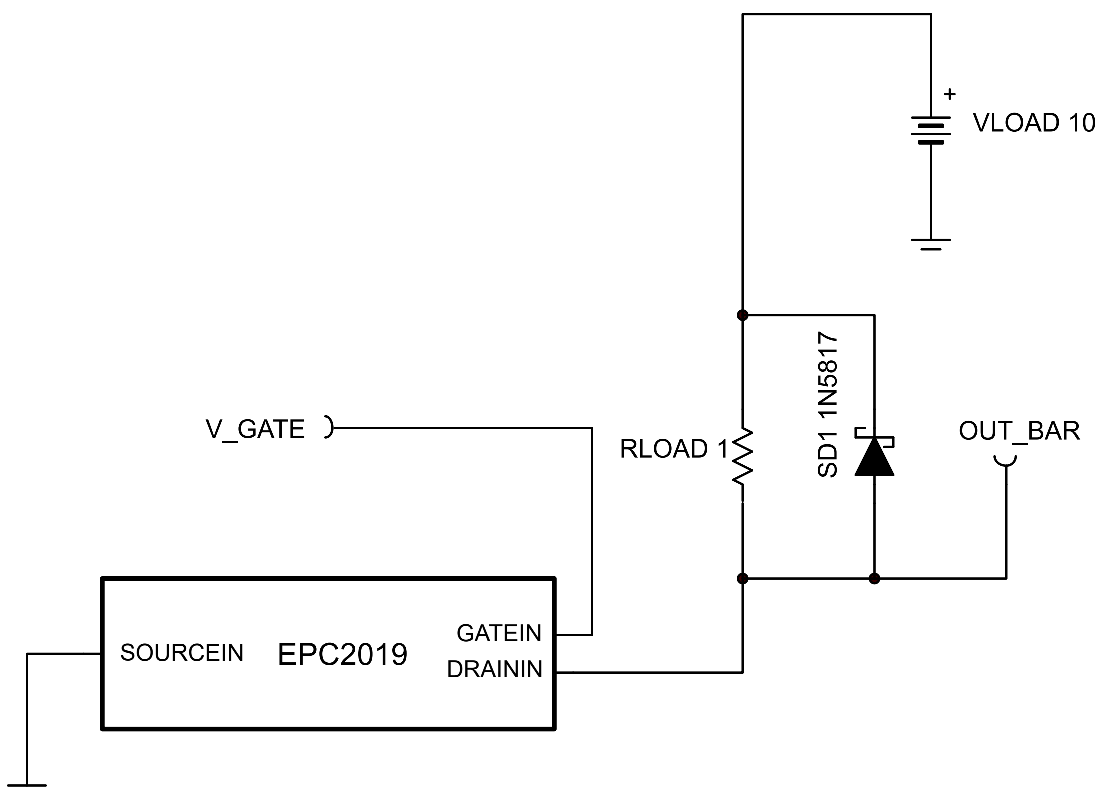
The LMG1020 enable pin (INM in the TINA simulation model) is active low and thus can be left grounded to keep the LMG1020 enabled. The series resistances on the outputs follow the *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications* data sheet recommended minimum value of 2 Ω in the *Typical Applications* section. The shorted outputs then drive the gate of the EPC2019 GaN FET (V_GATE). The LMG1020 input is driven by the output of the TLV3601 (TLV3601_OUT).



LMG1020 Configuration

Step 4: Connecting the EPC2019 GaN FET

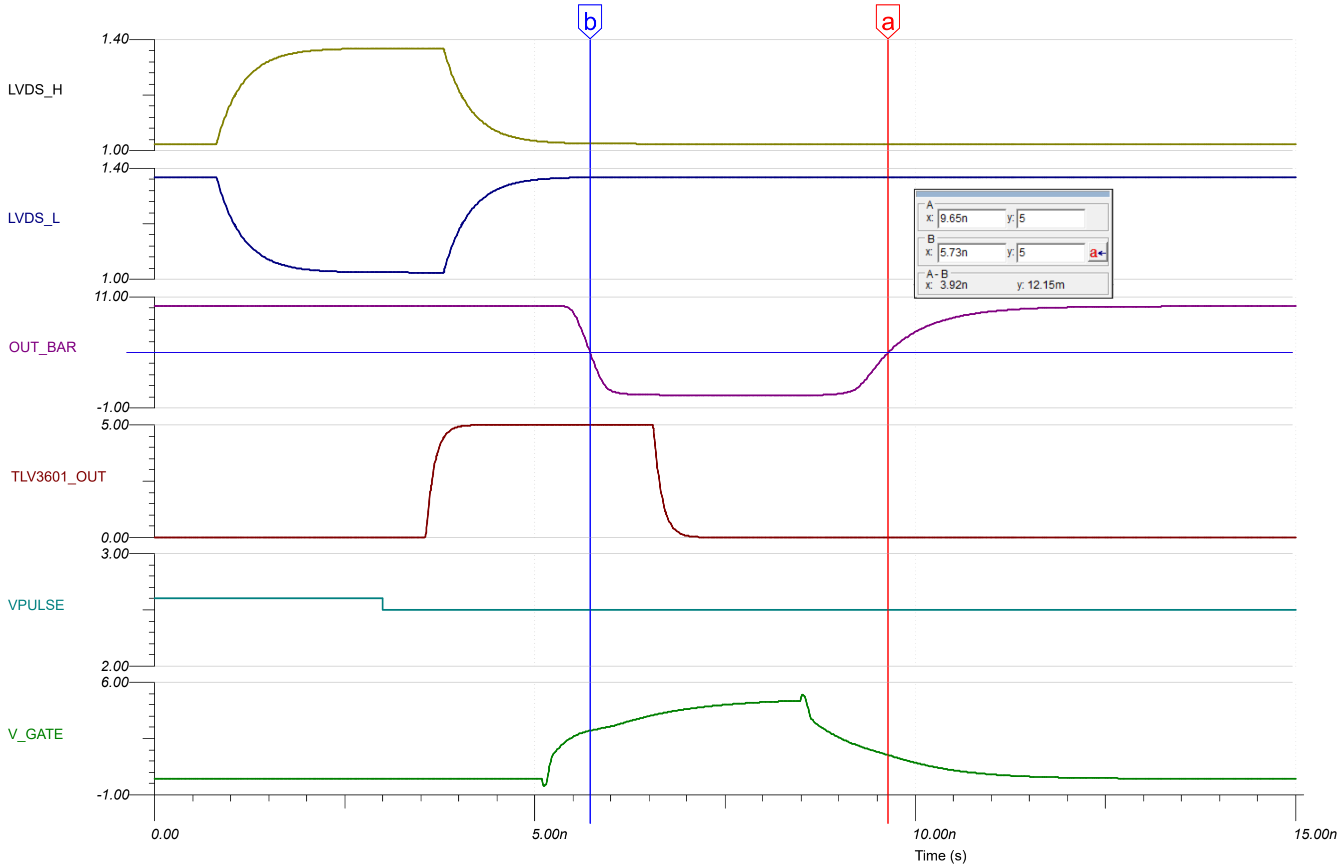
The GaN FET controls the 10-V supply current through the 1-Ω load. As a safety feature, a Schottky diode was placed in parallel with the load to ensure that the voltage across the load does not exceed 20 V.



Low-Side GaN FET Connections

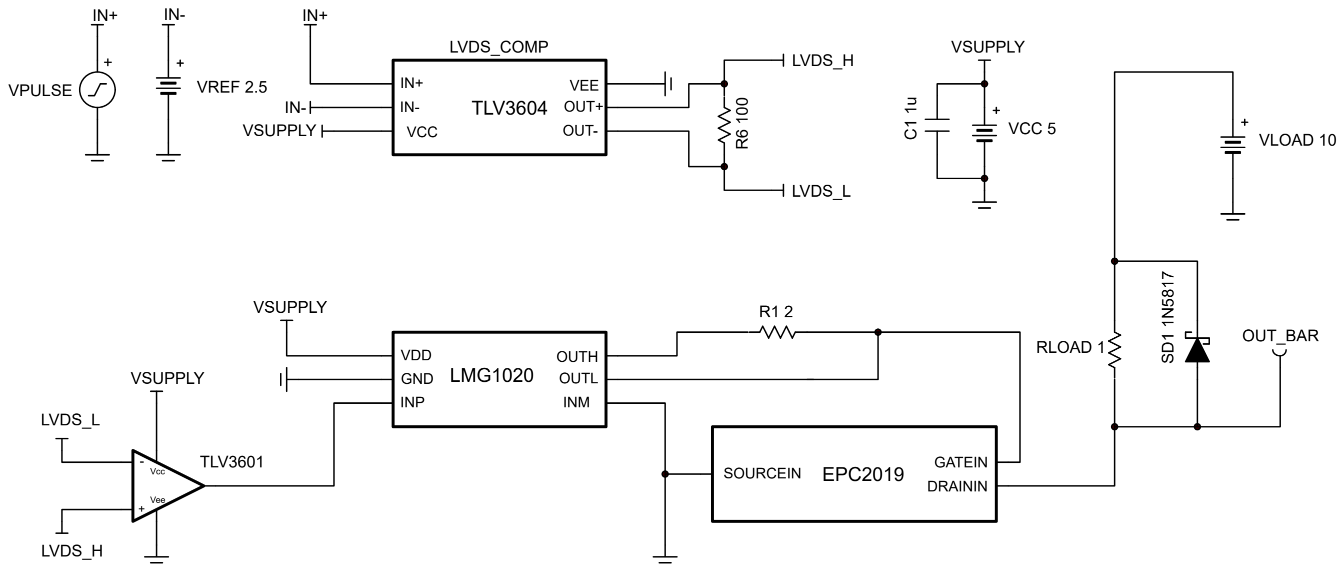
Transient Simulation Results

Using the "VPULSE" pulse waveform generator feeding into the TLV3604, the voltage below the 1-Ω load resistance is monitored as *OUT_BAR*. When the gate of the GaN FET is sufficiently driven, the voltage evident at the drain is approximately 0 V. The following image shows the initial simulation results.



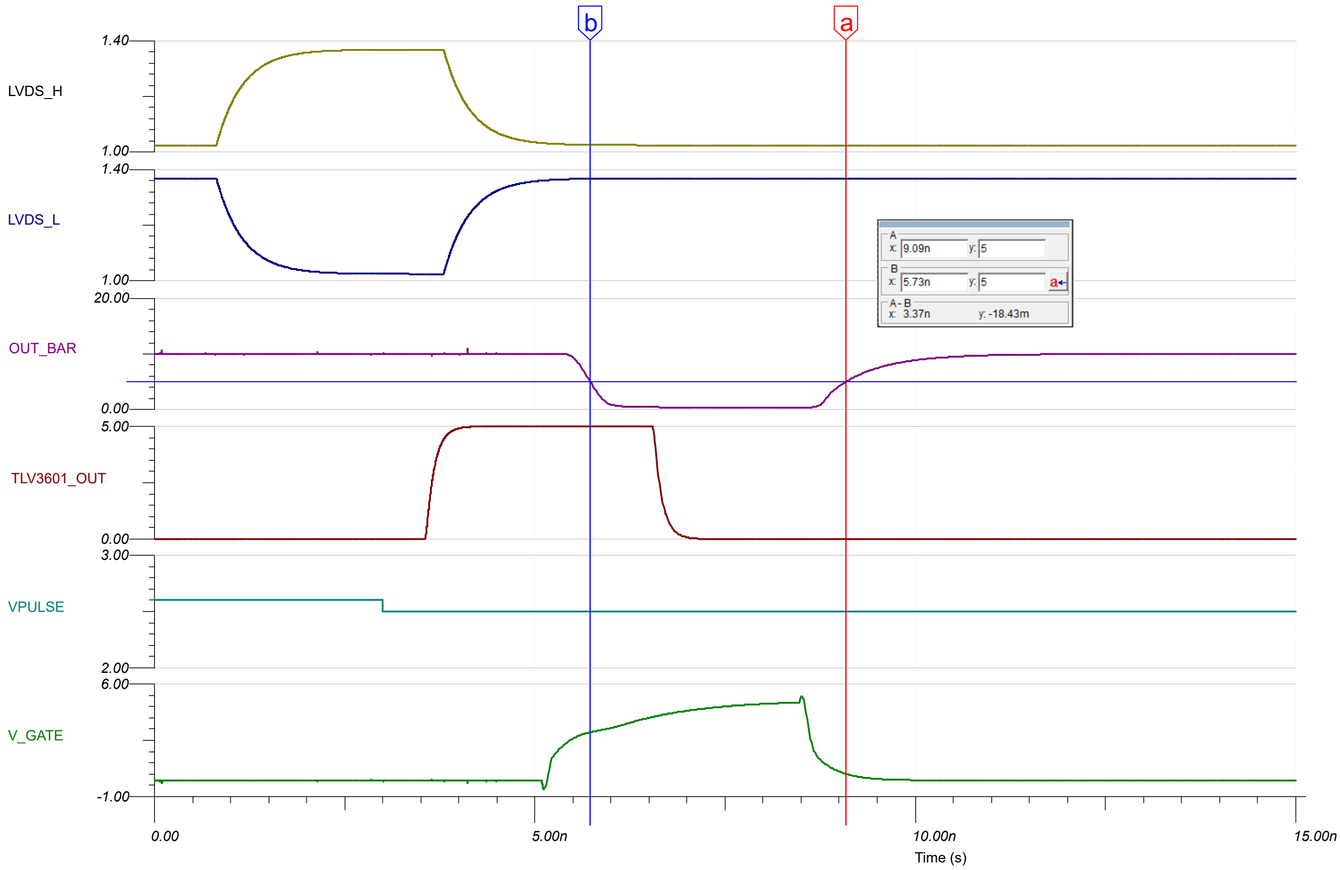
Initial Simulation Results

As depicted by Initial Simulation Results, the pulse width is approximately 0.6 ns wider than the design requirement at 3.92 ns. This is partly due to the series resistances on the gate of the EPC2019 that are used to avoid voltage overstress due to inductive ringing. To improve the turn-off time of the GaN FET Driver and GaN FET, the OUTL output of the LMG1020 is shorted to the gate of the EPC2019 as recommended in the *Typical Applications* section of the *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications* data sheet.



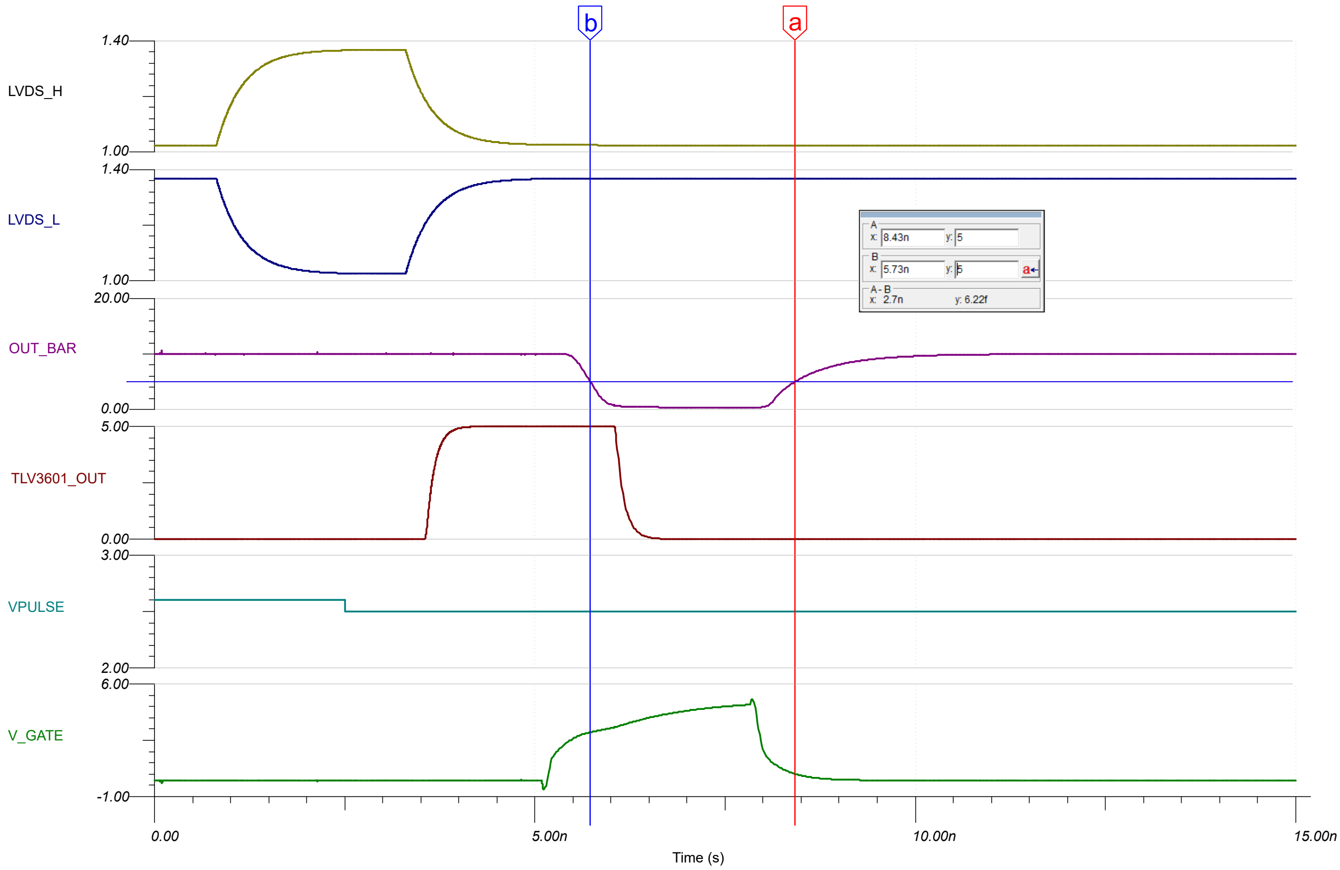
Modified Schematic to Improve Pulse Width

Next, the circuit is simulated again to see if the pulse width has been reduced to meet the design requirements.



Simulation Results After Removing Resistor

As illustrated by the simulation results in Simulation Results after Removing Resistor, the width of OUT_BAR is slightly out of the design requirement with a pulse width of 3.37 ns. To further improve the pulse width, a narrower LVDS pulse is sent to the TLV3601. To do this, the pulse width of the generator driving the non-inverting input of the TLV3604, VPULSE is reduced. The generator pulse width is adjusted to 2.5 ns to ensure the pulse width is within the design requirement. Design Compliant Simulation illustrates a simulated pulse width of 2.70 ns that complies with the design requirement.



Design Compliant Simulation

Design References

See the Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

See the following documents from Texas Instruments:

- *When to Use High-Speed Comparators or ADCs for Distance Measurements in Optical Time-of-Flight Systems* application report
- *TLV3601, TLV3603 325 MHz High-Speed Comparator with 2.5 ns Propagation Delay* data sheet
- *LMG1020 5-V, 7-A, 5-A Low-Side GaN and MOSFET Driver For 1-ns Pulse Width Applications* data sheet

Circuit SPICE Simulation File: SNOM733

For more information on many comparator topics including hysteresis, propagation delay, and input common-mode range, see the TI Precision Labs training.

Design Featured Comparator

TLV3601	
V_s	2.4 V–5.5 V
V_{inCM}	–0.2 V to 5.7 V
V_{os} (offset voltage at 25°C) (Max) (mV)	5
I_q	6 mA per channel
T_{PD} (ns)	2.5
Output type	Push-pull
#Channels	1
TLV3601	

Design Alternate Comparator

	TLV3603	TLV3501
V_s	2.4V–5.5V	2.7 V–5.5 V
V_{inCM}	–0.2V to 5.7V	–0.2 V to 5.7 V
V_{os} (offset voltage at 25°C) (Max) (mV)	5	6.5
I_q	6 mA per channel	3.2
T_{PD} (ns)	2.5	4.5
Output type	Push-pull	Push-pull
#Channels	1	1
Features	Configurable Hysteresis	Shutdown
Product Folder	TLV3603	TLV3501

Application Note
Low-Power, Bidirectional Current-Sensing Circuit

TEXAS INSTRUMENTS

Design Goals

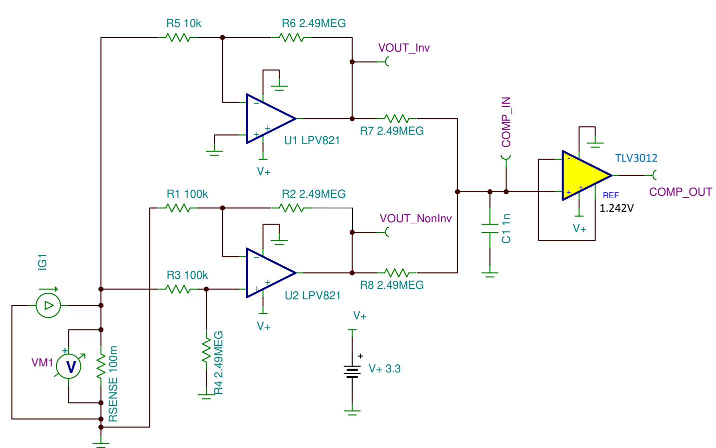
Overcurrent Levels		Supply	
I_{IN} (min)	I_{IN} (max)	V+	V–
–0.1 A	1.0 A	3.3 V	0 V

Design Description

This low-power, low-side, bidirectional current sensing solution uses two nano-power, zero-drift amplifiers (LPV821) and one micro-power comparator with an integrated, precision reference (TLV3012). This circuit is well-suited for battery powered devices where charging current and system current need to be monitored accurately. The gain of U1 and U2 are set independently.

As shown in the application circuit, the LPV821 amplifiers are connected out of phase across R_{SENSE} to amplify the currents of opposite polarity. Amplifier U2 linearly amplifies the charging (positive) current while amplifier U1 linearly amplifies the system (negative) current. When U2 is monitoring the positive current, U1 drives its output to ground. Similarly, U2 drives its ouput to ground when U1 monitors the negative current. The amplifier outputs are ORed together with resistors R_7 and R_8 while U1 or U2 provide the ground reference creating a single output voltage for the comparator to monitor.

If a regulated supply or reference is already available in the system, the TLV3012 can be replaced by a nano-power comparator such as the TLV7031. Moreover, if the charging current and system current have equal magnitudes, the gains of amplfier U1 and U2 can be set equal to each other. Even with the gains of the amplifiers being equal, ORing the amplifier outputs allows one comparator to detect overcurrent conditions for both charging and system current.



Design Notes

1. To minimize errors, utilize precision resistors and set $R_1 = R_3$, $R_2 = R_4$, and $R_7 = R_8$.
2. Select R_{SENSE} to minimize the voltage drop at max current and to reduce amplifier offset error when monitoring minimum current levels.
3. Select the amplifier gains so COMP_IN reaches 1.242 V when the charging and system currents reach their critical levels and avoid operating the amplifiers outside of their linear range.

Design Steps

1. Determine the transfer equation given $R_1 = R_3$, $R_2 = R_4$, and $R_7 = R_8$.

   Inverted Path:

   $$\mathrm{COMP\_IN} = -I_{G1} \times R_{SENSE} \times \left(-\frac{R_6}{R_5}\right) \times \left(\frac{R_8}{R_7 + R_8}\right)$$

   Non-Inverted Path:

   $$\mathrm{COMP\_IN} = I_{G1} \times R_{SENSE} \times \left(\frac{R_4}{R_3 + R_4}\right) \times \left(\frac{R_1 + R_2}{R_1}\right) \times \left(\frac{R_7}{R_7 + R_8}\right)$$

2. Select the SENSE resistor value assuming a maximum voltage drop (V_{SENSE}) of 100 mV when charging at 1 A and a minimum system current of 10 mA.

   $$R_{SENSE}(\max) = \frac{V_{SENSE}(\max)}{I_{G1}(\max)} = \frac{100\ \mathrm{mV}}{1\ \mathrm{A}} = 100\ \mathrm{m\Omega}$$

   $$\text{with}\quad I_{G1}(\min) = 10\mathrm{mA},\quad V_{SENSE} = 10\mathrm{mA} \times 100\mathrm{m\Omega} = 1\ \mathrm{mV} >> \mathrm{VOS}(\max) = 10\ \mu\mathrm{V}$$

3. Select ORing resistor R_7 and R_8 to generate COMP_IN.
   a. An equal attenuation factor of two is applied to the input of the comparator with $R_7 = R_8$. Choose large values to minimize current consumption from the output of the amplifiers.
   b. Special care must be taken when validating the voltage at COMP_IN. Since R_7 and R_8 are large impedance values, the input impedance of an oscilloscope probe or the input to a digital voltmeter can alter the measured voltage. Common probe and voltmeter input impedances are 10MΩ and this will attenuate the signal measured.

   $$\text{with}\quad R_7 = R_8 = 2.49\ \mathrm{M\Omega},$$
   $$\mathrm{COMP\_IN} = (\mathrm{VOUT\_Inv}\ \ \text{or}\ \ \mathrm{VOUT\_NonInv})/2$$

4. Select the amplifier gain such that COMP_IN reaches 1.242 V when the currents reach the critical threshold.

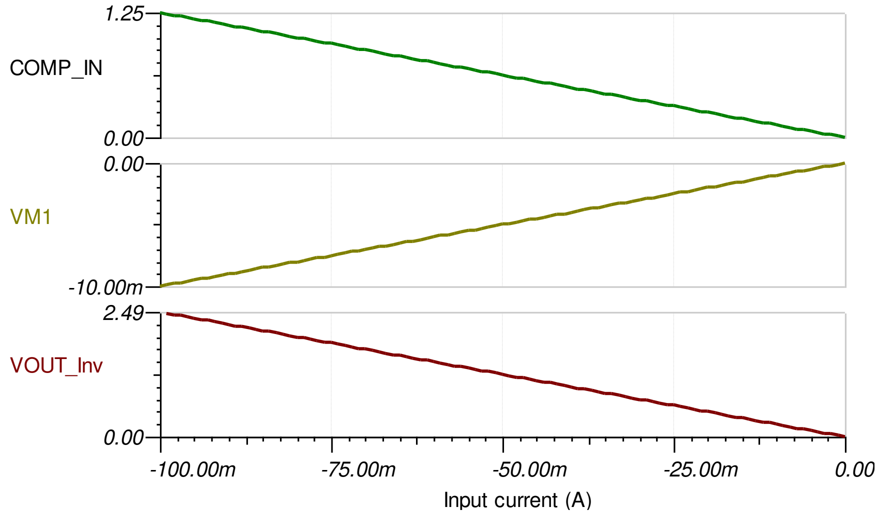
   $$\mathrm{Gain} = \frac{2 \times Comparator\ \ REF}{R_{SENSE} \times |I_{G1}\ (max)|}$$

   $$\mathrm{Gain}\ (Inv) = \frac{2 \times 1.242}{0.1 \times (-0.1)} = \frac{(-R_6)}{R_5} \approx -249\frac{\mathrm{V}}{\mathrm{V}}$$
   $$\mathrm{Gain}\ (NonInv) = \frac{2 \times 1.242}{0.1 \times 1.0} = \frac{R_4}{R_3 + R_4} \times \frac{R_1 + R_2}{R_1} \approx 24.9\frac{\mathrm{V}}{\mathrm{V}}$$

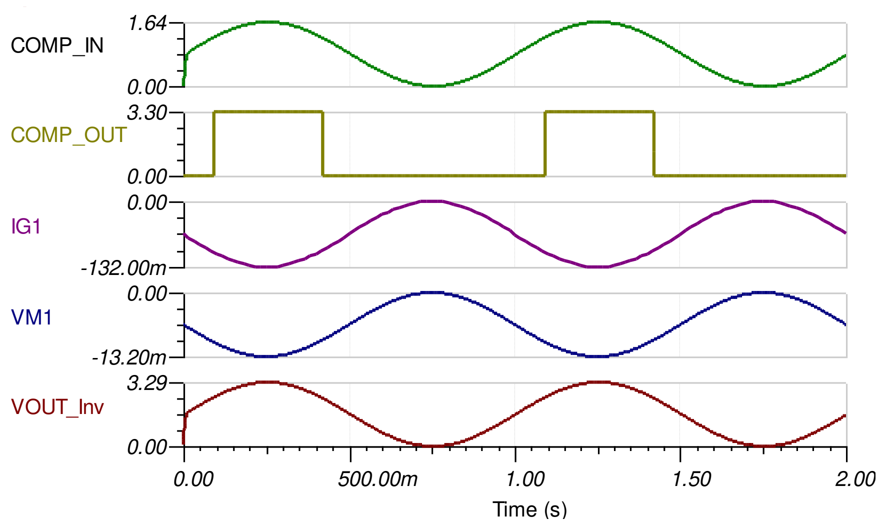
   $$R_1 = R_3 = 100\ \mathrm{k\Omega}\ \text{(Standard Value)}$$
   $$R_5 = 10\ \mathrm{k\Omega}\ \text{(Standard Value)}$$
   $$R_2 = R_4 = R_6 = 2.49\ \mathrm{M\Omega}\ \text{(Standard Value)}$$

Design Simulations

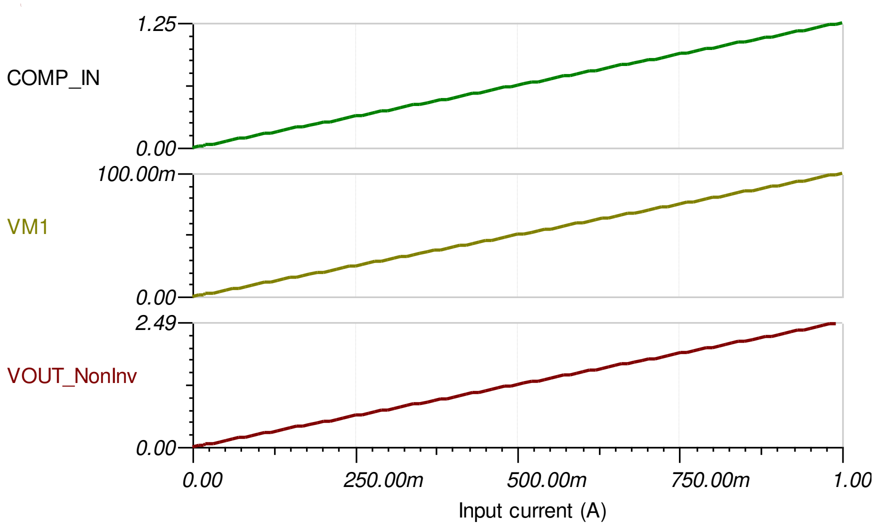
DC Simulation Results (VOUT_Inv)



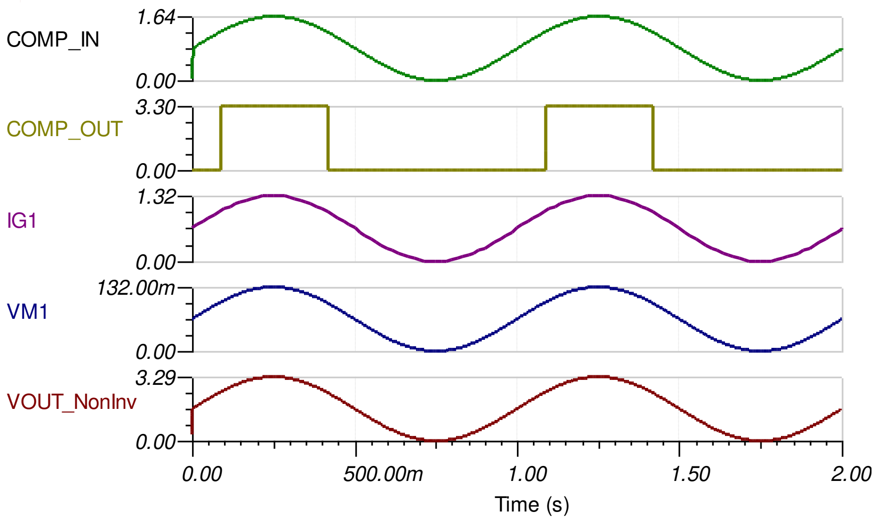
Transient Simulation Results (VOUT_Inv)



DC Simulation Results (VOUT_NonInv)



Transient Simulation Results (VOUT_NonInv)



Tech Note and Blog References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See *Advantages of Using Nanopower Zero Drift Amp for Mobile Phone Battery Monitoring*.

See *Current Sensing in No-Neutral Light Switches*.

See *GPIO Pins Power Signal Chain in Personal Electronics Running on Li-Ion Batteries*.

See Current Sensing Using NanoPower Op Amps Blog.

Design Featured Op Amp

LPV821	
V_S	1.7 V to 3.6 V
Input V_{CM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1.5 µV
V_{os} Drift	20 nV/°C
I_q	650 nA/Ch
I_b	7 pA
UGBW	8 kHz
#Channels	1
LPV821	

Design Alternate Op Amp

TLVx333	
V_S	1.8 V to 5.5 V
Input V_{CM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	2 µV
V_{os} Drift	20 nV/°C
I_q	17 µA/Ch
I_b	70 pA
UGBW	350 kHz
#Channels	1, 2, and 4
TLV333	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from March 4, 2018 to February 18, 2019	Page
• Changed title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page	1

Analog Engineer's Circuit

LVDS data and clock recovery circuit with high-speed comparators

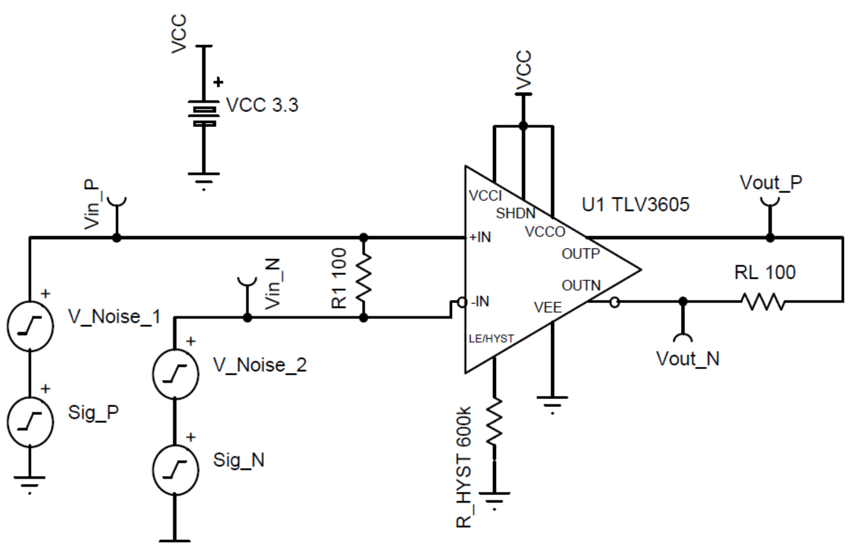
Amplifiers

Design Goals

Supply		Attenuated Input Signal		
V_{cc}	V_{ee}	V_i	V_{cm}	f
3.3V	0V	$50mV_{p\text{-}p}$	1.2V	1GHz

Design Description

The LVDS signal restoration circuit is used in digital systems to retrieve distorted clock or data waveforms. These clock and data signals can be attenuated and distorted on long traces due to stray capacitance, stray inductance, or reflections on transmission lines. The comparator is used to sense the attenuated and distorted input signal and convert it into a full scale LVDS output signal. This circuit can also be used to convert from single-ended signals to LVDS signaling. In that case, a dynamic reference voltage is connected to the inverting terminal of the comparator which is extracting the common-mode voltage from the input signal.



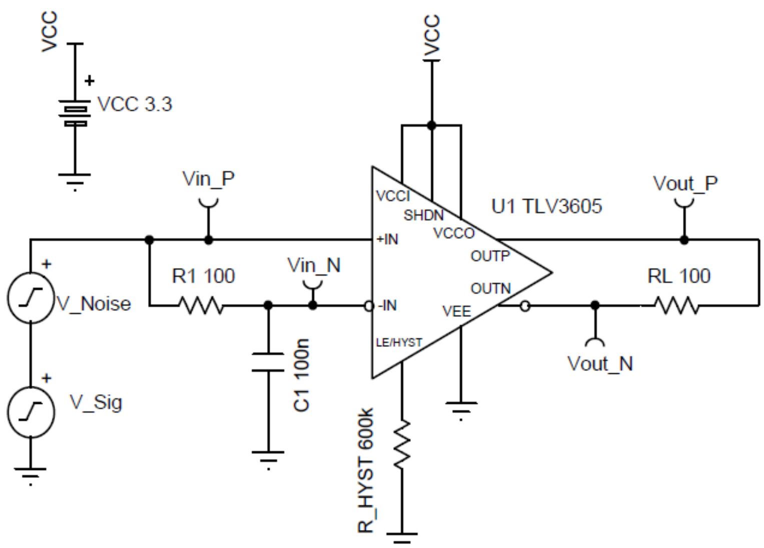
Design Notes

1. Select a comparator with low input offset voltage and fast propagation delay.
2. A comparator with a toggle frequency larger than the input signal frequency should be used to properly process the incoming digital signal. A margin of 30% is sufficient to allow for process and temperature variations if a minimum value is not warranted in the data sheet.
3. The signal should be symmetric around the waveform midpoint for the dynamic reference to accurately determine the common mode voltage of the input signal. For signals with duty cycles outside of 30–70%, the dynamic reference must be replaced with an external reference source.

Design Steps (LVDS Input)

1. Connect the positive and negative portions of the LVDS input to the non-inverting and inverting terminals, respectively, of the comparator.
2. Ensure that the LVDS signal is properly terminated with a 100-Ω resistor, R_1, connected between both inputs.
3. Connect VCC to the TLV3605 $\overline{\text{SHDN}}$ pin to disable the shutdown feature of the device.
4. Terminate the output signals using a 100-Ω resistor, R_L, connected between both nodes.
5. If the input signals are noisy in addition to being attenuated, TLV3605 is able to handle the noise though implementation of its adjustable hysteresis feature. This pin can be driven with a voltage source or be attached to a resistor to VEE and can cause the comparator to have a hysteresis up to 65mV, as well as latching the output depending on the voltage seen at the pin. See the *TLV3604, TLV3605 800-ps High-Speed RRI Comparator with LVDS Outputs* data sheet for more information. For this circuit, a hysteresis of 10mV is implemented to counter the noisy input signals by connecting a 600-kΩ resistor to VEE.

Design Steps (Single-Ended Input)



1. Set the non-inverting input of the comparator to the input data signal.
2. Create a dynamic reference from a low-pass network using a capacitor, C_1, and resistor, R_1. Connect the input of the network to the non-inverting input and the output to the inverting input.
3. Size the values of the dynamic reference so that its cutoff frequency is significantly below the operating frequency of the input signal while ensuring the time constant of the network is small enough for maximum responsivity. Let C_1 = 0.1µF and designing for a time constant τ of 10µs, calculate the needed resistor value:

$$\tau = R_1 C_1$$

$$10\mu s = R_1(100nF) \Rightarrow R_1 = 100\Omega$$

Using the solved-for resistor value, ensure the cutoff frequency is still significantly below the input signal frequency.

$$f_{cutoff} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(100\Omega)(100nF)} = 15.915khz \ll 1GHz$$

The time constant τ has an inverse relationship with f_{cutoff}. The quicker τ is, the more reactive the dynamic reference output node is to the input while pushing the cutoff frequency higher. However, if the cutoff frequency of the dynamic reference approaches the operating frequency of the input signal, the output of the network is unable to properly filter out the high-frequency component of the input signal, thereby failing to generate a stable DC reference voltage to compare the input signal against.

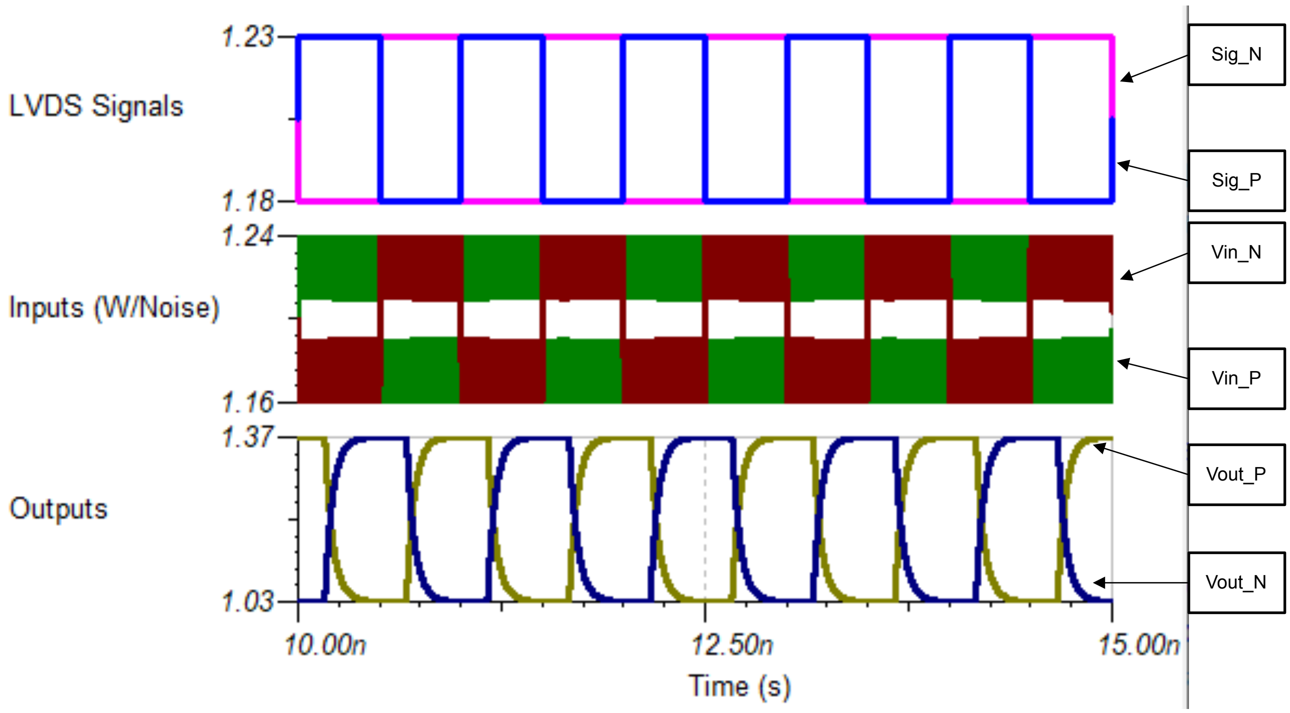
A ramification to consider when balancing the accurate filtering of the signal versus τ is start-up time. As the system starts in an uncharged state, once the system is active, there is a time period (around 5τ) until the voltage level at the inverting input is at an accurate level.

4. Connect VCC to the TLV3605 $\overline{\text{SHDN}}$ pin to disable the shutdown feature of the device.
5. Terminate the output signals using a 100-Ω resistor R_L connected between both nodes.
6. If the input signal is noisy in addition to being attenuated, the TLV3605 is able to handle the noise though implementation of its adjustable hysteresis feature. This pin can be driven with a voltage source or be attached to a resistor to VEE and can cause the comparator to have a hysteresis up to 65mV, as well as latching the output depending on the voltage seen at the pin. See the *TLV3604, TLV3605 800-ps High-Speed RRI Comparator with LVDS Outputs* data sheet for more information. For this circuit, a hysteresis of 10mV is implemented to counter the noisy input signals by connecting a 600-kΩ resistor to VEE.

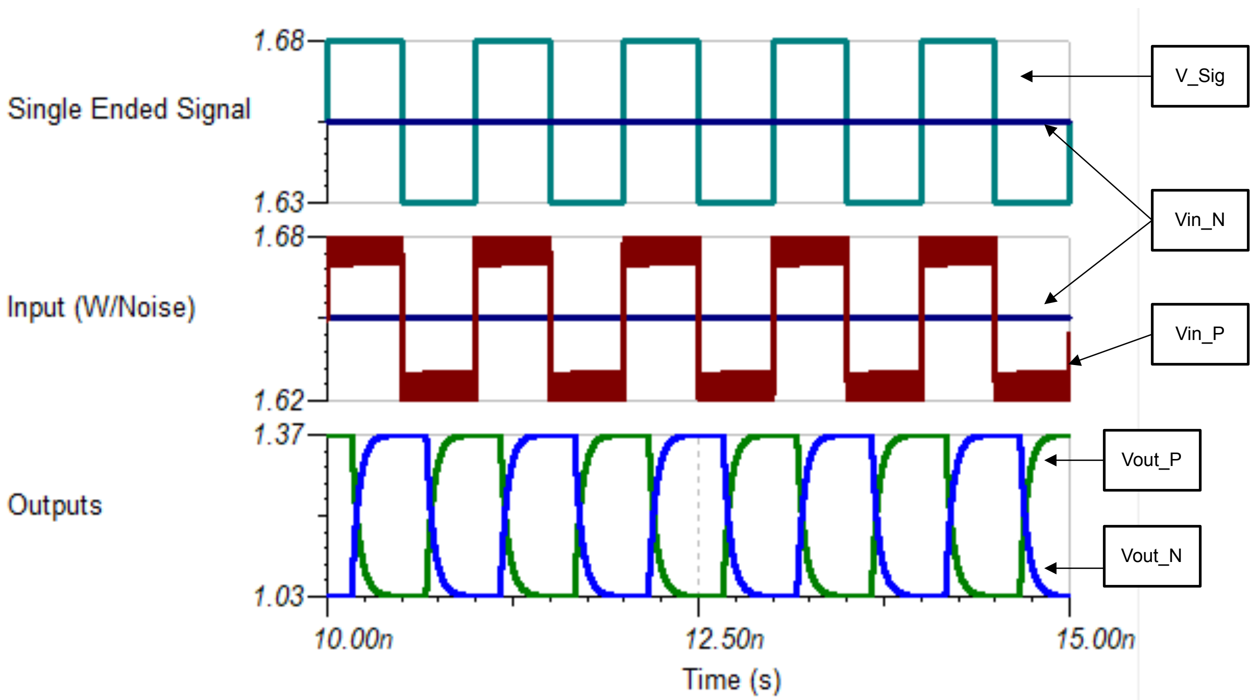
Design Simulations

Transient Simulation Results

LVDS Input



Single-Ended Input



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit spice simulation file, SNOM771 (LVDS) and SNOM710 (Single-Ended).

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, TI Precision Labs.

Design Featured Comparator

TLV3605	
V_{ss}	2.4V to 5.5V
V_{inCM}	Rail-to-rail
t_{pd}	800ps
V_{os}	0.5mV
V_{HYS}	Adjustable (0–65mV)
I_q	12.7mA
Output Type	LVDS
f_{toggle}	1.5GHz
#Channels	1
www.ti.com/product/TLV3605	

Design Alternate Comparator

	TLV3604	LMH7220
V_{ss}	2.4V to 5.5V	2.7V to 12V
V_{inCM}	Rail-to-rail	Rail-to-rail
t_{pd}	800ps	2.9ns
V_{os}	0.5mV	9.5mV
V_{HYS}	N/A	N/A
I_q	12.1mA	6.8mA
Output Type	LVDS	LVDS
f_{toggle}	1.5GHz	440MHz
#Channels	1	1
	www.ti.com/product/tlv3604	www.ti.com/product/lmh7220

Analog Engineer's Circuit

High-Speed Overcurrent Detection Circuit

TEXAS INSTRUMENTS

Design Goal

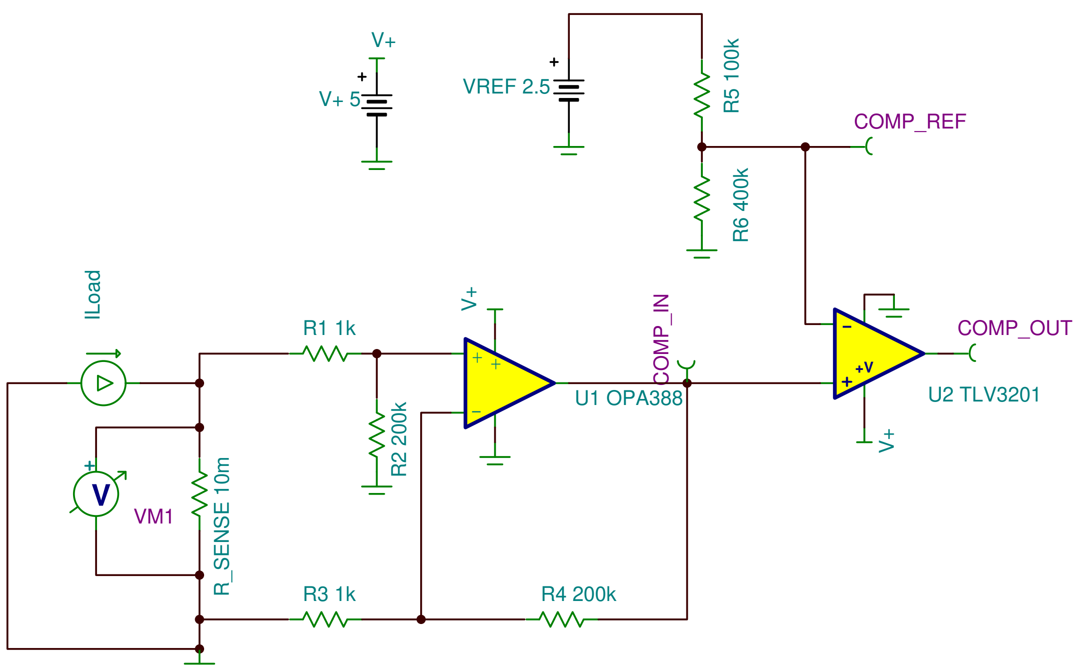
Overcurrent Levels		Supply		Transient Response Time
I_{IN} (min)	I_{IN} (max)	V+	V–	t
0 A	1.0 A	5 V	0 V	< 10 µs

Design Description

This high-speed, low-side overcurrent detection solution is implemented with a single zero-drift fast-settling amplifier (OPA388) and one high-speed comparator (TLV3201). This circuit is designed for applications that monitor fast current signals and overcurrent events, such as current detection in motors and power supply units.

The OPA388 is selected for its widest bandwidth with ultra-low offset and fast slew rate. The TLV3201 is selected for its fast response due to its small propagation delay of 40 ns and rise time of 4.8 ns. This allows the comparator to quickly respond and alert the system of an overcurrent event all within the transient response time requirement. The push-pull output stage also allows the comparator to directly interface with the logic levels of the microcontroller. The TLV3201 also has low power consumption with a quiescent current of 40 µA.

Typically for low-side current detection, the amplifier across the sense resistor can be used in a noninverting configuration. The application circuit shown, however, uses the OPA388 as a differential amplifier across the sense resistor. This provides a true differential measurement across the shunt resistor and can be beneficial in cases where the supply ground and load ground are not necessarily the same.



Design Notes

1. To minimize errors, choose precision resistors and set $R_1 = R_3$, and $R_2 = R_4$.
2. Select R_{SENSE} to minimize the voltage drop across the resistor at the max current of 1 A.
3. Due to the ultra-low offset of the OPA388 (0.25 µV), the effect of any offset error from the amplifier is minimal on the mV range measurement across R_{SENSE} .
4. Select the amplifier gain so COMP_IN reaches 2 V when the system crosses its critical overcurrent value of 1 A.
5. Traditional bypass capacitors are omitted to simplify the application circuit.

Design Steps

1. Determine the transfer equation where $R_1 = R_3$ and $R_2 = R_4$.

$$\text{COMP\_IN} = \left(R_{SENSE} \cdot I_{LOAD}\right) \cdot \left(\frac{R_2}{R_1 + R_2}\right) \cdot \left(1 + \frac{R_4}{R_3}\right)$$

2. Select the SENSE resistor value assuming a maximum voltage drop of 10 mV with a load current of 1 A in order to minimize the voltage drop across the resistor.

$$R_{SENSE} = \frac{V_{SENSE}(\max)}{I_{LOAD}(\text{critical})} = \frac{10\text{mV}}{1\text{A}} = 10\text{m}\Omega$$

3. Select the amplifier gain such that COMP_IN reaches 2 V when the load current reaches the critical threshold of 1 A.

$$\text{Gain} = \frac{\text{VREF}}{R_{SENSE} \cdot I_{LOAD}(\text{critical})} = \frac{2\text{ V}}{0.01\text{ V}} = \frac{R_2}{R_1 + R_2} \cdot 1 + \frac{R_4}{R_3} = 200$$

Set:

$$R_1 = R_3 = 1\text{k}\Omega$$

$$R_2 = R_4 = 200\text{k}\Omega$$

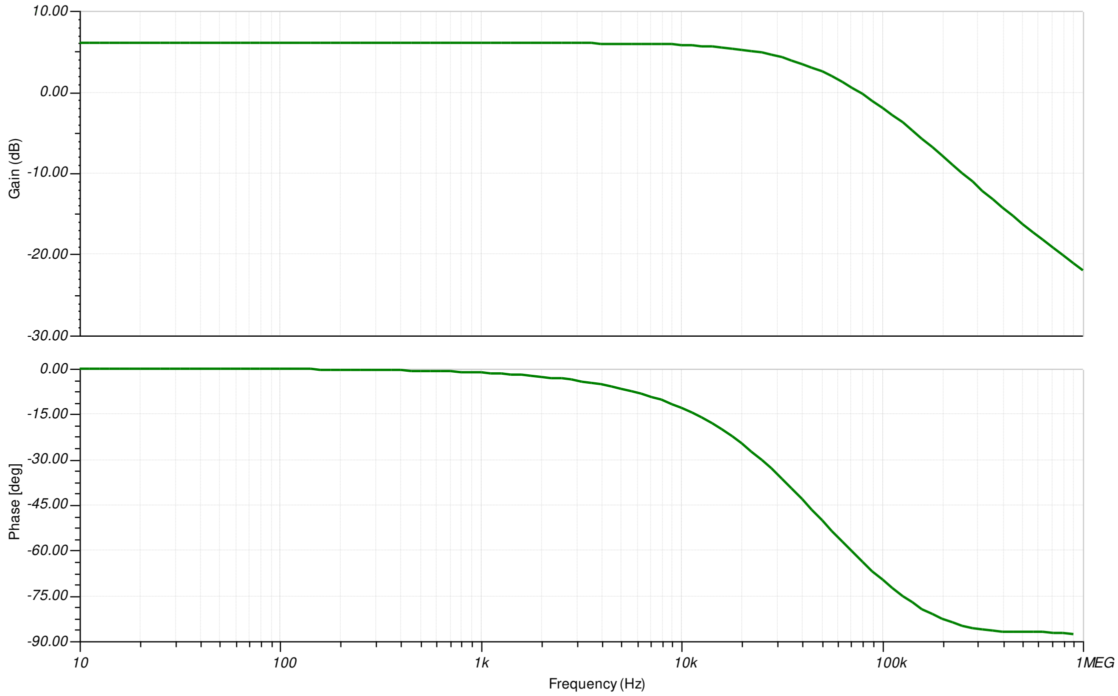
4. Calculate the transimpedance gain of the amplifier in order to verify the following AC simulation results:

$$V_{OUT} = I_{LOAD} \cdot 10\text{m}\Omega \cdot 200$$

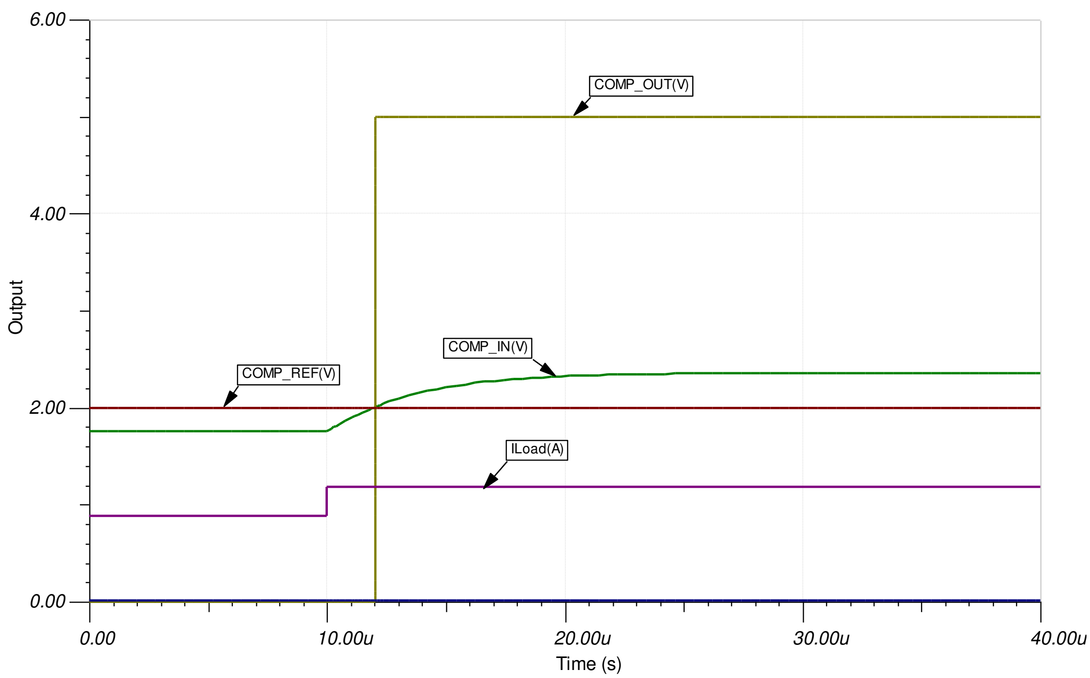
$$\frac{V_{OUT}}{I_{LOAD}} = 10\text{m}\Omega \cdot 200 = 2$$

Design Simulations

COMP_IN Transimpedance AC Simulation Results



Transient Response Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the Current sensing using nanopower op amps blog.

References

1. Texas Instruments, *Advantages of using nanopower, zero drift amplifiers for battery voltage and current monitoring in portable applications TI tech note*
2. Texas Instruments, *Current sensing in no-neutral light switches TI tech note*
3. Texas Instruments, *GPIO Pins power signal chain in personal electronics running on Li-Ion batteries TI tech note*

Design Featured Comparator

TLV3201	
V_S	2.7 V to 5.5 V
t_{PD}	40 ns
Input V_{CM}	Rail-to-rail
V_{os}	1 mV
I_q	40 µA
TLV3201	

Design Alternate Comparator

TLV7021	
V_S	1.6 V to 5.5 V
t_{PD}	260 ns
Input V_{CM}	Rail-to-rail
V_{os}	0.5 mV
I_q	5 µA
TLV7021	

Design Featured Op Amp

OPA388	
V_S	2.5 V to 5.5 V
Input V_{CM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.25 µV
V_{os} Drift	.005 µV/°C
I_q	1.7 mA/Ch
I_b	30 pA
UGBW	10 MHz
OPA388	

Design Alternate Op Amp

THS4521	
V_S	2.5 V to 5.5 V
Input V_{CM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	20 µV
V_{os} Drift	µV/°C
I_q	1 mA/Ch
I_b	0.6 µA
UGBW	145 MHz
THS4521	

Thermal Switch Circuit

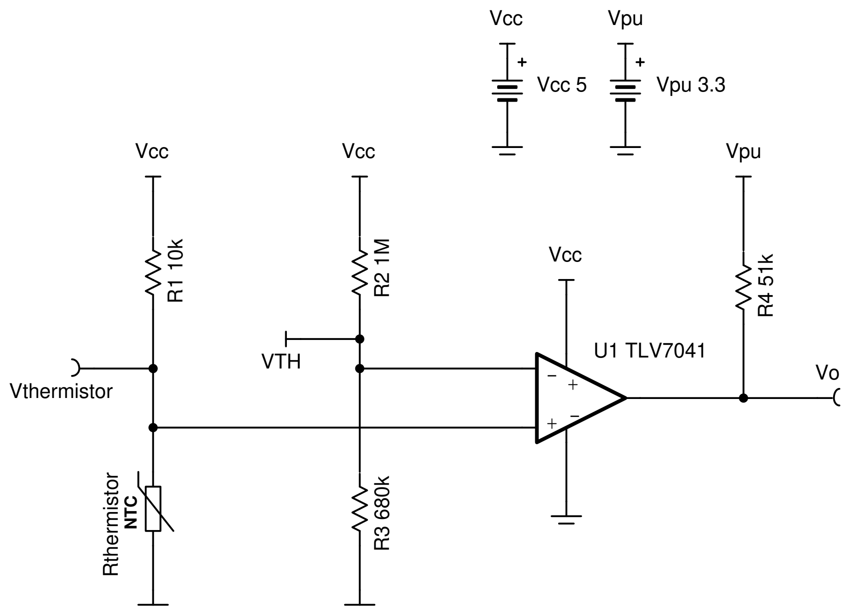
TEXAS INSTRUMENTS

Design Goals

Temperature Switching Point	Output		Supply		
T_{sp}	V_o = HIGH	V_o = LOW	V_{cc}	V_{ee}	V_{pu}
100 °C	$T_A < T_{sp}$	$T_A > T_{sp}$	5 V	0 V	3.3 V

Design Description

This thermal switch solution will signal low (to a GPIO pin) when a certain temperature is exceeded thus alerting when conditions are no longer optimal or device-safe. This circuit incorporates an NTC thermistor with a comparator configured in a non-inverting fashion.



Design Notes

1. The resistance of an NTC thermistor drops as temperature increases.
2. The TLV7041 has an open drain output, so a pull-up resistor is required.
3. Configurations where the thermistor is placed near the high side of the divider can be done; however, the comparator will have to be used in an inverting fashion to still have the output switch low.
4. To exercise good practice, a positive feedback resistor should be placed to add external hysteresis (for simplicity, it is not done in this example).

Design Steps

1. Select an NTC thermistor, preferably one with a high nominal resistance, R_0, (resistance value when ambient temperature, T_A, is 25 °C) since the TLV7041 has a very low input bias current. This will help lower power consumption, thus reducing the likelihood of reading a slightly higher temperature due to thermal dissipation in the thermistor. The thermistor chosen has its R_0 and its material constant, β, listed below.

   $$R_0 = 100\text{k}\Omega$$

   $$\beta = 3977\text{K}$$

2. Select R_1. For high temperature switching points, R_1 should be 10 times smaller than the nominal resistance of the thermistor. This causes a larger voltage difference per temperature change around the temperature switching point, which helps guarantee the output will switch at the desired temperature value.

   $$R_1 = \frac{R_0}{10}$$

   $$R_1 = \frac{100\text{k}\Omega}{10} = 10\text{k}\Omega \quad (\text{Standard Value})$$

3. Select R_2. Again, this can be a high resistance value.

   $$R_2 = 1\text{M}\Omega \quad (\text{Standard Value})$$

4. Solve for the resistance of the thermistor, $R_{thermistor}$, at the desired temperature switching point. Using the β formula is an effective approximation for thermistor resistance across the temperature range of -20 °C to 120 °C. Alternatively, the Steinhart-Hart equation can be used, but several device-specific constants must be provided by the thermistor vendor. Note that temperature values are in Kelvin. Here T_0 = 25 °C = 298.15K.

   $$R_{thermistor}\left(T_{sp}\right) = R_0 \times e^{\beta \times \left(\frac{1}{T_{sp}} - \frac{1}{T_0}\right)}$$

   $$R_{thermistor}\left(100°\text{C}\right) = 100\text{k}\Omega \times e^{3977\text{K} \times \left(\frac{1}{373.15\text{K}} - \frac{1}{298.15\text{K}}\right)}$$

   $$R_{thermistor}(100°\text{C}) = 6.85 \quad \text{k}\Omega$$

5. Solve for $V_{thermistor}$ at T_{sp}.

   $$V_{thermistor}\left(T_{sp}\right) = V_{cc} \times \frac{R_{thermistor}\left(T_{sp}\right)}{R_1 + R_{thermistor}\left(T_{sp}\right)}$$

   $$V_{thermistor}\left(100°\text{C}\right) = 5\text{V} \times \frac{6.85\text{k}\Omega}{10\text{k}\Omega + 6.85\text{k}\Omega} = 2.03\text{V}$$

6. Solve for R_3 with the threshold voltage, V_{TH}, equal to $V_{thermistor}$. This ensures that $V_{thermistor}$ will always be larger than V_{TH} until the temperature switching point is exceeded.

   $$R_3 = \frac{R_2 \times V_{TH}}{V_{cc} - V_{TH}}$$

   $$R_3 = \frac{1\text{M}\Omega \times 2.03\text{V}}{5\text{V} - 2.03\text{V}} = 685\text{k}\Omega$$

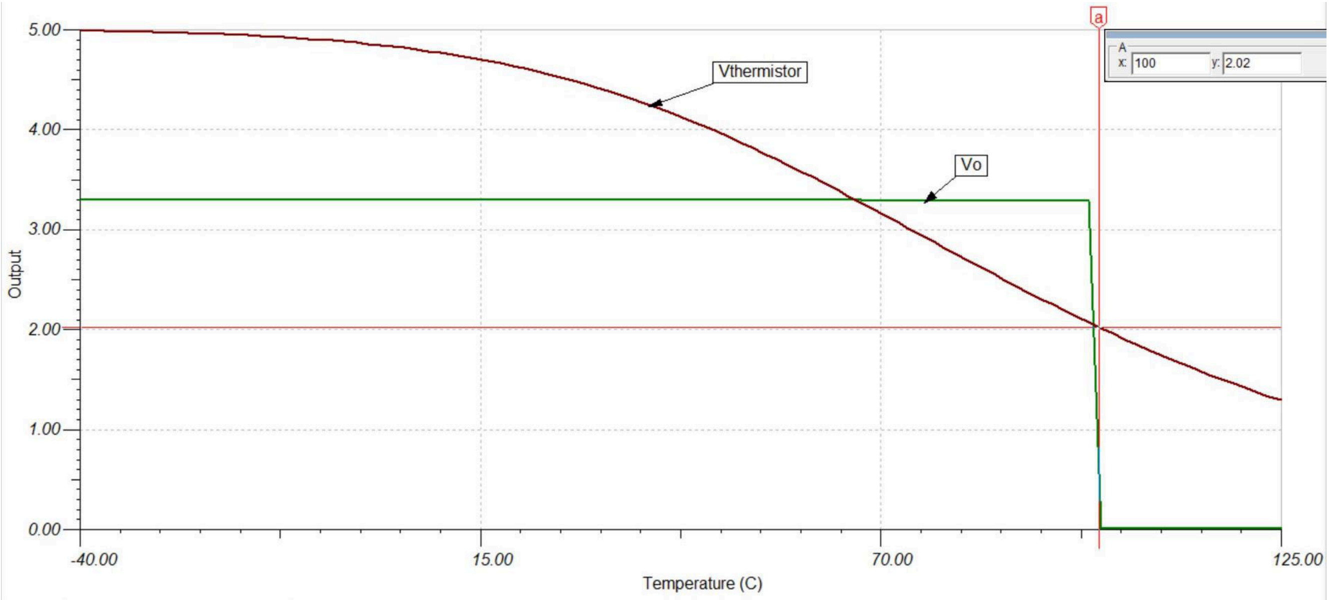
   $$R_3 = 680\text{k}\Omega \quad (\text{Standard Value})$$

7. Select an appropriate pull up resistor, R_4. Here, V_{pu} = 3.3 V (digital high for a microcontroller).

   $$R_4 = 51\text{k}\Omega \quad (\text{Standard Value})$$

Design Simulations

DC Temperature Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File, SLVMCS1.

Design Featured Comparator

TLV7041	
Output Type	Open-Drain
V_{cc}	1.6 V to 6.5 V
V_{inCM}	Rail-to-rail
V_{os}	±100 µV
V_{HYS}	7 mV
I_q	335 nA/Ch
t_{pd}	3 µs
#Channels	1
TLV7041	

Design Alternate Comparator

TLV1701	
Output Type	Open-Collector
V_{cc}	2.2 V to 36 V
V_{inCM}	Rail-to-rail
V_{os}	±500 µV
V_{HYS}	N/A
I_q	55 µA/Ch
t_{pd}	560 ns
#Channels	1, 2, and 4
	TLV1701
	TLV1701-Q1

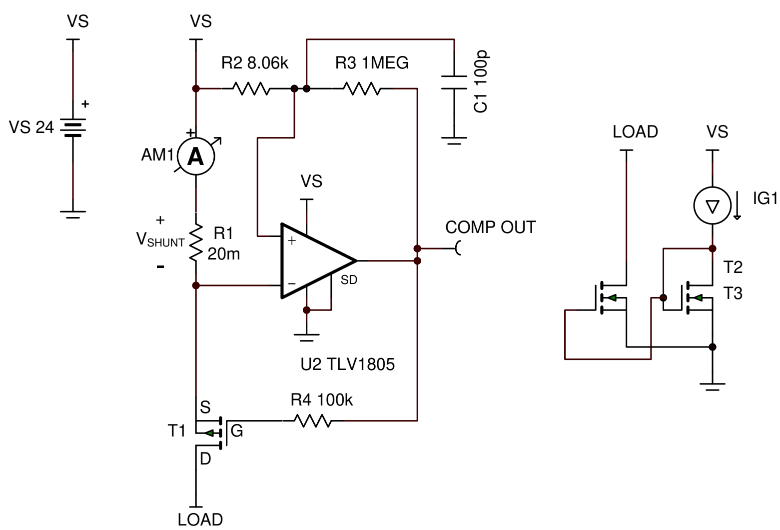
Over-Current Latch Circuit with Comparator Circuit

Design Goals

LOAD CURRENT (I_L)		SYSTEM SUPPLY (V_S)	COMPARATOR OUTPUT STATUS	
Over Current (I_{OC})	Recovery	Typical	Over Current	Normal Operation
10 A	Power Cycle	24 V	> V_S – 0.4 V	< 0.4 V

Design Description

This high-side, current sensing solution uses a high-voltage, rail-to-rail input comparator and a p-channel MOSFET to create an over-current (OC) latch circuit. The OC output signal from the comparator is a logic-high level when the load current exceeds 10 A. The logic-high output level turns the MOSFET switch off and disconnects the load from the system supply (V_S). The comparator output also drives the bottom of the R2/R3 resistor divider which controls the OC threshold level. Under normal operating current levels, the bottom of the resistor divider is held low at ground potential. However, when the OC level is exceeded, the comparator output goes high and elevates the non-inverting input of the comparator to a level equal to V_S. Due to the integrated hysteresis of the comparator, the comparator output will remain high and thus a latched output condition is achieved. Only power-cycling V_S will remove the latched output condition. The shutdown pin could also be utilized to clear the latch if a pull-down resistor is added at the output of the comparator.



Design Notes

1. Select a comparator with rail-to-rail input common mode range to enable high-side current sensing.
2. Select a comparator with a push-pull output stage to efficiently drive the p-channel MOSFET.
3. Select a comparator with low input offset voltage to optimize accuracy.
4. Select a comparator with integrated hysteresis to create a latched-output condition.

Design Steps

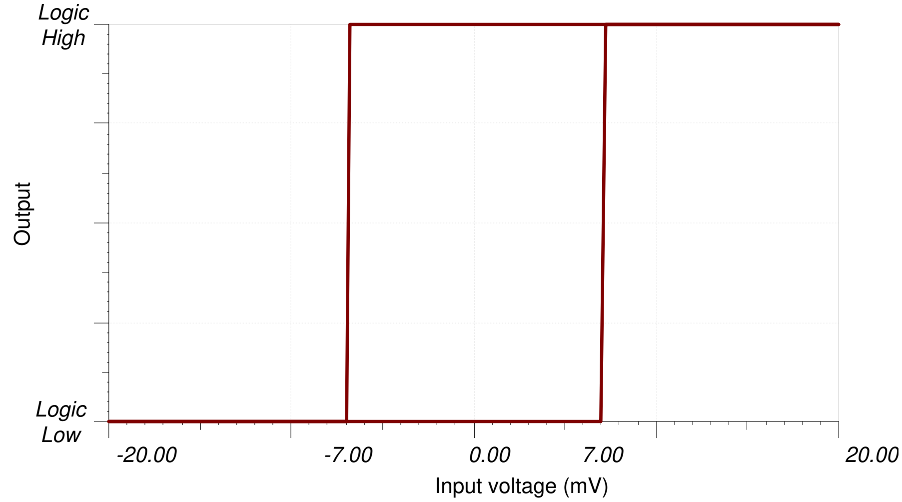
1. Select the value of shunt resistor (R1) so the shunt voltage (V_{SHUNT}) is at least 10x greater than the comparator input offset voltage (V_{IO}). Note that making R1 very large will improve OC detection accuracy but will reduce supply headroom.

$$V_{SHUNT} = (I_{OC} \times R_1) \geq 10 \times V_{IO}$$

$$\text{for} \quad I_{OC} = 10A \quad \& \quad V_{IO} = 6.5mV \quad (\text{max value for TLV1805}), \quad VSHUNT \geq 65mV$$

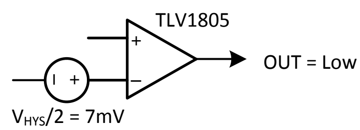
$$\text{set} \quad R_1 = 20m\Omega \quad \text{so that} \quad V_{SHUNT} = 200mV \quad \text{for} \quad I_{OC} = 10A$$

2. Since a comparator with integrated hysteresis is being utilized, the hysteresis needs to be accommodated for in the design. Note how a comparator with integrated hysteresis does not transition from high-to-low and from low-to-high at the same input voltage level. In the case of the TLV1805, the hysteresis is 14 mV and thus the transition thresholds are at ±7 mV respectively.

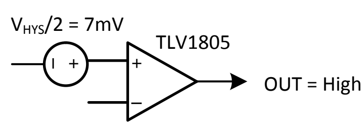


TLV1805 Transition Thresholds

3. A good way to model a comparator internal hysteresis is shown below. One can think of hysteresis as offset that is intentionally added to the design. When the output of the comparator is low, a voltage source equivalent to $V_{HYS}/2$ is added in series with the inverting input pin. However, when the comparator output is high, the hysteresis is modeled as a voltage source of the same value added in series with the non-inverting input.



Comparator Output Low



Comparator Output High

4. Select the values of resistor divider R2 and R3 so the comparator output will transition from low-to-high when V_{SHUNT} exceeds 200 mV. Since the output of the comparator will be *low* prior to an OC condition occuring, use the Comparator Output Low model. The integrated hysteresis effectively shifts the switching threshold from V_S - 200 mV to V_S - 193 mV in the case of the TLV1805 which has an integrated hysteresis value of 14mV. Recall that 1/2 of the hysteresis is applied since hysteresis is defined as the difference between the two switching thresholds of a comparator.

5. The following equation is used to solve for R2 and R3.

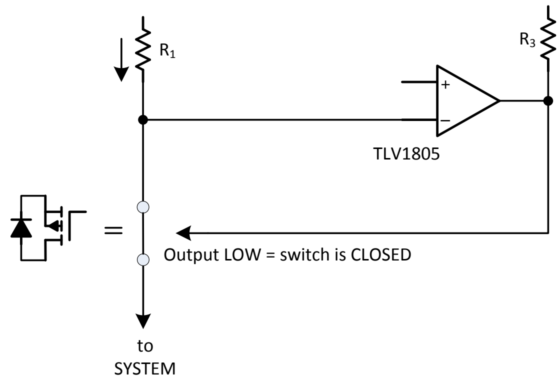
$$R_2 = \frac{(V_{SHUNT} - V_{HYS}/2) \times R3}{V_S - (V_{SHUNT} - V_{HYS}/2)}$$

$$\text{for} \quad V_S = 24V, \quad V_{SHUNT} = 200mV, \quad V_{HYS} = 14mV \quad \text{and} \quad R3 = 1M\Omega$$

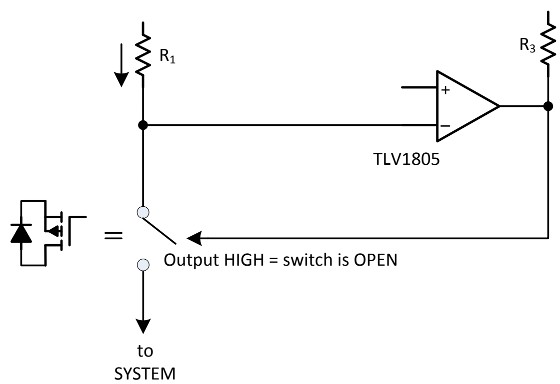
$$R2 = \frac{(200m - 14m/2) \times 1M}{24 - (200m - 14m/2)}$$

$$R2 = 8.107k\Omega \quad (\text{closest} \quad 1\% \quad \text{value} \quad \text{is} \quad 8.06k\Omega)$$

6. Since the goal of this design is to create a circuit that will disconnect the load from the system supply when an OC condition occurs, the output of the comparator is connected to the gate of a p-channel MOSFET switch. Recall that a p-ch MOSFET will look like a closed switch when the source to gate voltage is greater than the voltage threshold (V_{SG} > V_{TH}). Likewise, the MOSFET will look like an open-circuit when V_{SG} < V_{TH} (see figures below).



Normal Operation = Output LOW and CLOSED Switch

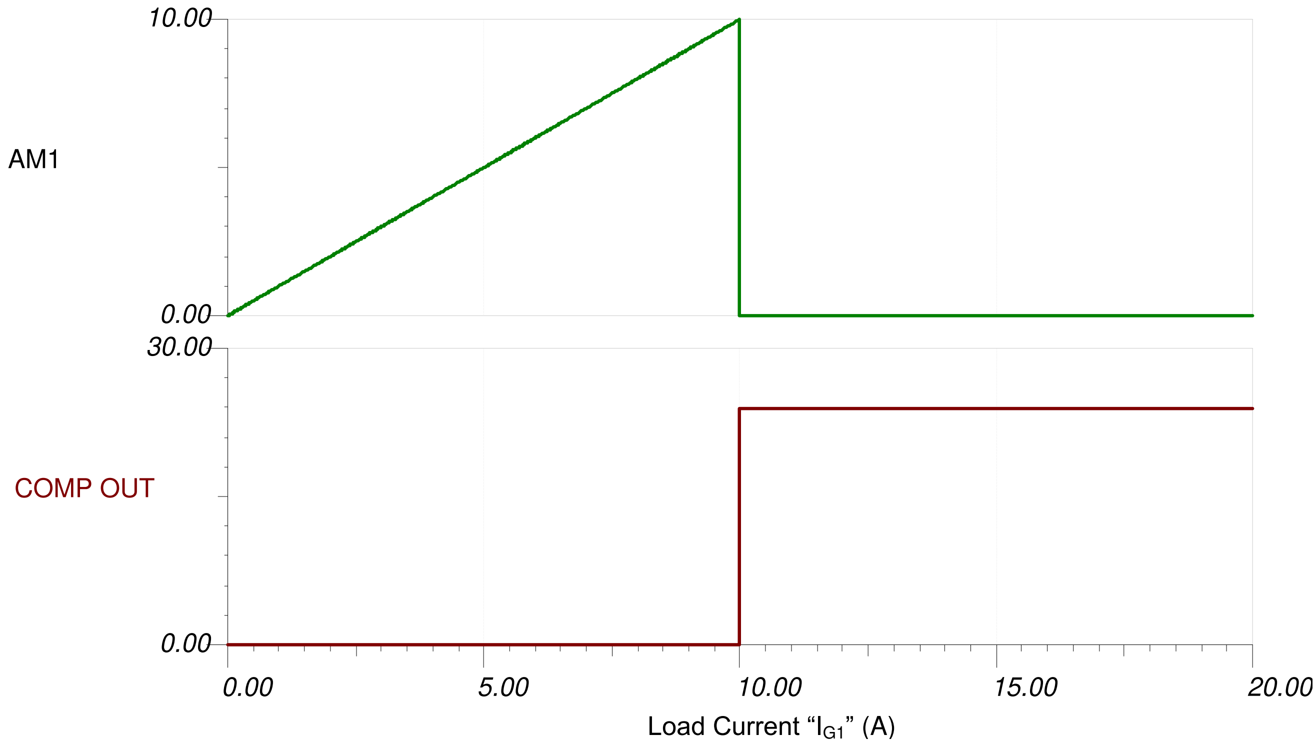


OC Condition = Output HIGH and OPEN Switch

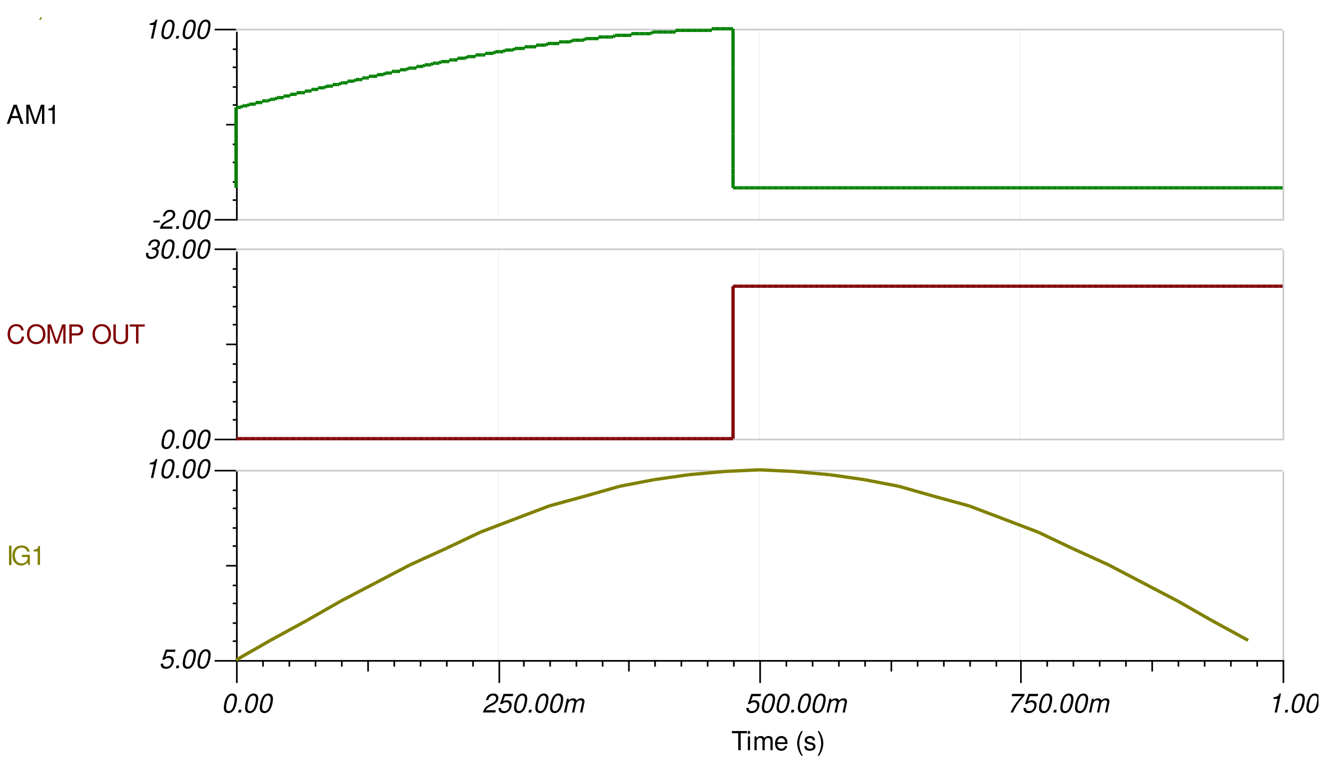
7. Add a series resistor (R4) between the comparator output and the gate of the MOSFET to limit the output current during the transition from low to high. Keeping the current in the mA range is sufficient. Selecting a value of 10 kΩ for R1, the current is limited to 2.4 mA (24 V/10 kΩ).
8. The other goal of this design is to latch the circuit when an OC condition occurs. This is accomplished by providing feedback to the resistor divider network of R2/R3. When the output of the comparator goes high, it turns off the MOSFET and raises the non-inverting node of the comparator to a voltage level of V_S.
9. Note that V_{SHUNT} also reduces to 0 V since the load current is now 0 A. The hysteresis of the comparator that was previously mentioned in Design Step 2 will keep the non-inverting input 7 mV higher than the inverting input. This is what latches the comparator output in a logic high state.
10. Lastly, capacitor C1 is connected from the non-inverting input to ground to make sure that the comparator starts in the logic low output state as V_S rises upon initial power-up.

Design Simulations

DC Simulation Results



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File, SLOM456.

Design Featured Comparator

TLV1805-Q1, TLV1805	
V_S	3.3 V to 40 V
V_{inCM}	Rail-to-rail
V_{OUT}	Push-Pull
V_{OS}	500 µV
I_Q	135 µA
$t_{PD(HL)}$	250 ns
#Channels	1
TLV1805-Q1, TLV1805	

Design Alternate Comparator

	LMC6762	TLV370x-Q1, TLV370x
V_S	2.7 V to 15 V	2.7 V to 16 V
V_{inCM}	Rail-to-rail	Rail-to-rail
V_{OUT}	Push-Pull	Push-Pull
V_{OS}	3 mV	250 µV
I_Q	20 µA	560 nA/Ch
$t_{PD(HL)}$	4 µs	36 µs
#Channels	1	1, 2, and 4
	LMC6762	TLV370x-Q1, TLV370x

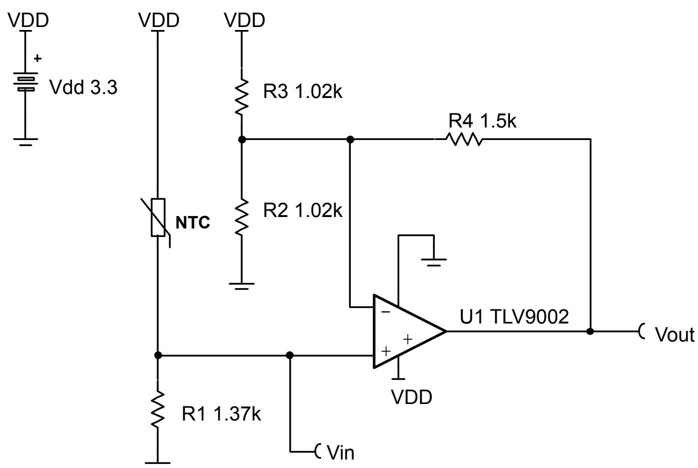
Temperature Sensing with NTC Circuit

Design Goals

Temperature		Output Voltage		Supply	
T_{Min}	T_{Max}	V_{outMin}	V_{outMax}	V_{dd}	V_{ee}
25°C	50°C	0.05 V	3.25 V	3.3 V	0 V

Design Description

This temperature sensing circuit uses a resistor in series with a negative–temperature–coefficient (NTC) thermistor to form a voltage divider, which has the effect of producing an output voltage that is linear over temperature. The circuit uses an op amp in a non–inverting configuration with inverting reference to offset and gain the signal, which helps to utilize the full ADC resolution and increase measurement accuracy.



Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. TLV9002 linear output swing 0.05 V to 3.25 V.
2. The connection, Vin, is a positive temperature coefficient output voltage. To correct a negative temperature coefficient (NTC) output voltage, switch the position of R_1 and the NTC thermistor.
3. Choose R_1 based on the temperature range and the value of NTC.
4. Using high value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit. It is recommended to use resistor values around 10 kΩ or less.
5. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability and help reduce noise.

Design Steps

$$V_{out} = V_{dd} \times \frac{R_1}{R_{NTC} + R_1} \times \frac{(R_2||R_3) + R_4}{(R_2||R_3)} - \left(\frac{R_4}{R_3} \times V_{dd}\right)$$

1. Calculate the value of R_1 to produce a linear output voltage. Use the minimum and maximum values of the NTC to obtain a range of values for R_1.

$$R_{NTCMax} = R_{NTC\ @\ 25C} = 2.252\ \ k\Omega,\ \ R_{NTCMin} = R_{NTC\ @\ 50C} = 819.7\ \ \Omega$$

$$R_1 = \sqrt{R_{NTC\ @\ 25C} \times R_{NTC\ @\ 50C}} = \sqrt{2.252\ \ k\Omega \times 819.7\ \ \Omega} = 1.359\ \ k\Omega \approx 1.37\ \ k\Omega$$

2. Calculate the input voltage range.

$$V_{inMin} = V_{dd} \times \frac{R_1}{R_{NTCMax} + R_1} = 3.3\ \ V \times \frac{1.37\ \ k\Omega}{2.252\ \ k\Omega + 1.37\ \ k\Omega} = 1.248\ \ V$$

$$V_{inMax} = V_{dd} \times \frac{R_1}{R_{NTCMin} + R_1} = 3.3\ \ V \times \frac{1.37\ \ k\Omega}{819.7\ \ \Omega + 1.37\ \ k\Omega} = 2.065\ \ V$$

3. Calculate the gain required to produce the maximum output swing.

$$G_{ideal} = \frac{V_{outMax} - V_{outMin}}{V_{inMax} - V_{inMin}} = \frac{3.25\ \ V - 0.05\ \ V}{2.065\ \ V - 1.248\ \ V} = 3.917\frac{V}{V}$$

4. Solve for the parallel combination of R_2 and R_3 using the ideal gain. Select R_4= 1.5 kΩ (Standard Value).

$$(R_2||R_3)_{ideal} = \frac{R_4}{G_{ideal} - 1} = \frac{1.5\ \ k\Omega}{3.917\ \ V/V - 1} = 514.226\ \ \Omega$$

5. Calculate R_2 and R_3 based off of the transfer function and gain.

$$R_3 = \frac{R_4 \times V_{dd}}{V_{inMax} \times G_{ideal} - V_{outMax}} = \frac{1.5\ \ k\Omega \times 3.3\ \ V}{2.065\ \ V \times 3.917\ \ V/V - 3.25\ \ V} = 1023.02\ \ \Omega$$

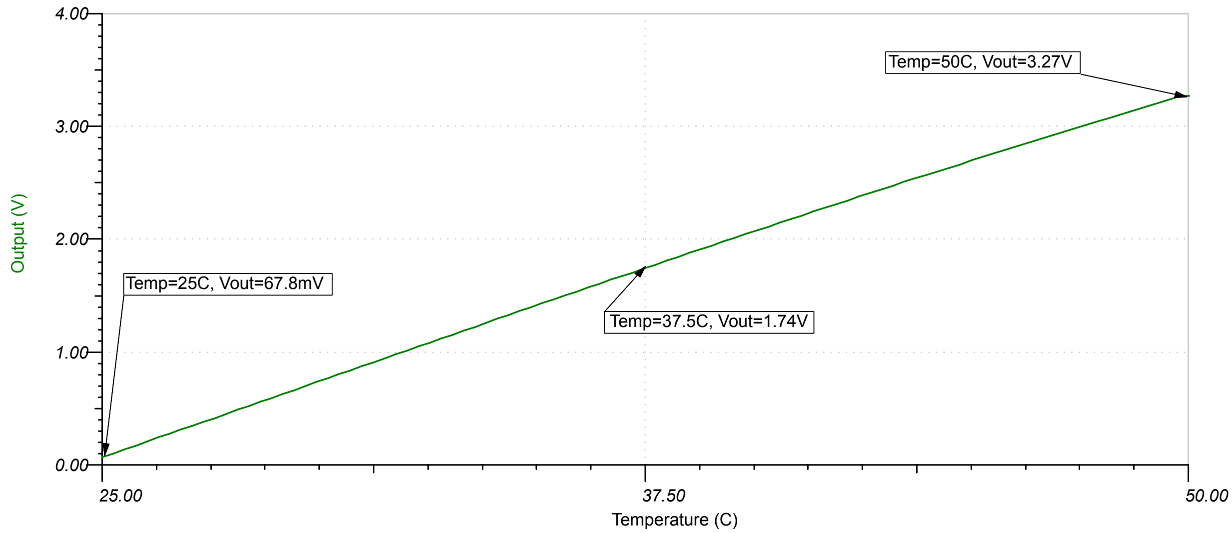
$$R_2 = \frac{(R_2||R_3)_{ideal} \times R_3}{R_3 - (R_2||R_3)_{ideal}} = \frac{514.226\ \ \Omega\ \ \times 1023.02\ \ \Omega}{1023.02\ \ \Omega - 514.226\ \ \Omega} = 1033.941\ \ \Omega$$

6. Calculate the actual gain with the standard values of R_2 (1.02 kΩ) and R_3 (1.02 kΩ).

$$G_{actual} = \frac{(R_2||R_3) + R_4}{(R_2||R_3)} = \frac{510\ \ \Omega\ \ + 1.5\ \ k\Omega}{510\ \ \Omega} = \ \ 3.941\frac{V}{V}$$

Design Simulations

DC Transfer Results



Design References

1. See the Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation file: SBOMAV6
3. TI Precision Labs

Design Featured Op Amp

TLV9002	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	1.5mV
I_q	0.06mA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1, 2, 4
http://www.ti.com/product/TLV9002	

Design Alternate Op Amp

OPA333	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	2µV
I_q	17µA
I_b	70pA
UGBW	350kHz
SR	0.16V/µs
#Channels	1, 2, 4
http://www.ti.com/product/OPA333	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Photodiode Amplifier Circuit

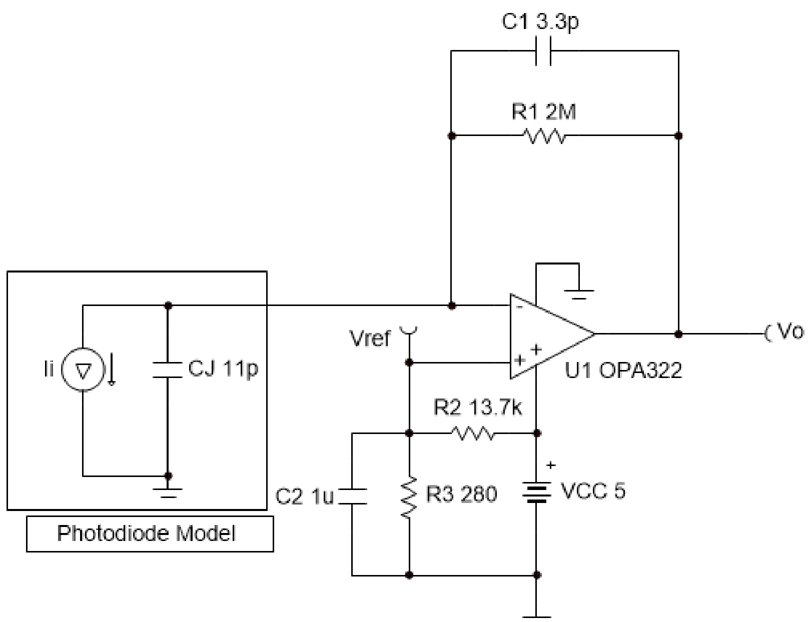
TEXAS INSTRUMENTS

Design Goals

Input		Output		BW	Supply		
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}	V_{ref}
0 A	2.4 µA	100 mV	4.9 V	20 kHz	5 V	0 V	0.1 V

Design Description

This circuit consists of an op amp configured as a transimpedance amplifier for amplifying the light-dependent current of a photodiode.



Design Notes

1. A bias voltage (V_{ref}) prevents the output from saturating at the negative power supply rail when the input current is 0 A.
2. Use a JFET or CMOS input op amp with low bias current to reduce DC errors.
3. Set output range based on linear output swing (see A_{ol} specification).

Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{4.9V - 0.1V}{2.4\mu A} = 2M\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \le \frac{1}{2 \times \pi \times R_1 \times f_p}$$

$$C_1 \le \frac{1}{2 \times \pi \times 2M\Omega \times 20kHz} \le 3.97pF \approx 3.3pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

$$GBW > \frac{C_i + C_1}{2 \times \pi \times R_1 \times {C_1}^2} > \frac{20pF + 3.3pF}{2 \times \pi \times 2M\Omega \times (3.3pF)^2} > 170kHz$$

$$\text{where } C_i = C_j + C_d + C_{cm} = 11pF + 5pF + 4pF = 20pF \text{ given}$$

- C_j: Junction capacitance of photodiode
- C_d: Differential input capacitance of the amplifier
- C_{cm}: Common-mode input capacitance of the inverting input

4. Calculate the bias network for a 0.1 V bias voltage.

$$R_2 = \frac{V_{cc} - V_{ref}}{V_{ref}} \times R_3$$

$$R_2 = \frac{5V - 0.1V}{0.1V} \times R_3$$

$$R_2 = 49 \times R_3$$

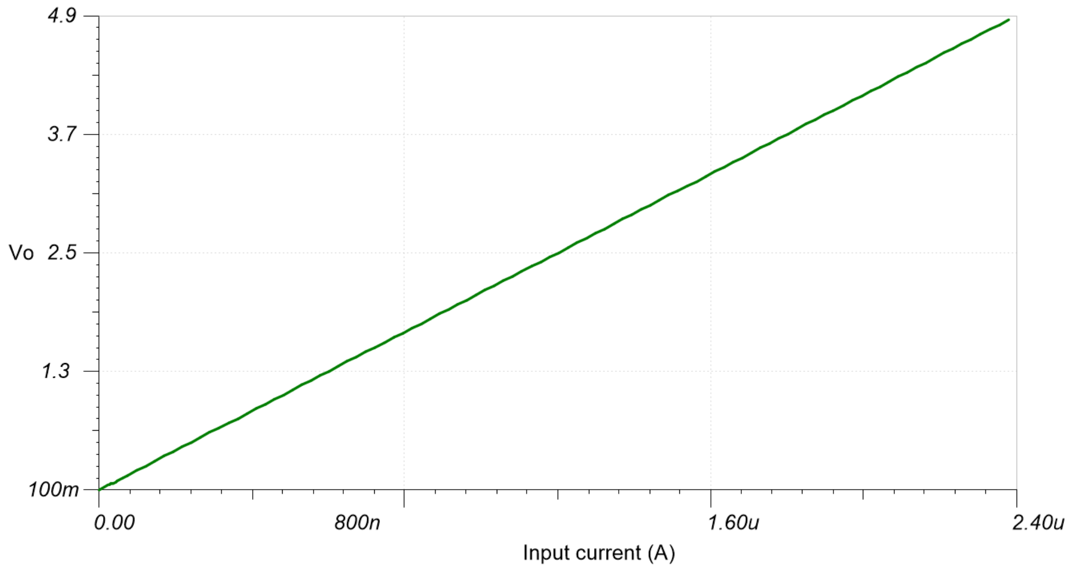
Closest 1% resistor values that yield this relationship are
$R_2 = 13.7k\Omega$ and $R_3 = 280\Omega$

5. Select C_2 to be 1 µF to filter the V_{ref} voltage. The resulting cutoff frequency is:

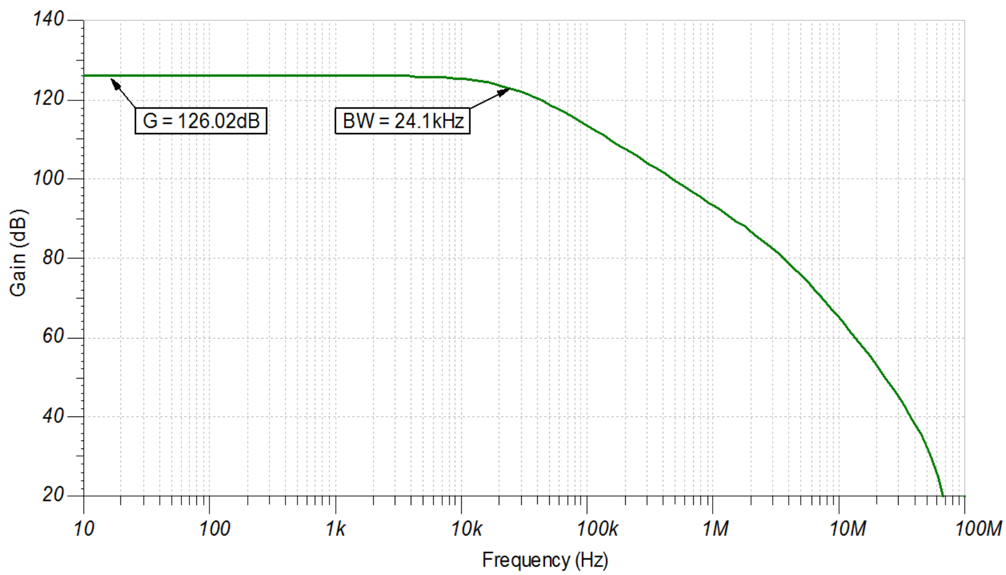
$$f_p = \frac{1}{2 \times \pi \times C_2 \times (R_2 \parallel R_3)} = \frac{1}{2 \times \pi \times 1\ \ \mu F \times (13.7k \parallel 280)} = 580Hz$$

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See the circuit SPICE simulation file SBOC517.

See TIPD176.

Design Featured Op Amp

OPA322	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	0.5 mV
I_q	1.6 mA/Ch
I_b	0.2 pA
UGBW	20 MHz
SR	10 V/µs
#Channels	1, 2, and 4
OPA322	

Design Alternate Op Amp

LMP7721	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	V_{ee} to (V_{cc} –1 V)
V_{out}	Rail–to–rail
V_{os}	26 µV
I_q	1.3 mA/Ch
I_b	3 fA
UGBW	17 MHz
SR	10.43 V/µs
#Channels	1
LMP7721	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from February 1, 2018 to February 4, 2019 **Page**

Analog Engineer's Circuit

Single-Supply Strain Gauge Bridge Amplifier Circuit

Amplifiers

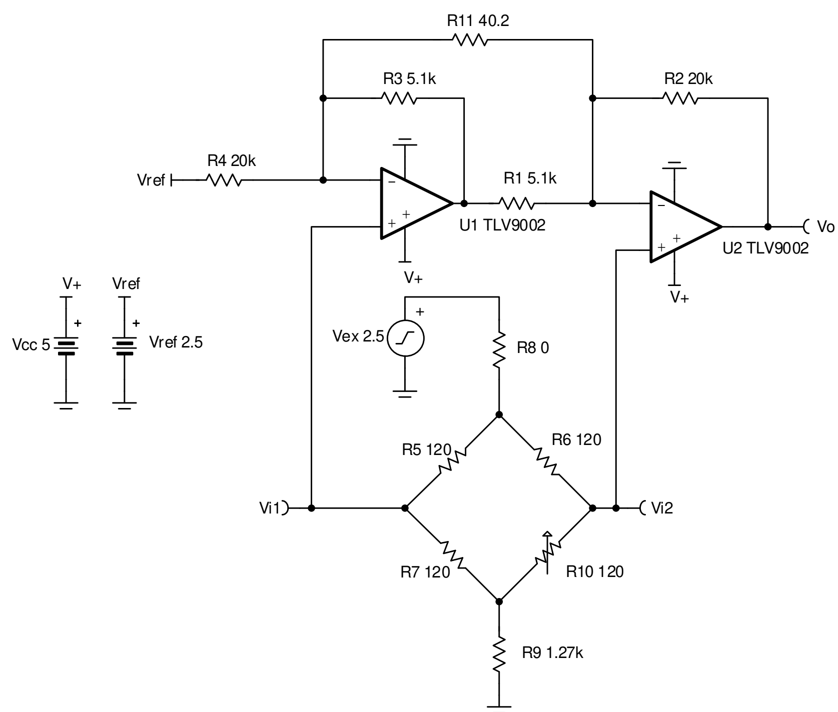
Design Goals

Input $V_{iDiff}(V_{i2} – V_{i1})$		Output		Supply		
V_{iDiff_Min}	V_{iDiff_Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–2.22 mV	2.27 mV	225 mV	4.72 V	5 V	0 V	2.5 V

Strain Gauge Resistance Variation (R_{10})	V_{cm}	Gain
115 Ω – 125 Ω	2.39 V	1001 V/V

Design Description

A strain gauge is a sensor whose resistance varies with applied force. The change in resistance is directly proportional to how much strain the sensor is experiencing due to the force applied. To measure the variation in resistance, the strain gauge is placed in a bridge configuration. This design uses a two op amp instrumentation circuit to amplify a differential signal created by the change in resistance of a strain gauge. By varying R_{10}, a small differential voltage is created at the output of the Wheatstone bridge which is fed to the two op amp instrumentation amplifier input. Linear operation of an instrumentation amplifier depends upon the linear operation of the primary building block: op amps. An op amp operates linearly when the input and output signals are within the input common-mode and output-swing ranges of the device, respectively. The supply voltages used to power the op amps define these ranges.



Design Notes

1. Resistors R_5, R_6, and R_7 of the Wheatstone bridge must match the stain gauge nominal resistance and must be equal to avoid creating a bridge offset voltage.
2. Low tolerance resistors must be used to minimize the offset and gain errors due to the bridge resistors.
3. V_{ex} sets the excitation voltage of the bridge and the common-mode voltage V_{cm}.
4. V_{ref} biases the output voltage of the instrumentation amplifier to mid-supply to allow differential measurements in the positive and negative directions.
5. R_{11} sets the gain of the instrumentation amplifier circuit.
6. R_8 and R_9 set the common-mode voltage of the instrumentation amplifier and limits the current through the bridge. This current determines the differential signal produced by the bridge. However, there are limitations on the current through the bridge due to self-heating effects of the bridge resistors and strain gauge.
7. Make sure that $R_1 = R_3$ and $R_2 = R_4$ and that ratios of R_2/R_1 and R_4/R_3 are matched to set the V_{ref} gain to 1 V/V and maintain high DC CMRR of the instrumentation amplifier.
8. Linear operation is contingent upon the input common-mode and the output swing ranges of the op amps used. The linear output swing ranges are specified under the A_{ol} test conditions in the op amps data sheets.
9. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.

Design Steps

1. Select R_5, R_6 and R_7 to match the stain gauge nominal resistance

$$R_{gauge} = R_5 = R_6 = R_7 = 120\ \Omega$$

2. Choose R_9 to set the common mode voltage of the instrumentation amplifier at 2.39 V

$$V_{cm} = \frac{\frac{R_{bridge}}{2} + R_9}{R_{bridge} + R_9} \times V_{ex}$$

$$V_{cm} = \frac{\frac{120\ \Omega}{2} + R_9}{120\ \Omega + R_9} \times 2.5\ V = 2.39\ V$$

$$\frac{\frac{120\ \Omega}{2} + R_9}{120\ \Omega + R_9} = \frac{2.39\ V}{2.5\ V} = 0.96$$

$$0.04\ R_9 = 49.7 \rightarrow R_9 = \frac{49.7}{0.04} = 1.24\ k\Omega = 1.27\ k\Omega\ \left(\text{Standard value}\right)$$

3. Calculate the gain required to produce the desired output voltage swing

$$G = \frac{V_{oMax} - V_{oMin}}{V_{iDiff\_Min} - V_{iDiff\_Min}} = \frac{4.72\ V - 0.225\ V}{0.00222\ V - (-0.00227\ V)} = 1001\ \frac{V}{V}$$

4. Select R_1, R_2, R_3, and R_4. To set the V_{ref} gain at 1 V/V and avoid degrading the instrumentation amplifier's CMRR, R_1 must equal R_3 and R_2 must equal R_4.

$$\text{Choose } R_1 = R_3 = 5.1\ k\Omega \text{ and } R_3 = R_4 = 20\ k\Omega\ (\text{Standard value})$$

5. Calculate R_{11} to meet the required gain

$$G = 1 + \frac{R_4}{R_3} + \frac{2 \times R_2}{R_{11}} = 1001\ \frac{V}{V}$$

$$G = 1 + \frac{20\ k\Omega}{5.1\ k\Omega} + \frac{2 \times R_2}{R_{11}} = 1001\ \frac{V}{V} \rightarrow 4.92 + \frac{40\ k\Omega}{R_{11}} = 1001\ \frac{V}{V} \rightarrow \frac{40\ k\Omega}{R_{11}} = 996.1 \rightarrow R_{11} = \frac{40\ k\Omega}{996.1} = 40.15\ \Omega \rightarrow R_{11} = 40.2\ \Omega\ (\text{Standard value})$$

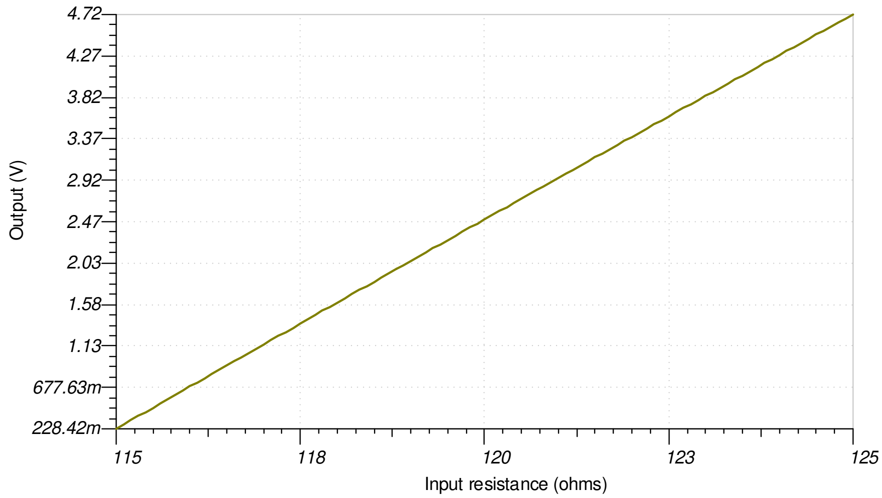
6. Calculate the current through the bridge

$$I_{bridge} = \frac{V_{ex}}{R_8 + R_9 + R_{bridge}} = \frac{2.5\ V}{0\ \Omega + 1.27\ k\Omega + 120\ \Omega}$$

$$I_{bridge} = \frac{2.5\ V}{1.27\ k\Omega + 120\ \Omega} \rightarrow I_{bridge} = 1.80\ mA$$

Design Simulations

DC Simulation Results



References

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOMAU4
3. TI Precision Designs TIPD170
4. TI Precision Labs
5. V_{CM} vs. V_{OUT} plots for instrumentation amplifiers with two op amps

Design Featured Op Amp

TLV9002	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-Rail
V_{os}	0.4 mV
I_q	0.06 mA
I_b	5 pA
UGBW	1 MHz
SR	2 V/µs
#Channels	1, 2, and 4
TLV9002	

Design Alternate Op Amp

OPA376	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	(V_{ee} – 0.1 V) to (V_{cc} – 1.3 V)
V_{out}	Rail-to-Rail
V_{os}	0.005 mV
I_q	0.76 mA
I_b	0.2 pA
UGBW	5.5 MHz
SR	2 V/µs
#Channels	1, 2, and 4
OPA376	

Temperature Sensing with PTC Circuit

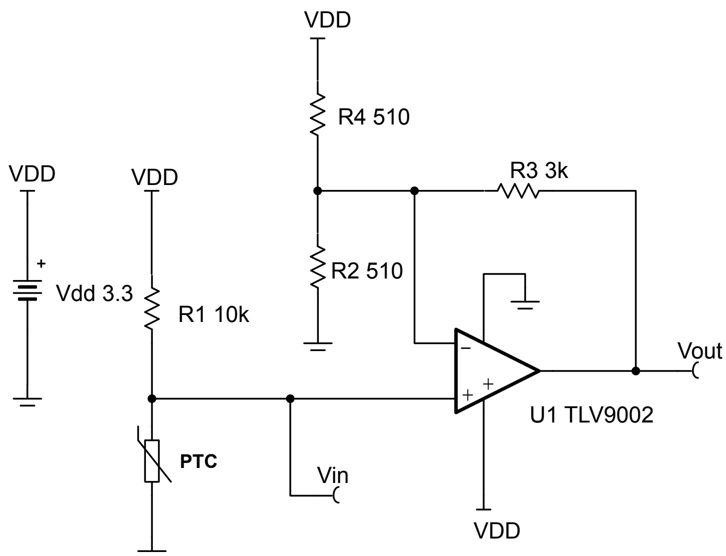
TEXAS INSTRUMENTS

Design Goals

Temperature		Output voltage		Supply	
T_{Min}	T_{Max}	V_{outMin}	V_{outMax}	V_{dd}	V_{ee}
0 °C	50 °C	0.05V	3.25V	3.3V	0V

Design Description

This temperature sensing circuit uses a resistor in series with a positive–temperature–coefficient (PTC) thermistor to form a voltage–divider, which has the effect of producing an output voltage that is linear over temperature. The circuit uses an op amp in a non–inverting configuration with inverting reference to offset and amplify the signal, which helps to utilize the full ADC resolution and increase measurement accuracy.



Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. TLV9002 linear output swing 0.05 V to 3.25 V.
2. The connection, V_{in}, is a positive temperature coefficient output voltage. To correct a negative–temperature–coefficient (NTC) output voltage, switch the position of R_1 and PTC thermistor.
3. Choose R_1 based on the temperature range and the PTC's value.
4. Using high–value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit. It is recommended to use resistor values around 10kΩ or less.
5. A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability and help reduce noise.

Design Steps

$$V_{out} = V_{dd} \times \frac{R_{PTC}}{R_{PTC} + R_1} \times \frac{(R_2||R_4) + R_3}{(R_2||R_4)} - \left(\frac{R_3}{R_4} \times V_{dd}\right)$$

1. Calculate the value of R_1 to produce a linear output voltage. Use the minimum and maximum values of the PTC to obtain a range of values for R_1.

$$R_{PTCMax} = R_{PTC\ @\ 50C} = 11.611\ k\Omega,\quad R_{PTCMin} = R_{PTC\ @\ 0C} = 8.525\ k\Omega$$

$$R_1 = \sqrt{R_{PTC\ @\ 0C} \times R_{PTC\ @\ 50C}} = \sqrt{8.525\ k\Omega \times 11.611\ k\Omega} = 9.95\ k\Omega \approx 10\ k\Omega$$

2. Calculate the input voltage range.

$$V_{inMin} = V_{dd} \times \frac{R_{PTCMin}}{R_{PTCMin} + R_1} = 3.3\ V \times \frac{8.525\ k\Omega}{8.525\ k\Omega + 10\ k\Omega} = 1.519\ V$$

$$V_{inMax} = V_{dd} \times \frac{R_{PTCMax}}{R_{PTCMax} + R_1} = 3.3\ V \times \frac{11.611\ k\Omega}{11.611\ k\Omega + 10\ k\Omega} = 1.773\ V$$

3. Calculate the gain required to produce the maximum output swing.

$$G_{ideal} = \frac{V_{outMax} - V_{outMin}}{V_{inMax} - V_{inMin}} = \frac{3.25\ V - 0.05\ V}{1.773\ V - 1.519\ V} = 12.598\frac{V}{V}$$

4. Solve for the parallel combination of R_2 and R_4 using the ideal gain. Select R_3= 3 kΩ (Standard Value).

$$(R_2||R_4)_{ideal} = \frac{R_3}{G_{ideal} - 1} = \frac{3\ k\Omega}{12.598\ {}^{V}\!/_{V} - 1} = 258.665\ \Omega$$

5. Calculate R_2 and R_4 based off of the transfer function and gain.

$$R_4 = \frac{R_3 \times V_{dd}}{V_{inMax} \times G_{ideal} - V_{outMax}} = \frac{3\ k\Omega \times 3.3\ V}{1.773\ V \times 12.598\ {}^{V}\!/_{V} - 3.25\ V} = 518.698\ \Omega$$

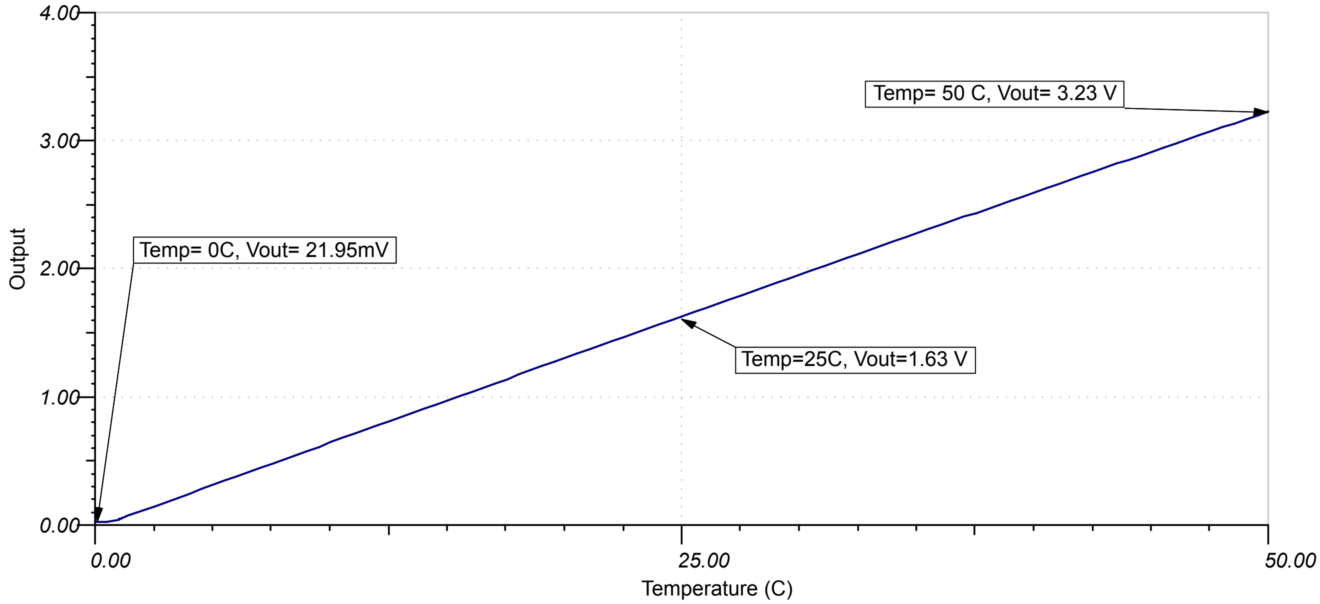
$$R_2 = \frac{(R_2||R_4)_{ideal} \times R_4}{R_4 - (R_2||R_4)_{ideal}} = \frac{258.665\ \Omega \times 518.698\ \Omega}{518.698\ \Omega - 258.665\ \Omega} = 515.969\ \Omega$$

6. Calculate the actual gain with the standard values of R_2 (510 Ω) and R_4 (510 Ω).

$$G_{actual} = \frac{(R_2||R_4) + R_3}{(R_2||R_4)} = \frac{255\ \Omega + 3\ k\Omega}{255\ \Omega} = 12.764\frac{V}{V}$$

Design Simulations

DC Transfer Results



Design References

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOMAV5
3. TI Precision Labs

Design Featured Op Amp

TLV9002	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	1.5mV
I_q	0.06mA
I_b	5pA
UGBW	1MHz
SR	2V/µs
#Channels	1, 2, 4
http://www.ti.com/product/TLV9002	

Design Alternate Op Amp

OPA333	
V_{cc}	1.8 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	2µV
I_q	17µA
I_b	70pA
UGBW	350kHz
SR	0.16V/µs
#Channels	1, 2, 4
http://www.ti.com/product/OPA333	

Design Featured Thermistor

TMP61	
V_{cc}	Up to 5.5 V
R_{25}	10kΩ
R_{TOL}	1%
I_{SNS}	400 µA
Operating Temperature Range	-40°C to 125°C
http://www.ti.com/product/TMP61	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May 2019) to Revision B (May 2021) **Page**

- Updated VREF with voltage divider, changed schematic, and equations..........1

Changes from Revision * (December 2018) to Revision A (May 2019) **Page**

- Added *Design Featured Thermistor* table..........4

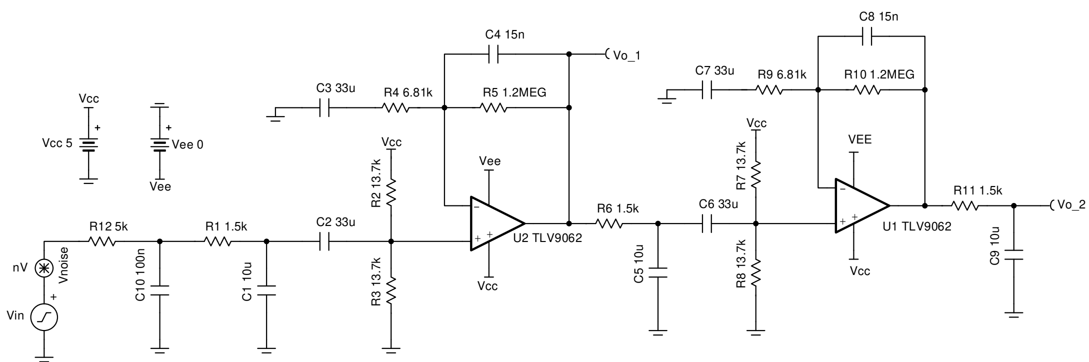
Low-Noise and Long-Range PIR Sensor Conditioner Circuit

Design Goals

AC Gain	Filter Cut Off Frequency		Supply	
	f_L	f_H	V_{cc}	V_{ee}
90 dB	0.7 Hz	10 Hz	5 V	0 V

Design Description

This two stage amplifier design amplifies and filters the signal from a passive infrared (PIR) sensor. The circuit includes multiple low–pass and high–pass filters to reduce noise at the output of the circuit to be able to detect motion at long distances and reduce false triggers. This circuit can be followed by a window comparator circuit to create a digital output or connect directly to an analog–to–digital converter (ADC) input.



Design Notes

1. The common mode voltage and output bias voltage are set using the resistor dividers between R_2 and R_3 (and R_7 and R_8).
2. Two or more amplifier stages must be used to allow for sufficient loop gain.
3. Additional low–pass and high–pass filters can be added to further reduce noise.
4. Capacitors C_4 and C_8 filter noise by decreasing the bandwidth of the circuit and help stabilize the amplifiers.
5. RC filters on the output of the amplifiers (for example, R_6 and C_5) are required to reduce the total integrated noise of the amplifier.
6. The maximum gain of the circuit can be affected by the cutoff frequencies of the filters. The cutoff frequencies may need to be adjusted to achieve the desired gain.

Design Steps

1. Choose large–valued capacitors C_1, C_5, and C_9 for the low–pass filters. These capacitors should be selected first since large–valued capacitors have limited standard values to select from compared to standard resistor values.

$$C_1 = C_5 = C_9 = 10\mu F$$

2. Calculate resistor values for R_1, R_6, and R_{11} to form the low–pass filters.

$$R_1 = R_6 = R_{11} = \frac{1}{2\pi \times f_H \times C_1} = \frac{1}{2\pi \times 10Hz \times 10\mu F} = 1.592k\Omega$$

$$\text{Choose} \quad R_1 = R_6 = R_{11} = 1.5k\Omega \quad \left(\text{Standard} \quad \text{value}\right)$$

3. Select capacitor values for C_2, C_3, C_6, and C_7 for the high–pass filters.

$$C_2 = C_3 = C_6 = C_7 = 33\mu F$$

4. Calculate the resistor values for R_4 and R_9 for the high–pass filters.

$$R_4 = R_9 = \frac{1}{2\pi \times f_L \times C_2} = \frac{1}{2\pi \times 0.7Hz \times 33\mu F} = 6.89k\Omega$$

$$\text{Choose} \quad R_4 = R_9 = 6.81k\Omega \quad \left(\text{Standard} \quad \text{value}\right)$$

5. Set the common–mode voltage of the amplifier to mid–supply using a voltage divider. The equivalent resistance of the voltage divider should be equal to R_4 to properly set the corner frequency of the high–pass filter.

$$R_2 = R_3 = R_7 = R_8 = 2 \times R_4 = 2 \times 6.81k\Omega = 13.62k\Omega$$
$$\text{Choose} \quad R_2 = R_3 = R_7 = R_8 = 13.7k\Omega \quad (\text{Standard} \quad \text{value})$$

6. Calculate the gain required by each gain stage to achieve the total gain requirement. Distribute the total gain target of the circuit evenly between both gain stages.

$$\text{Gain} = \frac{90dB}{2} = 45dB = 177.828\frac{V}{V}$$

7. Calculate R_5 to set the gain of the first stage.

$$R_5 = (\text{Gain} - 1) \times R_4 = \left(177.828\frac{V}{V} - 1\right) \times 6.81k\Omega = 1.204M\Omega$$
$$\text{Choose} \quad 1.2M\Omega$$

8. Calculate C_4 to set the low–pass filter cut off frequency.

$$C_4 = \frac{1}{2\pi \times R_5 \times f_H} = \frac{1}{2\pi \times 1.2M\Omega \times 10Hz} = 13.263nF$$
$$\text{Choose} \quad C_4 = 15nF$$

9. Since the gain and cut off frequency of the first gain stage is equal to the second gain stage, set all component values of both stages equal to each other.

$$R_1 = R_6 = 1.5k\Omega$$

$$R_7 = R_8 = 13.7k\Omega$$

$$R_9 = R_4 = 6.81k\Omega$$

$$R_{10} = R_5 = 1.2M\Omega$$

$$C_8 = C_4 = 15nF$$

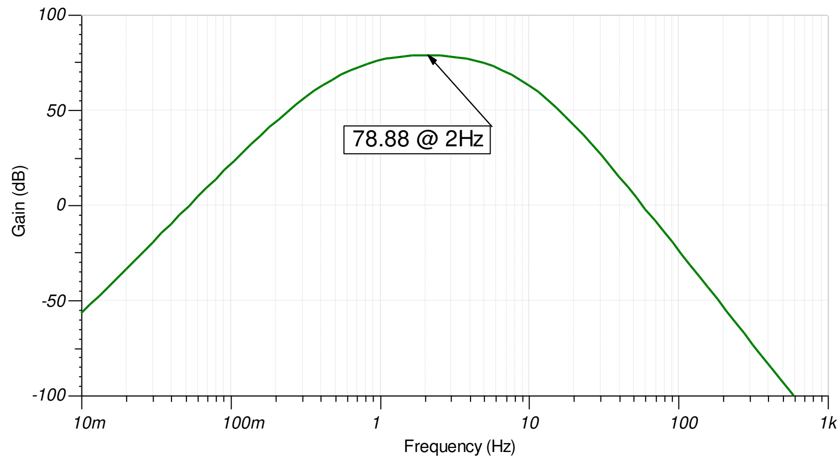
10. Calculate R_{11} to set the cut off frequency of the low–pass filter at the output of the circuit.

$$R_{11} = \frac{1}{2\pi \times C_9 \times f_H} = \frac{1}{2\pi \times 10\mu F \times 10Hz} = 1.592k\Omega$$

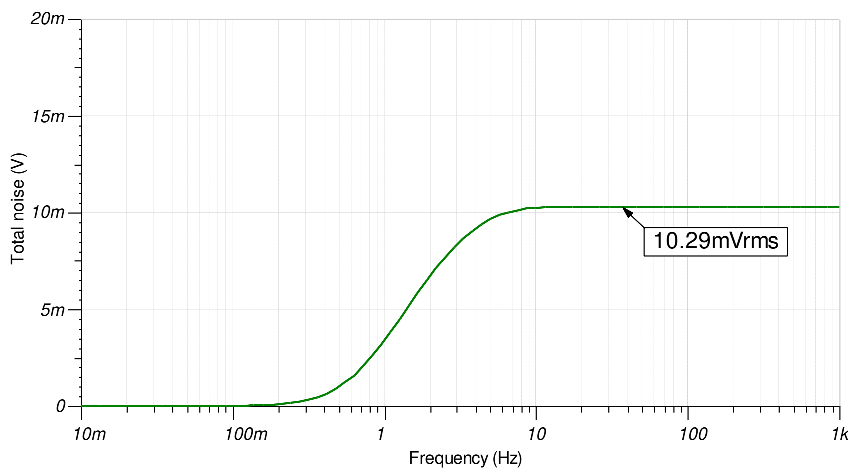
$$\text{Choose} \quad R_{11} = 1.5k\Omega$$

Design Simulations

AC Simulation Results



Noise Simulation Results



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOC524
3. TI Precision Labs

Design Featured Op Amp

TLV9062	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	0.3 mV
I_q	538 µA
I_b	0.5 pA
UGBW	10 MHz
SR	6.5 V/µs
#Channels	1, 2, and 4
www.ti.com/product/tlv9062	

Design Alternate Op Amp

OPA376	
V_{ss}	2.2 V to 5.5 V
V_{inCM}	V_{ee} to V_{cc}–1.3 V
V_{out}	Rail–to–rail
V_{os}	5 µV
I_q	760 µA/Ch
I_b	0.2 pA
UGBW	5.5 MHz
SR	2 V/µs
#Channels	1, 2, and 4
http://www.ti.com/product/opa376	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from December 30, 2018 to February 29, 2020 **Page**

- Changed the equations in the following steps of the *Design Steps* section: 2, 4, 8, 9, and 10 1

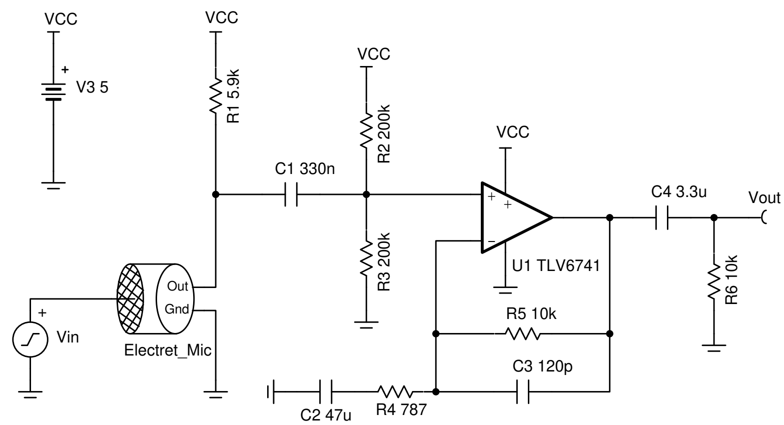
Application Note
Non-inverting microphone pre-amplifier circuit

Design Goals

Input Pressure (Max)	Output Voltage (Max)	Supply		Frequency Response Deviation	
		V_{cc}	V_{ee}	@20Hz	@20kHz
100dB SPL (2 Pa)	$1.228V_{rms}$	5V	0V	–0.5dB	–0.1dB

Design Description

This circuit uses a non–inverting amplifier circuit configuration to amplify the microphone output signal. This circuit has very good magnitude flatness and exhibits minor frequency response deviations over the audio frequency range. The circuit is designed to be operated from a single 5V supply.



Design Notes

1. Operate within the op amp linear output operating range, which is usually specified under the A_{OL} test conditions.
2. Use low–K capacitors (tantalum, C0G, and so forth) and thin film resistors help to decrease distortion.
3. Use a battery to power this circuit to eliminate distortion caused by switching power supplies.
4. Use low value resistors and low noise op amps for low noise designs.
5. The common mode voltage is equal to the DC bias voltage set using the resistor divider plus any variation caused by the microphone output voltage. For op amps with a complementary pair input stage it is recommended to keep the common mode voltage away from the cross over region to eliminate the possibility of cross over distortion.
6. Resistor R_1 is used to bias the microphone internal JFET transistor to achieve the bias current specified by the microphone.
7. The equivalent input resistance is determined by R_1, R_2, R_3. Use large value resistors for R_2 and R_3 to increase the input resistance.
8. The voltage connected to R_1 to bias the microphone does not have to be the same as the op amp supply voltage. Using a higher voltage supply for the microphone bias allows for a lower bias resistor value.

Design Steps

This design procedure uses the microphone specifications provided in the following table.

Microphone Parameter	Value
Sensitivity @ 94dB SPL (1 Pa)	–35 ± 4 dBV
Current Consumption (Max)	0.5mA
Impedance	2.2kΩ
Standard Operating Voltage	2Vdc

1. Convert the sensitivity to volts per Pascal.

$$10^{\frac{-35\text{dB}}{20}} = 17.78\frac{\text{mV}}{\text{Pa}}$$

2. Convert volts per Pascal to current per Pascal.

$$\frac{17.78\frac{\text{mV}}{\text{Pa}}}{2.2\text{k}\Omega} = 8.083\frac{\mu\text{A}}{\text{Pa}}$$

3. Max output current occurs at max pressure 2Pa.

$$I_{Max} = 2\text{Pa} \times 8.083\frac{\mu\text{A}}{\text{Pa}} = 16.166\mu\text{A}$$

4. Calculate bias resistor. In the following equation, Vmic is microphone standard operating voltage.

$$R_1 = \frac{V_{cc} - V_{mic}}{I_S} = \frac{5\text{V-}2\text{V}}{0.5\text{mA}} = 6\text{k}\Omega \approx 5.9\text{k}\Omega\ (\text{Standard Value})$$

5. Set the amplifier input common mode voltage to mid–supply voltage. The equivalent resistance of R_2 in parallel with R_3 should be 10 times larger than R1 so that a majority of the microphone current flows through R_1.

$$R_{eq} = R2||R3 > 10 \times R1 = 100\text{k}\Omega$$
$$\text{Choose } R_2 = R_3 = 200\text{k}\Omega$$

6. Calculate the maximum input voltage.

$$R_{in} = R1||R_{eq} = 5.9\text{k}\Omega||100\text{k}\Omega = 5.571\text{k}\Omega$$
$$V_{in} = I_{max} \times R_{in} = 16.166\text{uA} \times 5.571\text{k}\Omega = 90.067\text{mV}$$

7. Calculate gain required to produce the largest output voltage swing.

$$\text{Gain} = \frac{V_{outmax}}{V_{in}} = \frac{1.228\text{V}}{90.067\text{mV}} = 13.634\frac{\text{V}}{\text{V}}$$

8. Calculate R_4 to set the gain calculated in step 7. Select feedback resistor R_5 as 10kΩ.

$$R_4 = \frac{R_5}{\text{Gain-1}} = \frac{10\text{k}\Omega}{13.634\text{-}1} = 791\Omega \approx 787\Omega\ (\text{Standard Values})$$

The final gain of this circuit is:

$$\text{Gain} = 20\log\left(\frac{\text{Vout}}{\text{Vin}}\right) = 20\log\left(\frac{16.166\text{uA} \times 5.571\text{k}\Omega \times \left(1+\frac{10\text{k}\Omega}{787\Omega}\right)}{2\text{V}}\right) = -4.191\text{dB}$$

9. Calculate the corner frequency at low frequency according to the allowed deviation at 20 Hz. In the following equation, G_pole1 is the gain contributed by each pole at frequency “f”. Note that you divide by three because there are three poles.

$$f_c = f\sqrt{\left(\frac{1}{\text{G\_pole1}}\right)^2 - 1} = 20\text{Hz}\sqrt{\left(\frac{1}{10^{\frac{-0.5/3}{20}}}\right)^2 - 1} = 3.956\text{Hz}$$

10. Calculate C_1 based on the cut off frequency calculated in step 9.

$$C_1 = \frac{1}{2\pi \times Req \times f_c} = \frac{1}{2\pi \times 100k\Omega \times 3.956Hz} = 0.402\mu F \approx 0.33\mu F \text{ (Standard Value)}$$

11. Calculate C_2 based on the cut off frequency calculated in step 9.

$$C_2 = \frac{1}{2\pi \times R4 \times f_c} = \frac{1}{2\pi \times 787\Omega \times 3.956Hz} = 51.121\mu F \approx 47\mu F \text{ (Standard Value)}$$

12. Calculate the high frequency pole according to the allowed deviation at 20 kHz. In the following equation, G_pole2 is the gain contributed by each pole at frequency "f".

$$f_p = \frac{f}{\sqrt{\left(\frac{1}{G\_pole2}\right)^2 - 1}} = \frac{20kHz}{\sqrt{\left(\frac{1}{10^{\frac{-0.1}{20}}}\right)^2 - 1}} = 131.044kHz$$

13. Calculate C3 to set the cut off frequency calculated in step 12.

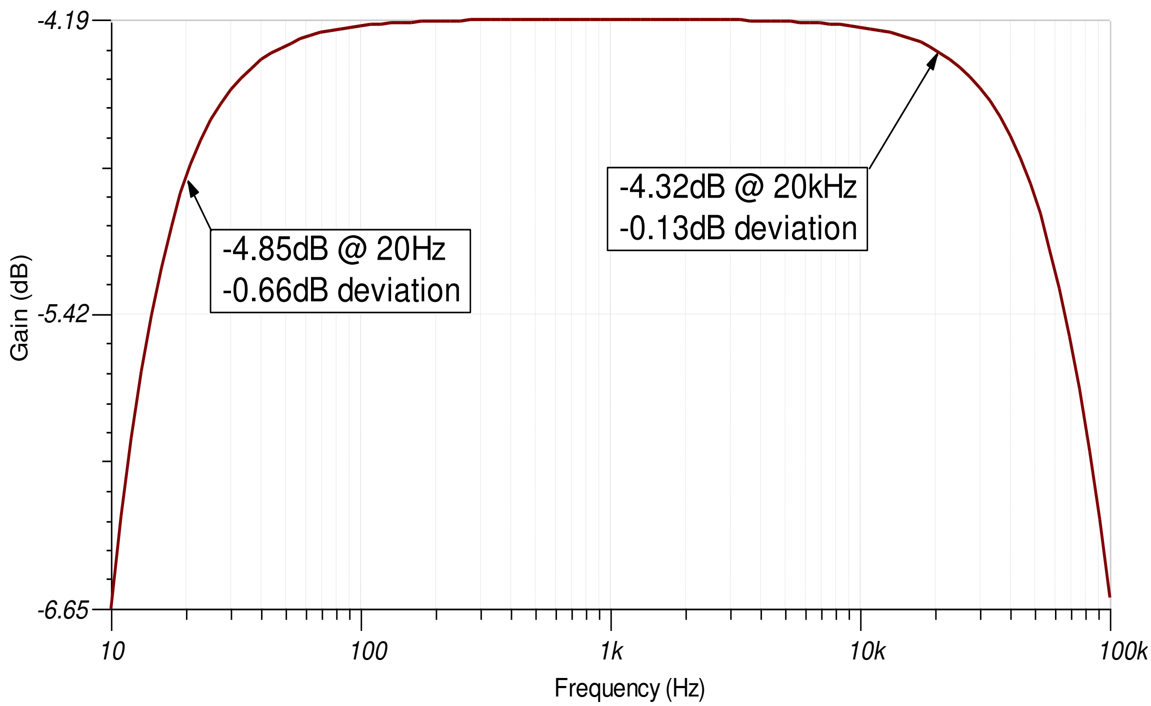
$$C_3 = \frac{1}{2\pi \times R_5 \times f_p} = \frac{1}{2\pi \times 10k\Omega \times 131.044kHz} = 121.451pF \approx 120pF \text{ (Standard Value)}$$

14. Calculate the output capacitor, C_4, based on the cut off frequency calculated in step 9. Assume the output load R_6 is 10kΩ.

$$C_4 = \frac{1}{2\pi \times R_6 \times f_c} = \frac{1}{2\pi 10k\Omega \times 3.956Hz} = 4.023\mu F \approx 3.3\mu F \text{ (Standard Value)}$$

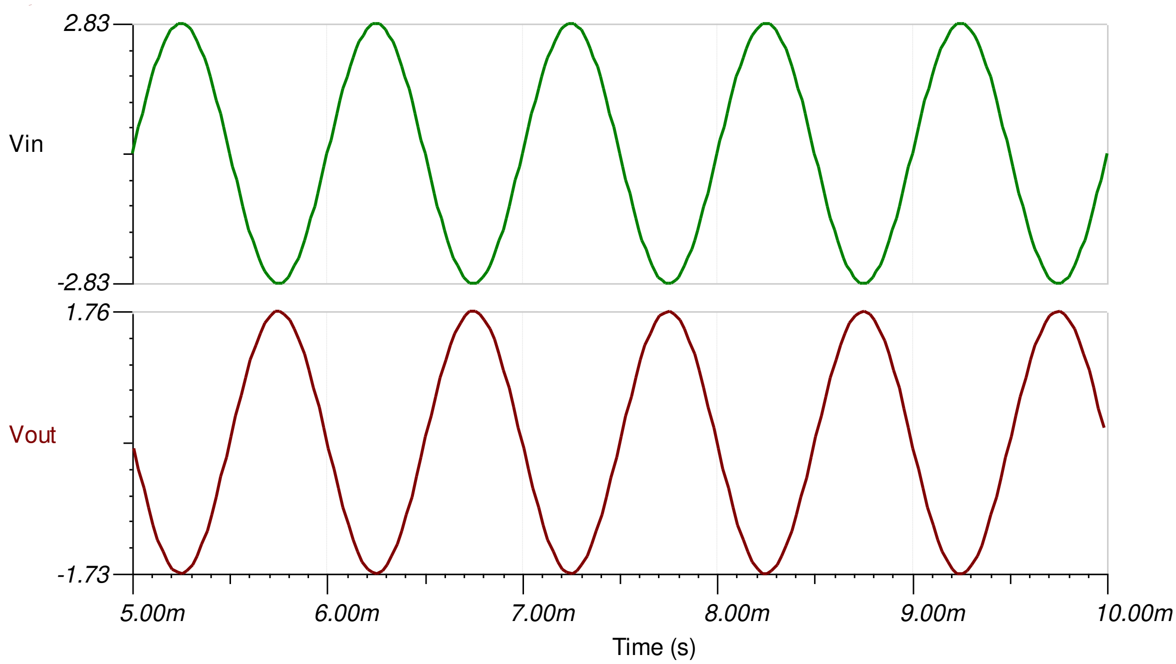
Design Simulations

AC Simulation Results



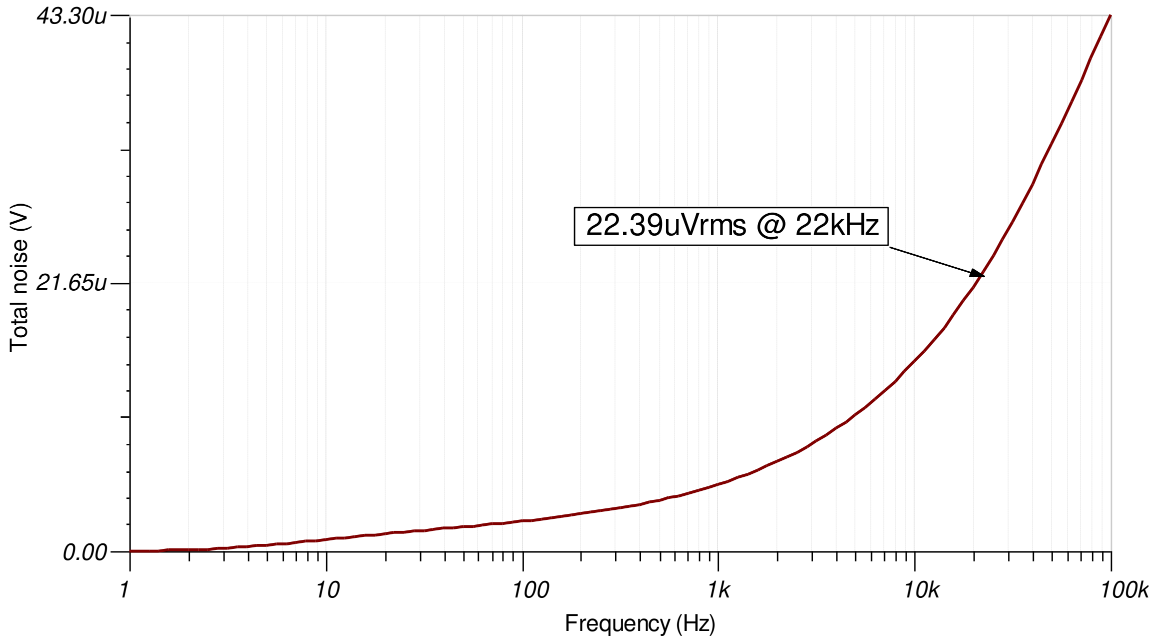
Transient Simulation Results

The input voltage represents the SPL of an input signal to the microphone. A 1 V_{rms} input signal represents 1 Pascal.



Noise Simulation Results

The following simulation results show 22.39uVrms of noise at 22kHz. The noise is measured at a bandwidth of 22kHz to represent the measured noise using an audio analyzer with the bandwidth set to 22kHz.



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOC525
3. TI Precision Designs TIPD181
4. TI Precision Labs

Design Featured Op Amp

TLV6741	
V_{ss}	1.8V to 5.5V
V_{inCM}	(Vee) to (Vcc –1.2V)
V_{out}	Rail–to–rail
V_{os}	150µV
I_q	890uA/Ch
I_b	10pA
UGBW	10MHz
SR	4.75V/µs
#Channels	1
www.ti.com/product/tlv6741	

Design Alternate Op Amp

OPA320	
V_{ss}	1.8V to 5.5V
V_{inCM}	Rail–to–rail
V_{out}	Rail–to–rail
V_{os}	40µV
I_q	1.5mA/Ch
I_b	0.2pA
UGBW	20MHz
SR	10V/µs
#Channels	1, 2
www.ti.com/product/opa320	

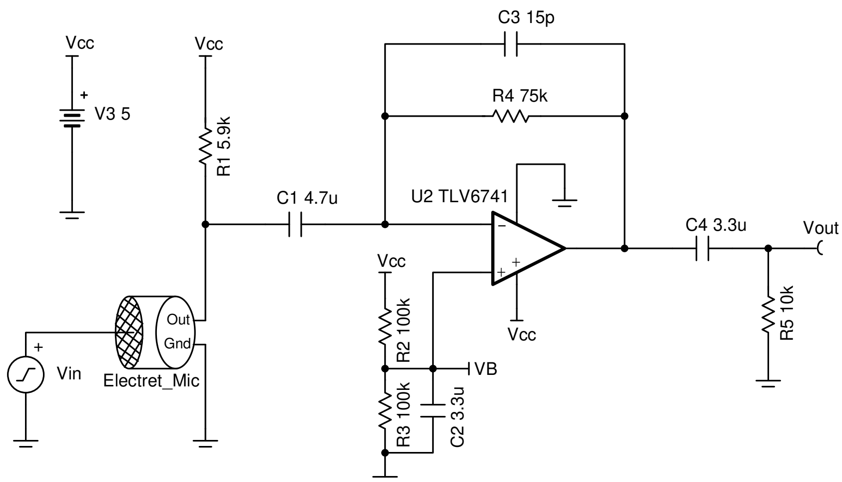
TIA Microphone Amplifier Circuit

Design Goals

Input pressure (Max)	Output Voltage (Max)	Supply		Frequency Response Deviation	
100 dB SPL(2Pa)	1.228 V_{rms}	V_{cc}	V_{ee}	At 20 Hz	At 20 kHz
		5 V	0 V	–0.5 dB	–0.1 dB

Design Description

This circuit uses an op amp in a transimpedance amplifier configuration to convert the output current from an electret capsule microphone into an output voltage. The common mode voltage of this circuit is constant and set to mid–supply eliminating any input–stage cross over distortion.



Design Notes

1. Use the op amp in the linear output operating range, which is usually specified under the A_{OL} test conditions.
2. Use low–K capacitors (tantalum, C0G, and so forth) and thin film resistors help to decrease distortion.
3. Use a battery to power this circuit to eliminate distortion caused by switching power supplies.
4. Use low value resistors and low noise op amp to achieve high performance low noise designs.
5. The voltage connected to R_1 to bias the microphone does not have to match the supply voltage of the op amp. Using a larger microphone bias voltage allows for a larger value or R_1 which decreases the noise gain of the op amp circuit while still maintaining normal operation of the microphone.
6. Capacitor C_1 should be large enough that its impedance is much less than resistor R_1 at audio frequency. Pay attention to the signal polarity when using tantalum capacitors.

Design Steps

The following microphone is chosen as an example to design this circuit.

1.

Microphone parameter	Value
Sensitivity at 94 dB SPL (1 Pa)	–35 ± 4 dBV
Current Consumption (Max)	0.5 mA
Impedance	2.2 kΩ
Standard Operating Voltage	2 V_{dc}

2. Convert the sensitivity to volts per Pascal.

$$10^{\frac{-35dB}{20}} = 17.78\ mV/Pa$$

3. Convert volts per Pascal to current per Pascal.

$$\frac{17.78mV/Pa}{2.2k\Omega} = 8.083\ \mu A/Pa$$

4. Max output current occurs at max sound pressure level of 2Pa.

$$I_{Max} = 2Pa \times 8.083\ \mu A/Pa = 16.166\ \mu A$$

5. Calculate the value of resistor R_4 to set the gain

$$R_4 = \frac{V_{max}}{I_{max}} = \frac{1.228V}{16.166\mu A} = 75.961\ k\Omega \approx 75k\Omega\ \left(\text{Standard value}\right)$$

The final signal gain is:

$$\text{Gain} = 20 \times \log\left(\frac{V_{out}}{V_{in}}\right) = 20 \times \log\left(\frac{16.166\mu A \times 75k\Omega}{2V}\right) = -4.347\ dB$$

6. Calculate the value for the bias resistor R_1. In the following equation, Vmic is the standard operating voltage of the microphone

$$R_1 = \frac{V_{cc} - V_{mic}}{I_s} = \frac{5V - 2V}{0.5mA} = 6k\Omega \approx 5.9\ k\Omega\ \left(\text{Standard value}\right)$$

7. Calculate the high frequency pole according to the allowed deviation at 20 kHz. In the following equation, G_pole1 is the gain at frequency *f*.

$$f_p = \frac{f}{\sqrt{\left(\frac{1}{G\_pole1}\right)^2 - 1}} = \frac{20kHz}{\sqrt{\left(\frac{1}{10^{\frac{-0.1}{20}}}\right)^2 - 1}} = 131.044\ kHz$$

8. Calculate C_3 based on the pole frequency calculated in step 6.

$$C_3 = \frac{1}{2\pi \times f_p \times R_4} = \frac{1}{2\pi \times 131.044kHz \times 75k\Omega} = 16.194\ pF \approx 15pF\ \left(\text{Standard value}\right)$$

9. Calculate the corner frequency at low frequency according to the allowed deviation at 20 Hz. In the following equation, G_pole2 is the gain contributed by each pole at frequency *f* respectively. There are two poles, so divided by two.

$$f_c = f \times \sqrt{\left(\frac{1}{G\_pole2}\right)^2 - 1} = 20Hz \times \sqrt{\left(\frac{1}{10^{\frac{-0.5/2}{20}}}\right)^2 - 1} = 4.868\ Hz$$

10. Calculate the input capacitor C_1 based on the cut off frequency calculated in step 8.

$$C_1 = \frac{1}{2\pi \times R_1 \times f_c} = \frac{1}{2\pi \times 5.9k\Omega \times 4.868Hz} = 5.541\ \mu F \approx 4.7\ \mu F\ \left(\text{Standard value}\right)$$

11. Assuming the output load R_5 is 10 kΩ, calculate the output capacitor C_4 based on the cut off frequency calculated in step 8.

$$C_4 = \frac{1}{2\pi \times R_5 \times f_c} = \frac{1}{2\pi \times 10k\Omega \times 4.868Hz} = 3.269\ \mu F \approx 3.3\ \mu F \ \left(\text{Standard value}\right)$$

12. Set the amplifier input common mode voltage to mid–supply voltage. Select R_2 and R_3 as 100 kΩ. The equivalent resistance equals to the parallel combination of the two resistors:

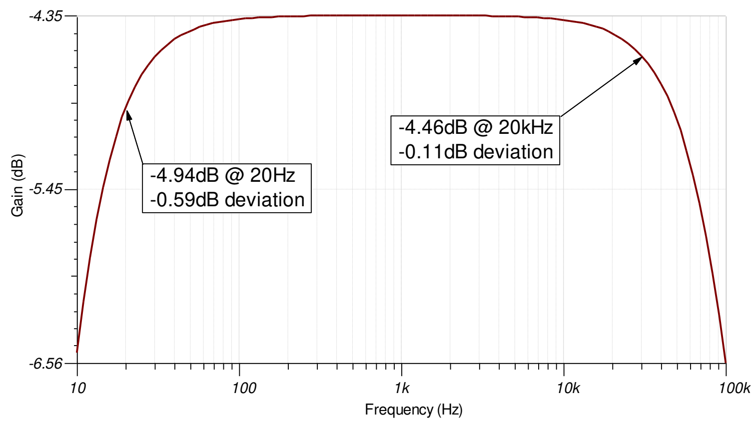
$$R_{eq} = R_2||R_3 = 100k\Omega||100k\Omega = 50k\Omega$$

13. Calculate the capacitor C_2 to filter the power supply and resistor noise. Set the cutoff frequency to 1 Hz.

$$C_2 = \frac{1}{2\pi \times (R_2||R_3) \times 1Hz} = \frac{1}{2\pi \times (100k\Omega||100k\Omega) \times 1Hz} = 3.183\ \mu F \approx 3.3\ \mu F \ \left(\text{Standard value}\right)$$

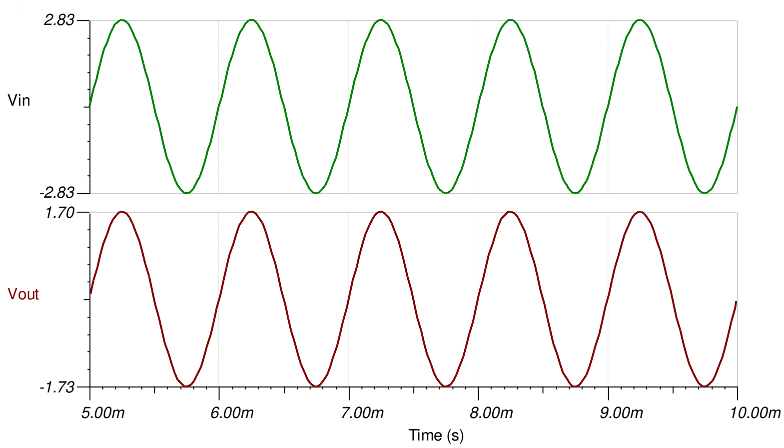
Design Simulations

AC Simulation Results

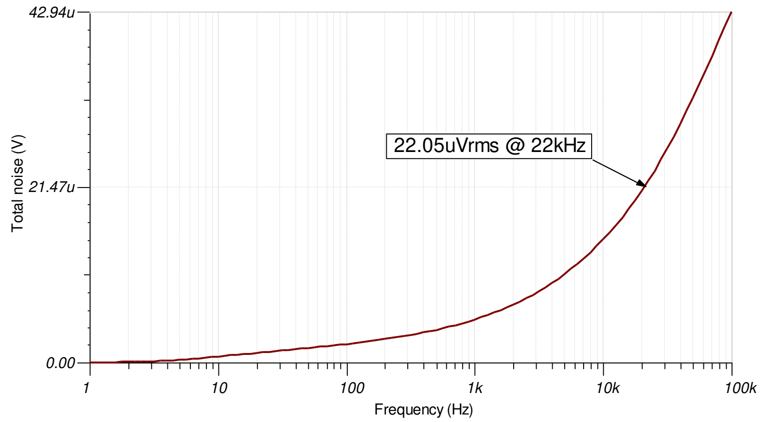


Transient Simulation Results

The input voltage represents the SPL of an input signal to the microphone. A 2 V_{rms} input signal represents 2 Pascal.



The following simulation results show 22.39 μV_{rms} of noise at 22 kHz. The noise is measured at a bandwidth of 22 kHz to represent the measured noise using an audio analyzer with the bandwidth set to 22 kHz.



References:

1. Analog Engineer's Circuit Cookbooks
2. SPICE Simulation File SBOC526
3. TI Precision Designs TIPD181
4. TI Precision Labs

Design Featured Op Amp

TLV6741	
V_{ss}	1.8 V to 5.5 V
V_{inCM}	V_{ee} to V_{cc}–1.2 V
V_{out}	Rail–to–rail
V_{os}	150 µV
I_q	890 µA/Ch
I_b	10 pA
UGBW	10 MHz
SR	4.75 V/µs
#Channels	1
TLV6741	

Design Alternate Op Amp

	OPA172	OPA192
V_{ss}	4.5 V to 36 V	4.5 V to 36 V
V_{inCM}	V_{ee}–0.1 V to V_{cc}–2 V	V_{ee}–0.1 V to V_{cc}+0.1 V
V_{out}	Rail–to–rail	Rail–to–rail
V_{os}	±200 µV	±5 µV
I_q	1.6 mA/Ch	1 mA/Ch
I_b	8 pA	5 pA
UGBW	10 MHz	10 MHz
SR	10 V/µs	20 V/µs
#Channels	1, 2, and 4	1, 2, and 4
	OPA172	OPA192

Temperature Sensing NTC Circuit With MSP430™ Smart Analog Combo

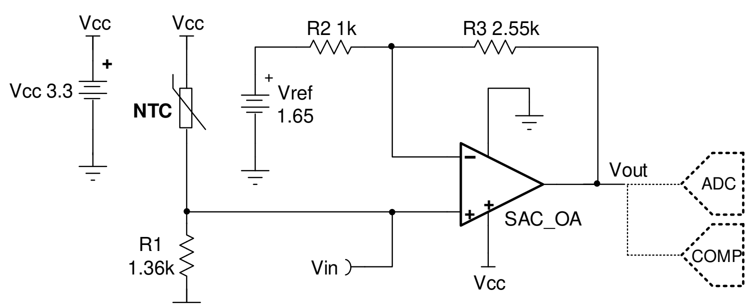
Design Goals

Temperature		Output Voltage		Supply		
T_{Min}	T_{Max}	V_{outMin}	V_{outMax}	V_{cc}	V_{ee}	V_{ref}
25℃	50℃	0.2 V	3.1 V	3.3 V	0 V	1.65 V

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the Smart Analog Combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the Temperature Sensing NTC Circuit Design Files.

This temperature sensing circuit uses a resistor in series with a negative-temperature-coefficient (NTC) thermistor to form a voltage divider, which produces an output voltage that is linear over temperature. The circuit uses the MSP430FR2311 SAC_L1 op-amp in a noninverting amplifier configuration with inverting reference to offset and gain the signal, which helps to use the full ADC resolution and increase measurement accuracy. (Note: The MSP430FR2355 features four SAC_L3 peripherals which each contain a built-in DAC and PGA, providing a single-chip solution for generating Vref and measuring the thermistor circuit.) The output of the integrated SAC op-amp can be sampled directly by the on-board ADC or monitored by the on-board comparator for further processing inside the MCU.



Design Notes

- The connection, Vin, is a negative temperature coefficient output voltage. To measure the output voltage of a PTC thermistor, switch the position of R_1 and the thermistor.
- V_{ref} can be generated using one of the integrated SAC_L3 DACs in the MSP430FR2355 or a voltage divider. If a voltage divider is used the equivalent resistance of the voltage divider will influence the gain of the circuit.
- Using high value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit. It is recommended to use resistor values of approximately 10 kΩ or less.
- If the solution is implemented using the MSP430FR2311, the SAC_L1 op-amp is configured in general purpose mode to measure the thermistor circuit.
- If the solution is implemented using the MSP430FR2355, one SAC_L3 peripheral is configured in DAC mode to generate the reference voltage and another is configured in general purpose mode to measure the thermistor circuit.

Design Steps

$$V_{out} = V_{cc} \times \frac{R_1}{R_{NTC} + R_1} \times \frac{R_2 + R_3}{R_2} - \frac{R_3}{R_2} \times V_{ref}$$

1. Calculate the value of R_1 to produce a linear output voltage. Use the minimum and maximum values of the NTC to obtain a range of values for R_1.

$$R_{NTC\_max} = R_{NTC\ @25°C} = 2.252\ k\Omega, \quad R_{NTC\_min} = R_{NTC\ @50°C} = 819.7\Omega$$

$$R_1 = \sqrt{R_{NTC\ @25°C} \times R_{NTC\ @50°C}} = \sqrt{2.252\ k\Omega \times 819.7\ \Omega} = 1.359\ k\Omega \quad \approx 1.36 k\Omega$$

2. Calculate the input voltage range.

$$V_{inMin} = V_{cc} \times \frac{R_1}{R_{NTC\_max} + R_1} = 3.3\ V \times \frac{1.36\ k\Omega}{2.252\ k\Omega + 1.36\ k\Omega} = 1.2418\ V$$

$$V_{inMax} = V_{cc} \times \frac{R_1}{R_{NTC\_min} + R_1} = 3.3\ V \times \frac{1.36\ k\Omega}{819.7\ \Omega + 1.36\ k\Omega} = 2.0582\ V$$

3. Calculate the gain required to produce the maximum output swing.

$$G_{ideal} = \frac{V_{outMax} - V_{outMin}}{V_{inMax} - V_{inMin}} = \frac{3.1\ V - 0.2\ V}{2.0582\ V - 1.2418\ V} = 3.5519\ \frac{V}{V}$$

4. Select R_2 and calculate R_3 to set the gain in Step 3.

$$\text{Gain} = \frac{R_2 + R_3}{R_2}$$

$$R_2 = 1\ k\Omega \quad (\text{Standard value})$$

$$R_3 = R_2 \times (G_{ideal} - 1) = 1\ k\Omega \times \left(3.5519\frac{V}{V} - 1\right) = 2.5519\ k\Omega$$

$$\text{Choose} \quad R_3 = 2.55\ k\Omega$$

5. Calculate the actual gain based on standard values of R_2 and R_3.

$$G_{actual} = \frac{R_2 + R_3}{R_2} = \frac{1\ k\Omega + 2.55\ k\Omega}{1\ k\Omega} = 3.55\ \frac{V}{V}$$

6. Calculate the output voltage swing based on the actual gain.

$$V_{out\_swing} = (V_{inMax} - V_{inMin}) \times G_{actual} = (2.0582\ V - 1.2418\ V) \times 3.55\ \frac{V}{V} = 2.9\ V$$

7. Calculate the maximum output voltage when the output voltage is symmetrical around mid-supply.

$$V_{outMax} = V_{mid-supply} + \frac{V_{out\_swing}}{2} = \frac{V_{cc} - V_{ee}}{2} + \frac{V_{out\_swing}}{2} = \frac{3.3\ V - 0\ V}{2} + \frac{2.9\ V}{2} = 3.1\ V$$

8. Calculate the reference voltage.

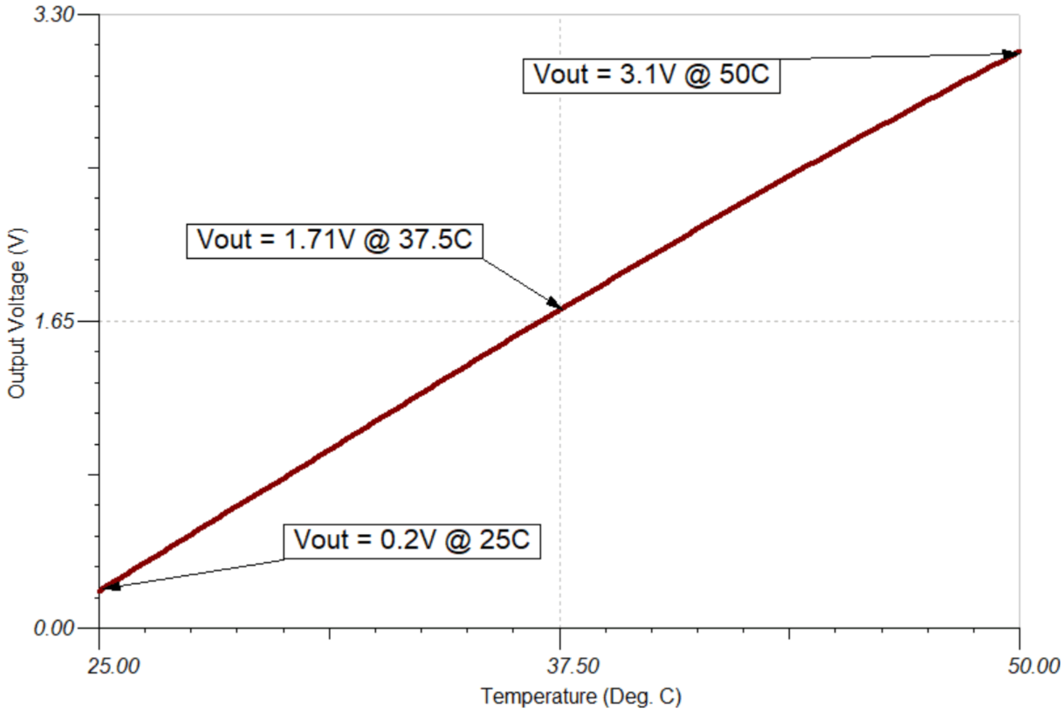
$$V_{outMax} = V_{inMax} \times G_{actual} - \frac{R_3}{R_2} \times V_{ref}$$

$$3.1\ V = 2.0582\ V \times 3.55\ \frac{V}{V} - \frac{2.55\ k\Omega}{1\ k\Omega} \times V_{ref}$$

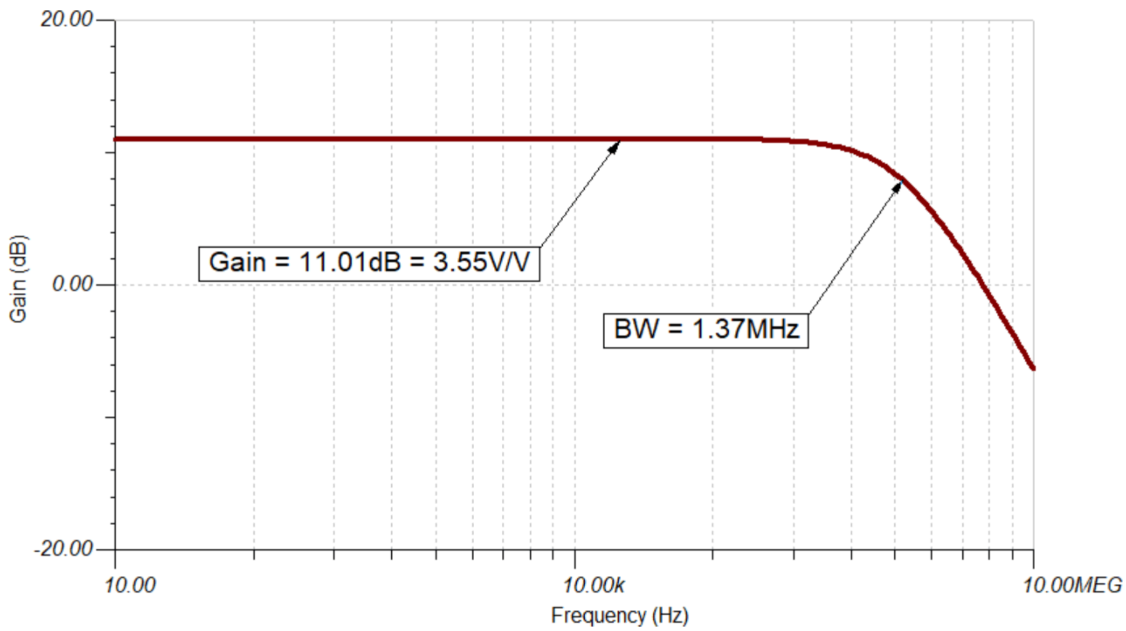
$$V_{ref} = \frac{2.0582\ V \times 3.55\ \frac{V}{V} - 3.1\ V}{\frac{2.55\ k\Omega}{1\ k\Omega}} = 1.65\ V$$

Design Simulations

DC Transfer Results



AC Simulation Results



Target Applications

- Field temperature transmitters
- Thermostats
- Thermometers
- Thermistor probes
- System temperature monitor

References

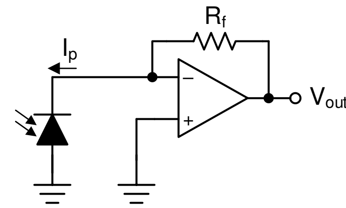
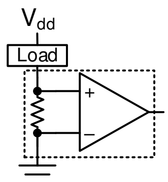
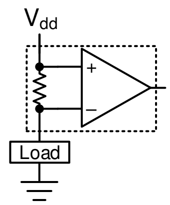
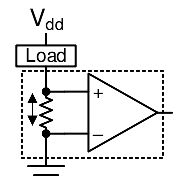
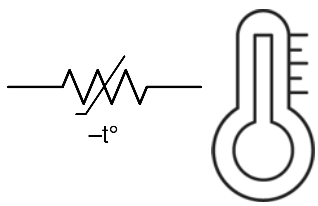
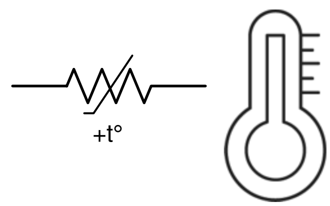
1. MSP430 MCUs Smart Analog Combo Training
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. MSP430 Temp Sense NTC Circuit Code Examples and SPICE Simulation File

Design Featured Op Amp

MSP430FRxx Smart Analog Combo		
	MSP430FR2311 SAC_L1	MSP430FR2355 SAC_L3
V_{cc}	2.0 V to 3.6 V	
V_{CM}	-0.1 V to V_{CC} + 0.1 V	
V_{out}	Rail-to-rail	
V_{os}	±5 mV	
A_{OL}	100 dB	
I_q	350 µA (high-speed mode)	
	120 µA (low-power mode)	
I_b	50 pA	
UGBW	4 MHz (high-speed mode)	2.8 MHz (high-speed mode)
	1.4 MHz (low-power mode)	1 MHz (low-power mode)
SR	3 V/µs (high-speed mode)	
	1 V/µs (low-power mode)	
Number of channels	1	4
	MSP430FR2311	MSP430FR2355

Design Alternate Op Amp

MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
MSP430FR2311	

Low-noise and long-range PIR sensor conditioner circuit 	Bridge amplifier circuit 	Transimpedance amplifier circuit 
Single-supply, low-side, unidirectional current-sensing circuit 	High-side current sensing with discrete difference amplifier circuit 	Low-side, bidirectional current-sensing circuit 
Half-wave rectifier circuit 	Temperature sensing with NTC thermistor circuit 	Temperature sensing with PTC thermistor circuit 

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 19, 2019 to March 9, 2020	**Page**
• Added *Related MSP430 Circuits* section	1

Analog Engineer's Circuit

Single-Supply Strain Gauge Bridge Amplifier Circuit with MSP430™ Smart Analog Combo

Design Goals

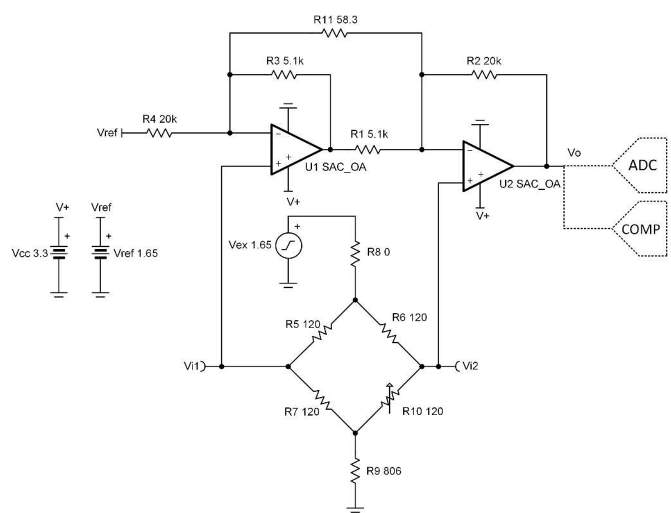
Input V_{iDiff} (V_{i2} – V_{i1})		Output		Supply		
V_{iDiff_Min}	V_{iDiff_Max}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	V_{ref}
–2.22 mV	2.27 mV	0.1 V	3.2 V	3.3 V	0 V	1.65 V

Strain Gauge Resistance Variation (R_{10})	V_{cm}	Gain
115 Ω to 125 Ω	1.34 V	690 V/V

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the Smart Analog Combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the Strain Gauge Bridge Amplifier Circuit Design Files.

A strain gauge is a sensor whose resistance varies with applied force. The change in resistance is directly proportional to how much strain the sensor is experiencing due to the force applied. This pressure sensing circuit uses a strain gauge placed in a bridge configuration to measure the variation in resistance. This design leverages all four of the built-in op-amp blocks (SACs) in the MSP430FR2355. Two SAC_L3 peripherals are configured in general-purpose mode to amplify a differential signal created by the change in resistance of a strain gauge while the other two are configured in DAC mode to supply the reference voltage (Vref) and the excitation voltage (Vex). By varying R_{10}, a small differential voltage is created at the output of the Wheatstone bridge which is fed to the 2 SAC op-amp instrumentation amplifier inputs. The linearity of the instrumentation amplifier is based on the input common-mode and output-swing ranges of the MSP430 SAC op-amp, which can be found in the specification chart at the end of this document. The output of the second stage op-amp can be sampled directly by the on-board ADC or monitored by the on-board comparator for further processing inside the MCU.



Design Notes

- Resistors R_5, R_6, and R_7 of the Wheatstone bridge must match the stain gauge nominal resistance and must be equal to avoid creating a bridge offset voltage.
- Low tolerance resistors must be used to minimize the offset and gain errors due to the bridge resistors.
- V_{ex} sets the excitation voltage of the bridge and the common-mode voltage V_{cm}.
- V_{ref} biases the output voltage of the MSP430 SAC-based instrumentation amplifier to mid-supply to allow differential measurements in the positive and negative directions.
- R_{11} sets the gain of the instrumentation amplifier circuit.
- R_8 and R_9 set the common-mode voltage of the instrumentation amplifier and limits the current through the bridge. This current determines the differential signal produced by the bridge. However, there are limitations on the current through the bridge due to self-heating effects of the bridge resistors and strain gauge.
- Ensure that $R_1 = R_3$ and $R_2 = R_4$ and that ratios of R_2/R_1 and R_4/R_3 are matched to set the V_{ref} gain to 1 V/V and maintain high DC CMRR of the instrumentation amplifier.
- Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
- If the solution is implemented using the MSP430FR2311, the instrumentation amplifier would need to consist of one SAC_L1 op-amp and one Transimpedance Amplifier (TIA) op-amp. The excitation and reference voltages, Vex and Vref, would need to be supplied externally (for example, voltage divider).
- The Strain Gauge Bridge Amplifier Circuit Design Files include code examples showing how to properly initialize the SAC peripherals.

Design Steps

1. Select R_5, R_6 and R_7 to match the stain gauge nominal resistance

$$R_{gauge} = R_5 = R_6 = R_7 = 120\Omega$$

2. Choose R_9 to set the common mode voltage of the instrumentation amplifier at 1.34 V.

$$V_{cm} = \frac{\frac{R_{bridge}}{2} + R_9}{R_{bridge} + R_8 + R_9} \times V_{ex}$$

Where R_{bridge} = total resistance of the bridge

Choose $R_8 = 0\,\Omega$ to allow maximum current through the bridge

$$V_{cm} = \frac{\frac{120\Omega \times 4}{2} + R_9}{(120\Omega \times 4) + 0\Omega + R_9} \times 1.65\text{V} = 1.34\text{V}$$

$$\frac{240 + R_9}{480 + 0\Omega + R_9} = \frac{1.34\text{V}}{1.65\text{V}} = 0.812$$

$$0.188\,R_9 = 149.82 \rightarrow R_9 = \frac{149.82}{0.188} = 797.42\Omega \rightarrow R_9 = 806\,\Omega\ \left(\text{Standard value}\right)$$

3. Calculate the gain required to produce the desired output voltage swing

$$G = \frac{V_{oMax} - V_{oMin}}{V_{iDiff\_Min} - V_{iDiff\_Min}} = \frac{3.2\text{ V} - 0.1\text{V}}{0.00222\text{V} - (-0.00227\text{V})} = 690.42\frac{\text{V}}{\text{V}}$$

4. Select R_1, R_2, R_3 and R_4. To set the V_{ref} gain at 1 V/V and avoid degrading the instrumentation amplifier's CMRR, R_1 must equal R_3 and R_2 equal R_4.

Choose $R_1 = R_3 = 5.1\text{k}\,\Omega$ and $R_3 = R_4 = 20\text{ k}\,\Omega$ (Standard value)

5. Calculate R_{11} to meet the required gain

$$G = 1 + \frac{R_4}{R_3} + \frac{2 \times R_2}{R_{11}} = 690.42\frac{\text{V}}{\text{V}}$$

$$G = 1 + \frac{20\text{k}\Omega}{5.1\text{k}\Omega} + \frac{2 \times R_2}{R_{11}} = 690.42\frac{\text{V}}{\text{V}} \rightarrow 4.92 + \frac{40\text{k}\Omega}{R_{11}} = 690.42\frac{\text{V}}{\text{V}} \rightarrow \frac{40\text{k}\Omega}{R_{11}} = 685.5 \rightarrow R_{11} = \frac{40\text{k}\Omega}{685.5} = 58.35\Omega \rightarrow R_{11} = 58.3\Omega\ \left(\text{Standard Value}\right)$$

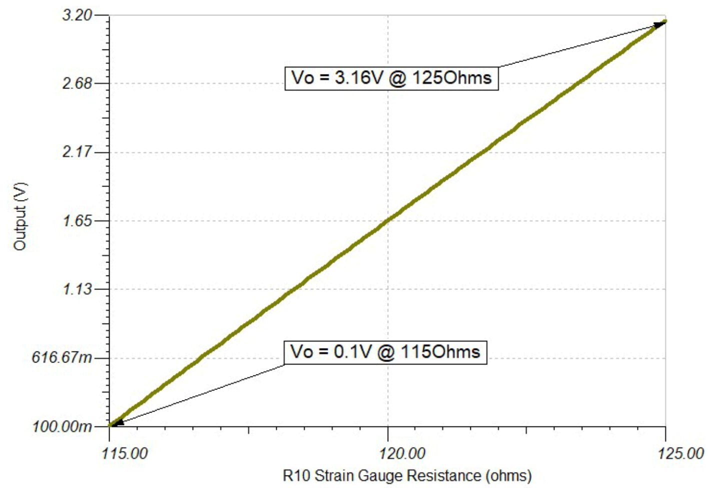
6. Calculate the current through the bridge

$$I_{bridge} = \frac{V_{ex}}{R_8 + R_9 + R_{bridge}} = \frac{1.65V}{0\Omega + 806\Omega + 120\Omega \times 4}$$

$$I_{bridge} = \frac{1.65V}{806\Omega + 480\Omega} \rightarrow I_{bridge} = 1.28mA$$

Design Simulations

DC Simulation Results



Target Applications

- Pressure transmitter
- Weigh scale

References

1. MSP430 Strain Gauge Bridge Amplifier Circuit Code Examples and SPICE Simulation File
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. MSP430 MCUs Smart Analog Combo Training

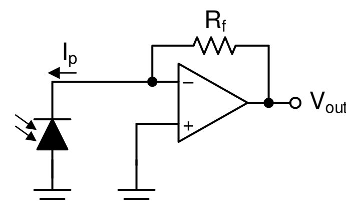
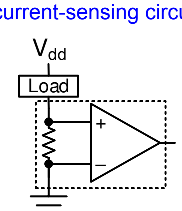
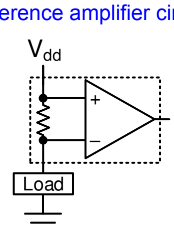
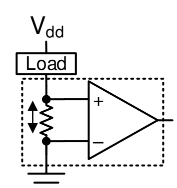
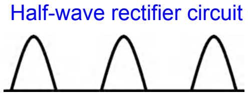
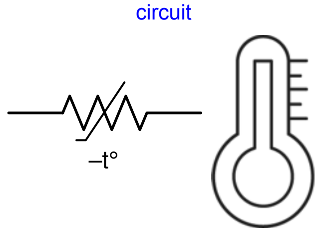
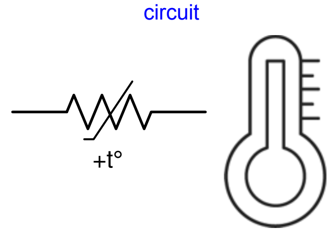
Design Featured Op Amp

MSP430FRxx Smart Analog Combo		
	MSP430FR2311 SAC_L1	MSP430FR2355 SAC_L3
V_{cc}	2.0 V to 3.6 V	
V_{CM}	-0.1 V to V_{CC} + 0.1 V	
V_{out}	Rail-to-rail	
V_{os}	±5 mV	
A_{OL}	100 dB	
I_q	350 µA (high-speed mode)	
	120 µA (low-power mode)	
I_b	50 pA	
UGBW	4 MHz (high-speed mode)	2.8 MHz (high-speed mode)
	1.4 MHz (low-power mode)	1 MHz (low-power mode)
SR	3 V/µs (high-speed mode)	
	1 V/µs (low-power mode)	
Number of channels	1	4
	MSP430FR2311	MSP430FR2355

Design Alternate Op Amp

MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
MSP430FR2311	

Related MSP430 Circuits

Low-noise and long-range PIR sensor conditioner circuit 	Bridge amplifier circuit 	Transimpedance amplifier circuit 
Single-supply, low-side, unidirectional current-sensing circuit 	High-side current sensing with discrete difference amplifier circuit 	Low-side, bidirectional current-sensing circuit 
Half-wave rectifier circuit 	Temperature sensing with NTC thermistor circuit 	Temperature sensing with PTC thermistor circuit 

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 27, 2019 to March 6, 2020	Page
• Added *Related MSP430 Circuits* section	1

Analog Engineer's Circuit

Transimpedance Amplifier Circuit with MSP430™ Smart Analog Combo

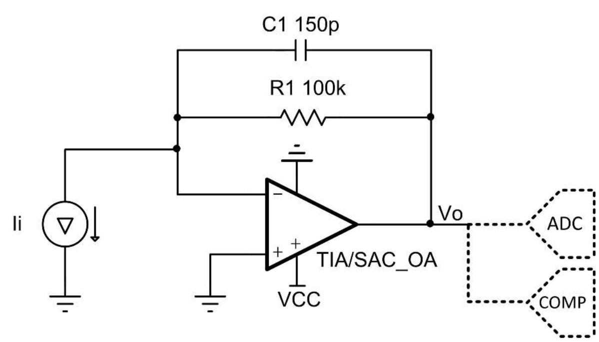
Design Goals

Input		Output		BW	Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	f_p	V_{cc}	V_{ee}
0 A	30 µA	0.2 V	3.2 V	10 kHz	3.3 V	0 V

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the smart analog combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the MSP430 Transimpedance Amplifier Circuit Design Files.

The transimpedance op amp circuit configuration converts an input current source into an output voltage. The current to voltage gain is based on the feedback resistance. The circuit can maintain a constant voltage bias across the input source as the input current changes, which benefits many sensors. The characteristics of the Transimpedance Amplifier (TIA) module in MSP430FR2311 make it especially suited for this functionality; however, this circuit can also be implemented with the MSP430FR2311 SAC_L1, or with the MSP430FR2355 SAC_L3 with additional built-in DAC and PGA capabilities. The output of these integrated amplifiers can be sampled directly by the on-board ADC or monitored by the on-board comparator for further processing inside the MCU.



Design Notes

- An op amp with low input bias current reduces DC errors.
- A bias voltage can be added to the non-inverting input to set the output voltage for 0-A input currents. The integrated 12-bit DAC in MSP430FR2355 SAC_L3 can be used for this purpose.
- Operate within the linear output voltage swing (see A_{ol} specification) to minimize non-linearity errors.
- If the solution is implemented with the MSP430FR2311, this circuit can be realized by the TransImpedance Amplifier (TIA) module, or by the SAC_L1.
- If the solution is implemented with the MSP430FR2355 SAC_L3, the op-amp should be configured in general-purpose mode.
- The MSP430 Transimpedance Amplifier Circuit Design Files include code examples showing how to properly initialize the peripherals.

Design Steps

1. Select the gain resistor.

$$R_1 = \frac{V_{oMax} - V_{oMin}}{I_{iMax}} = \frac{3.2V - 0.2V}{30\mu A} = 100k\Omega$$

2. Select the feedback capacitor to meet the circuit bandwidth.

$$C_1 \le \frac{1}{2 \times \pi \times R_1 \times f_p}$$

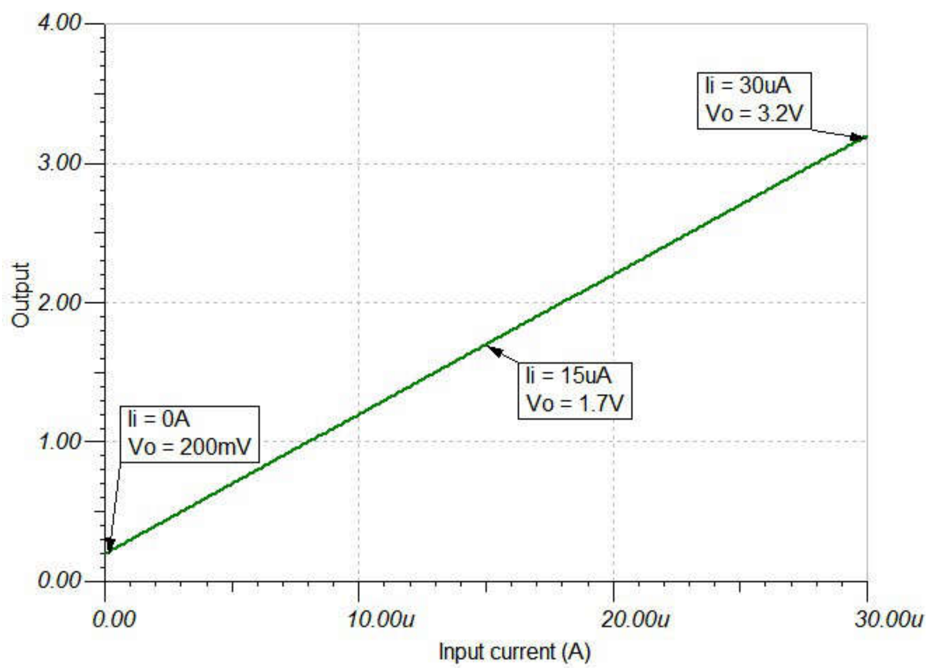
$$C_1 \le \frac{1}{2 \times \pi \times 100k\Omega \times 10kHz} \le 159pF \approx 150pF \text{ (Standard Value)}$$

3. Calculate the necessary op amp gain bandwidth (GBW) for the circuit to be stable.

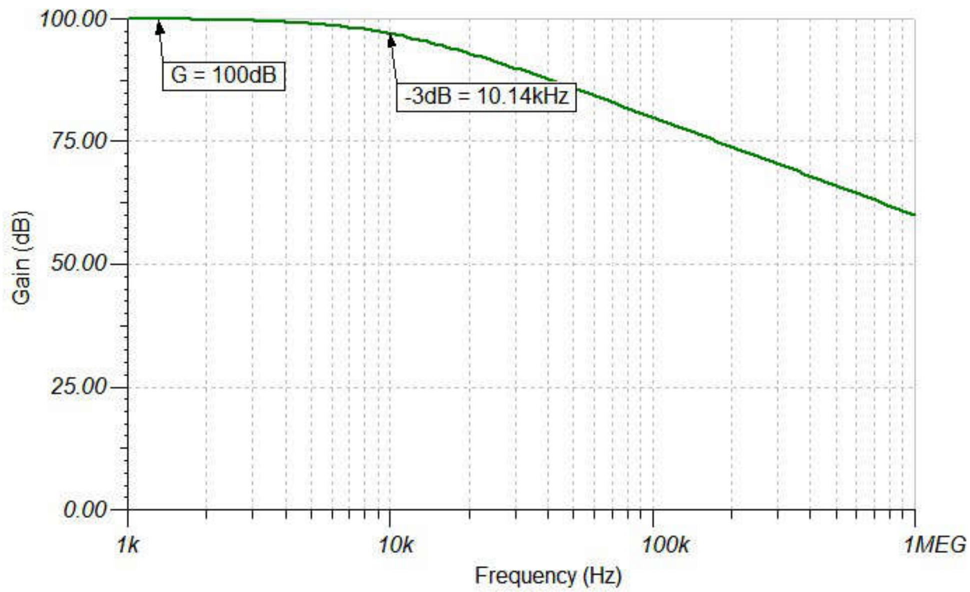
$$GBW > \frac{C_{in} + C_1}{2 \times \pi \times R_1 \times {C_1}^2} > \frac{7pF + 150pF}{2 \times \pi \times 100k\Omega \times (150pF)^2} > 11.10kHz$$

Design Simulations

DC Simulation Results



AC Simulation Results



Target Applications

- Smoke and Heat Detectors
- Air Quality and Gas Detection
- Gas Detectors
- Motion Detectors
- Pulse Oximeters
- Blood Glucose Monitors

Design References

1. MSP430 Transimpedance Amplifier Circuit Code Examples and SPICE Simulation Files
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. MSP430 MCUs Smart Analog Combo Training

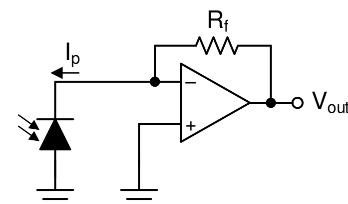
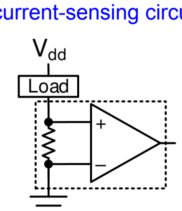
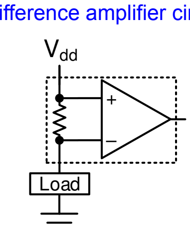
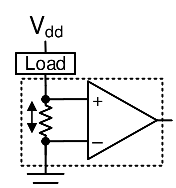
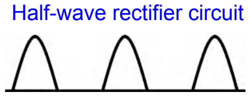
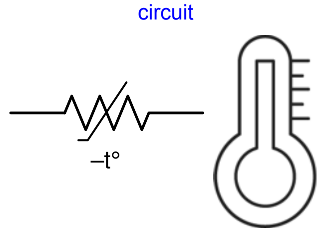
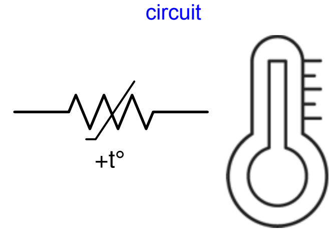
Design Featured Op Amp

MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
	MSP430FR2311

Design Alternate Op Amp

MSP430FRxx Smart Analog Combo		
	MSP430FR2311 SAC_L1	MSP430FR2355 SAC_L3
V_{cc}	2.0 V to 3.6 V	
V_{CM}	-0.1 V to V_{CC} + 0.1 V	
V_{out}	Rail-to-rail	
V_{os}	±5 mV	
A_{OL}	100 dB	
I_q	350 µA (high-speed mode)	
	120 µA (low-power mode)	
I_b	50 pA	
UGBW	4 MHz (high-speed mode)	2.8 MHz (high-speed mode)
	1.4 MHz (low-power mode)	1 MHz (low-power mode)
SR	3 V/µs (high-speed mode)	
	1 V/µs (low-power mode)	
Number of channels	1	4
	MSP430FR2311	MSP430FR2355

Related MSP430 Circuits

Low-noise and long-range PIR sensor conditioner circuit 	Bridge amplifier circuit 	Transimpedance amplifier circuit 
Single-supply, low-side, unidirectional current-sensing circuit 	High-side current sensing with discrete difference amplifier circuit 	Low-side, bidirectional current-sensing circuit 
Half-wave rectifier circuit 	Temperature sensing with NTC thermistor circuit 	Temperature sensing with PTC thermistor circuit 

1 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Analog Engineer's Circuit
High-Side Current-Sensing Circuit Design with MSP430™ Smart Analog Combo

TEXAS INSTRUMENTS

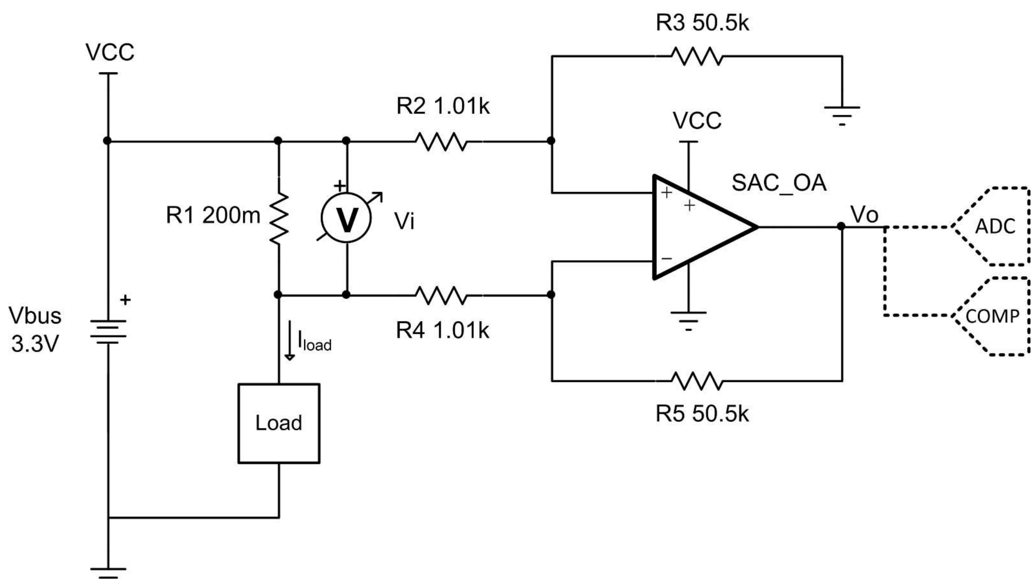
Design Goals

Input		Output		Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
25 mA	300 mA	0.25 V	3 V	3.3 V	0 V

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the smart analog combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the High-Side Current Sensing Circuit Design Files.

This single-supply, high-side, low-cost current sensing solution detects load current between 25 mA and 300 mA and converts it to an output voltage from 0.25 V to 3 V. High-side sensing allows for the system to identify ground shorts and does not create a ground disturbance on the load. The circuit uses the MSP430FR2311 SAC_L1 op-amp in general-purpose (GP) mode with OAx+ and OAx- dedicated as noninverting and inverting inputs. The same approach can be implemented with the MSP430FR2355, featuring four SAC_L3 peripherals with additional built-in DAC and PGA capabilities. The output of the integrated SAC op-amp can be sampled directly by the on-board ADC or monitored by the on-board comparator for further processing inside the MCU.



Design Notes

- DC common-mode rejection ratio (CMRR) performance is dependent on the matching of the gain setting resistors, R_2-R_5.
- Increasing the shunt resistor increases power dissipation.
- Ensure that the common-mode voltage is within the linear input operating region of the amplifier. The common-mode voltage is set by the resistor divider formed by R_2, R_3, and the bus voltage. Depending on the common-mode voltage determined by the resistor divider a rail-to-rail input (RRI) amplifier may not be required for this application.
- An op amp that does not have a common-mode voltage range that extends to V_{cc} may be used in low-gain or an attenuating configuration.
- A capacitor placed in parallel with the feedback resistor will limit bandwidth, improve stability, and help reduce noise.
- Use the op amp in a linear output operating region. Linear output swing is usually specified under the A_{OL} test conditions.
- If the solution is implemented with the MSP430FR2311 SAC_L1 or with the MSP430FR2355 SAC_L3, the op-amp is configured in general-purpose mode.
- If the solution is implemented using the MSP430FR2311 TIA, the input voltage range is limited to $V_{CC}/2$, so the gain or range must be adjusted accordingly.
- The High-Side Current Sensing Circuit Design Files include code examples showing how to properly initialize the SAC peripherals.

Design Steps

1. The full transfer function of the circuit is provided below.

$$V_o = I_{in} \times R_1 \times \frac{R_5}{R_4}$$
$$\text{Given} \quad R_2 = R_4 \quad \text{and} \quad R_3 = R_5$$

2. Calculate the maximum shunt resistance. Set the maximum voltage across the shunt to 60 mV.

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{60mV}{300mA} = 200m\Omega$$

3. Calculate the gain to set the maximum output swing range.

$$\text{Gain} = \frac{V_{oMax} - V_{oMin}}{(I_{iMax} - I_{iMin}) \times R_1} = \frac{3V - 0.25V}{(0.3A - 0.025A) \times 200m\Omega} = 50\frac{V}{V}$$

4. Calculate the gain setting resistors to set the gain calculated in step 3.

$$\text{Choose} \quad R_2 = R_4 = 1.01k\,\Omega \quad (\text{Standard} \quad \text{value})$$
$$R_3 = R_5 = R_2 \times \text{Gain} = 1.01k\,\Omega \times 50\frac{V}{V} = 50.5k\,\Omega\ (\text{Standard} \quad \text{value})$$

5. Calculate the common-mode voltage of the amplifier to ensure linear operation.

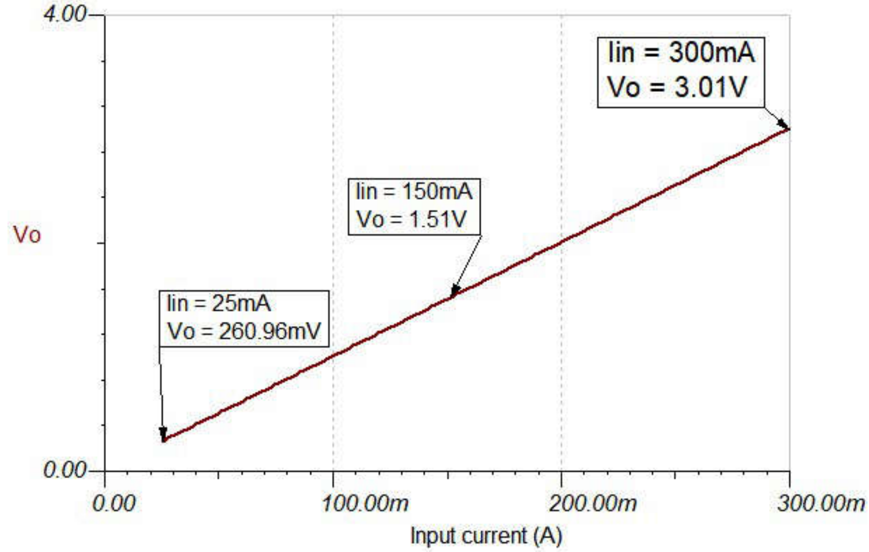
$$V_{cm} = V_{CC} \times \frac{R_3}{R_2 + R_3} = 3.3V \times \frac{50.5k}{1.01k + 50.5k} = 3.235V$$

6. The upper cutoff frequency (f_H) is set by the non-inverting gain (noise gain) of the circuit and the gain bandwidth (GBW) of the op amp.

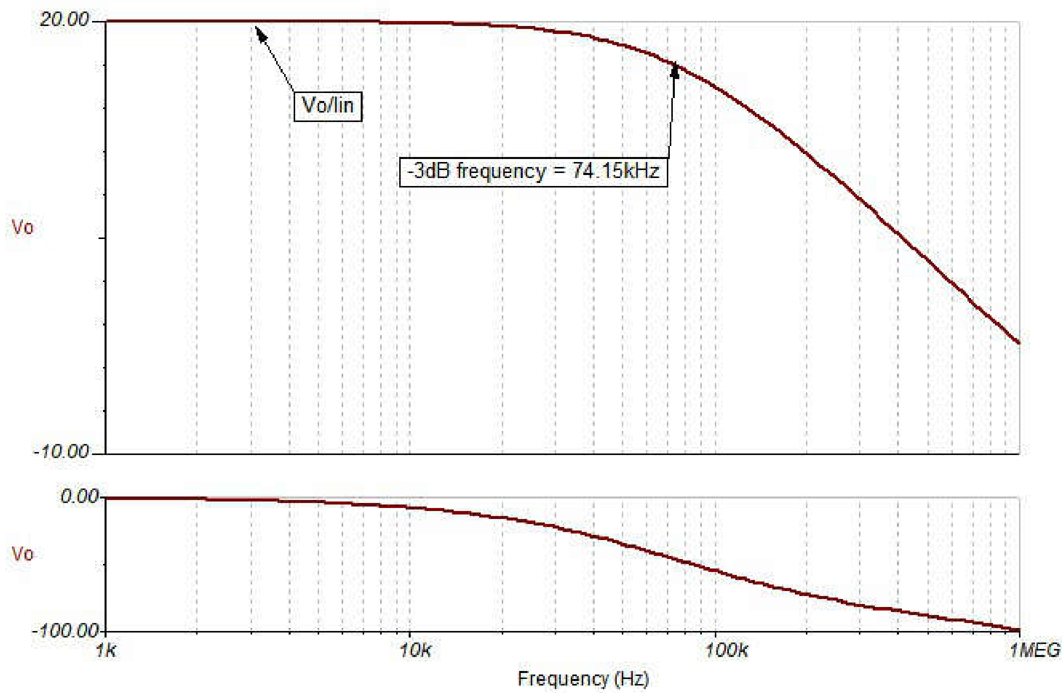
$$f_H = \frac{GBW}{\text{Noise Gain}} = \frac{4MHz}{51\frac{V}{V}} = 78.43 \quad kHz$$

Design Simulations

DC Simulation Results



AC Simulation Results



Target Applications

- Cordless power tool battery pack
- E-bike, e-scooter battery pack
- Motor drives
- LED luminaire
- Grid infrastructure

References

1. High-Side Current Sensing Circuit Design Files
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. MSP430 MCUs Smart Analog Combo Training

Design Featured Op Amp

MSP430FRxx Smart Analog Combo		
	MSP430FR2311 SAC_L1	MSP430FR2355 SAC_L3
V_{cc}	2.0 V to 3.6 V	
V_{CM}	-0.1 V to V_{CC} + 0.1 V	
V_{out}	Rail-to-rail	
V_{os}	±5 mV	
A_{OL}	100 dB	
I_q	350 µA (high-speed mode)	
	120 µA (low-power mode)	
I_b	50 pA	
UGBW	4 MHz (high-speed mode)	2.8 MHz (high-speed mode)
	1.4 MHz (low-power mode)	1 MHz (low-power mode)
SR	3 V/µs (high-speed mode)	
	1 V/µs (low-power mode)	
Number of channels	1	4
	MSP430FR2311	MSP430FR2355

Design Alternate Op Amp

MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
	MSP430FR2311

Related MSP430 Circuits

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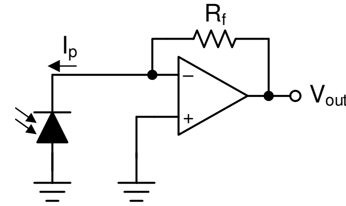
</td>
<td>Transimpedance amplifier circuit

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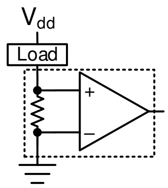
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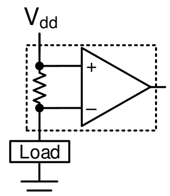
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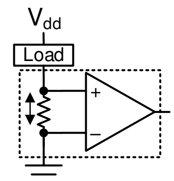
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<td>Half-wave rectifier circuit
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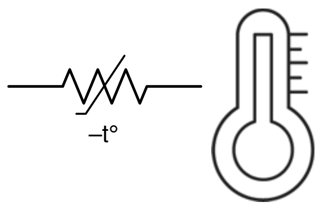
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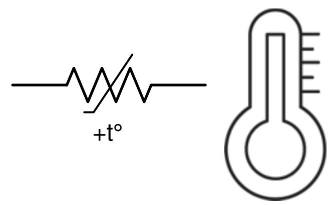
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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 26, 2019 to March 6, 2020	Page
• Added *Related MSP430 Circuits* section	1

Analog Engineer's Circuit

Single-Supply, Low-Side, Unidirectional Current-Sensing Circuit with MSP430™ Smart Analog Combo

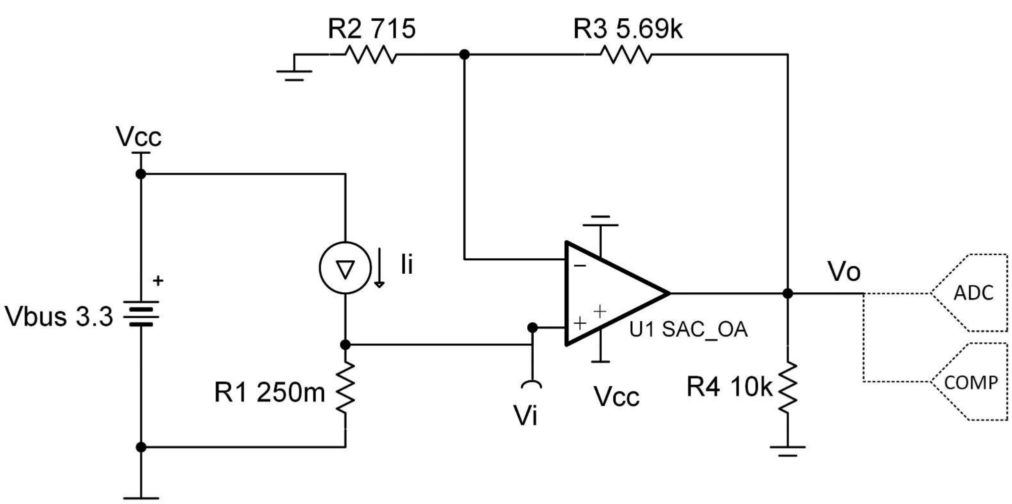
Design Goals

Input		Output		Supply		Full-Scale Range Error
I_{iMax}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}	FSR_{Error}
1 A	250 mV	100 mV	2.25 V	3.3 V	0 V	2.09%

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the Smart Analog Combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the Single-Supply, Low-Side, Unidirectional Current-Sensing Circuit Design Files.

This single-supply, low-side, current sensing solution accurately detects load current up to 1 A and converts it to a voltage between 100 mV and 2.25 V. The circuit uses the MSP430FR2311 SAC_L1 op-amp in a noninverting amplifier configuration. There is room for further integration by using the programmable gain stage block within the MSP430FR2355 SAC_L3 peripheral which allows you to integrate the feedback resistor ladder (R2 and R3) into the MCU. The input current range and output voltage range can be scaled as necessary and larger supplies can be used to accommodate larger swings. The output of the second stage op-amp can be sampled directly by the onboard ADC or monitored by the onboard comparator for further processing inside the MCU.



Design Notes

- Use the op amp linear output operating range, which is usually specified under the test conditions.
- The common-mode voltage is equal to the input voltage.
- The tolerance of the shunt resistor and feedback resistors determine the gain error of the circuit.
- Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
- Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
- The small-signal bandwidth of this circuit depends on the gain of the circuit and gain bandwidth product (GBP) of the amplifier.
- Filtering can be accomplished by adding a capacitor in parallel with R_3. Adding a capacitor in parallel with R_3 also improves the stability of the circuit if high-value resistors are used.
- If the solution is implemented with the MSP430FR2355 SAC_L3, the op-amp can be configured in noninverting programmable gain amplifier mode or general-purpose mode with external R2 and R3 passives to measure the current-sense circuit.
- If the solution is implemented using the MSP430FR2311, the op-amp can be realized by the SAC_L1 op-amp or by the transimpedance amplifier (TIA) op-amp to measure the current-sense circuit.
- The enhanced reference module in the MSP430FR2355 can be used to scale the ADC using a VREF of 2.5 V to more accurately measure the output of the current sensing AFE.
- The Single-Supply, Low-Side, Unidirectional Current-Sensing Circuit Design Files include code examples showing how to properly initialize the SAC peripherals.

Design Steps

The transfer function for this circuit is given below.

$$V_o = I_i \times R_1 \times \left(1 + \frac{R_3}{R_2}\right)$$

1. Define the full-scale shunt voltage and calculate the maximum shunt resistance.

$$V_{iMax} = 250\ \text{mV} \quad \text{at} \quad I_{iMax} = 1\ \text{A}$$

$$R_1 = \frac{V_{iMax}}{I_{iMax}} = \frac{250\ \text{mV}}{1\ \text{A}} = 250\ \text{m}\ \Omega$$

2. Calculate the gain required for maximum linear output voltage.

$$V_{iMax} = 250\ \text{mV} \quad \text{and} \quad V_{oMax} = 2.25\ \text{V}$$

$$\text{Gain} = \frac{V_{oMax}}{V_{iMax}} = \frac{2.25\ \text{V}}{250\ \text{mV}} = 9\frac{\text{V}}{\text{V}}$$

3. Select standard values for R_2 and R_3.

   Let R_2 = 715 Ω (0.1% Standard Value)

$$\text{Gain} = 9\frac{\text{V}}{\text{V}} = 1 + \frac{R_3}{R_2} \tag{1}$$

$$R_3 = \left(9\ \frac{\text{V}}{\text{V}} - 1\right) * R_2 = 8 * 715\ \Omega = 5.72\ k\Omega \tag{2}$$

   Choose R_3 = 5.69 kΩ (0.1% Standard Value)

   Note: The feedback resistor ladder (R_2 and R_3) can be realized using the integrated programmable gain resistor ladder of the SAC_L3 with a programmed noninverting gain of 9x. This implementation is showcased in the MSP430FR2355 code example. If the SAC op-amps are being used in general purpose mode, external resistors would be used to build the feedback resistor ladder.

4. Calculate minimum input current before hitting output swing-to-rail limit. I_{iMin} represents the minimum accurately detectable input current.

$$V_{oMin} = 100\ \text{mV};\quad R_1 = 250\ \text{m}\ \Omega$$

$$V_{iMin} = \frac{V_{oMin}}{\text{Gain}} = \frac{100\ \text{mV}}{9\ \frac{V}{V}} = 11.1\ \text{mV}$$

$$I_{iMin} = \frac{V_{iMin}}{R_1} = \frac{11.1\ \text{mV}}{250\ \text{m}\ \Omega} = 44.4\ \text{mA}$$

5. Calculate Full scale range error and relative error. V_{os} is the typical offset voltage found in data sheet.

$$\text{FSR}_{\text{error}} = \left(\frac{V_{os}}{V_{iMax} - V_{iMin}}\right) \times 100 = \left(\frac{5\ \text{mV}}{238.9\ \text{mV}}\right) \times 100 = 2.09\ \%$$

$$\text{Relative Error at } I_{iMax} = \left(\frac{V_{os}}{V_{iMax}}\right) \times 100 = \left(\frac{5\ \text{mV}}{250\ \text{mV}}\right) \times 100 = 2\ \%$$

$$\text{Relative Error at } I_{iMin} = \left(\frac{V_{os}}{V_{iMin}}\right) \times 100 = \left(\frac{5\ \text{mV}}{11.1\ \text{mV}}\right) \times 100 = 45\ \%$$

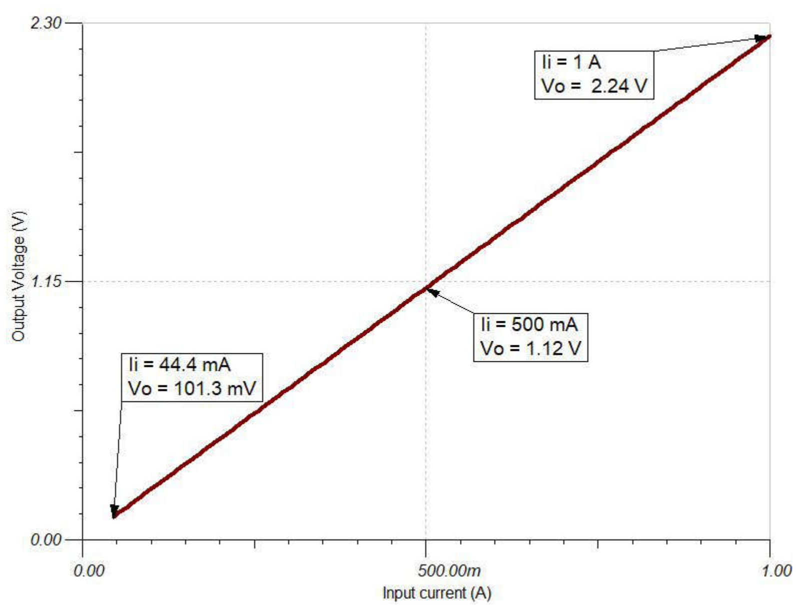
6. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit

$$\frac{1}{2\times\pi\times(C_{cm}+C_{diff})\times(R_2||R_3)} > \frac{\text{GBP}}{G}$$

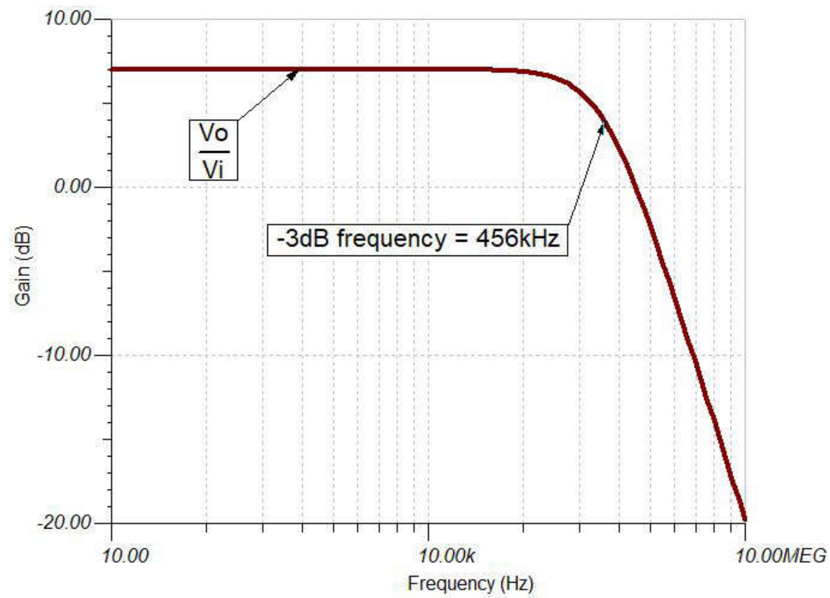
$$\frac{1}{2\times\pi\times(3\text{pF}+3\text{pF})\times\left(\frac{715\ \Omega\times5.69\ \text{k}\Omega}{715\ \Omega+5.69\ \text{k}\Omega}\right)} > \frac{4\ \text{MHz}}{9\ \frac{V}{V}} = 41.76\ \text{MHz} > 444.4\ \text{kHz}$$

Design Simulations

DC Simulation Results



AC Simulation Results



Target Applications

- Cordless power tool battery pack
- E-bike, e-scooter battery pack
- Motor drives
- LED luminaire
- Grid infrastructure

References

1. MSP430 Single-Supply, Low-Side, Unidirectional Current-Sensing Circuit Code Examples and SPICE Simulation File
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. MSP430 MCUs Smart Analog Combo Training

Design Featured Op Amp

<table>
<tr><th colspan="3">MSP430FRxx Smart Analog Combo</th></tr>
<tr><td></td><td>MSP430FR2311 SAC_L1</td><td>MSP430FR2355 SAC_L3</td></tr>
<tr><td>V_{cc}</td><td colspan="2">2.0 V to 3.6 V</td></tr>
<tr><td>V_{CM}</td><td colspan="2">-0.1 V to V_{CC} + 0.1 V</td></tr>
<tr><td>V_{out}</td><td colspan="2">Rail-to-rail</td></tr>
<tr><td>V_{os}</td><td colspan="2">±5 mV</td></tr>
<tr><td>A_{OL}</td><td colspan="2">100 dB</td></tr>
<tr><td rowspan="2">I_q</td><td colspan="2">350 µA (high-speed mode)</td></tr>
<tr><td colspan="2">120 µA (low-power mode)</td></tr>
<tr><td>I_b</td><td colspan="2">50 pA</td></tr>
<tr><td rowspan="2">UGBW</td><td>4 MHz (high-speed mode)</td><td>2.8 MHz (high-speed mode)</td></tr>
<tr><td>1.4 MHz (low-power mode)</td><td>1 MHz (low-power mode)</td></tr>
<tr><td rowspan="2">SR</td><td colspan="2">3 V/µs (high-speed mode)</td></tr>
<tr><td colspan="2">1 V/µs (low-power mode)</td></tr>
<tr><td>Number of channels</td><td>1</td><td>4</td></tr>
<tr><td colspan="3">MSP430FR2311</td></tr>
<tr><td colspan="3">MSP430FR2355</td></tr>
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Design Alternate Op Amp

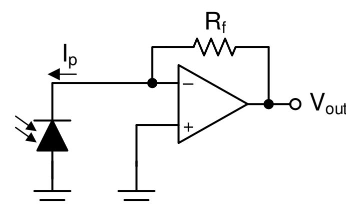
MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
MSP430FR2311	

Related MSP430 Circuits

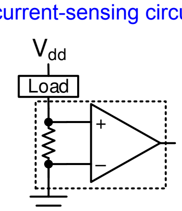
Low-noise and long-range PIR sensor conditioner circuit

Bridge amplifier circuit

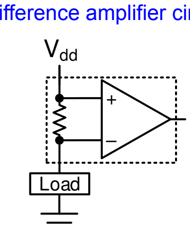
Transimpedance amplifier circuit



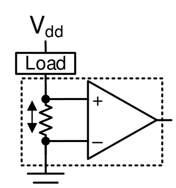
Single-supply, low-side, unidirectional current-sensing circuit



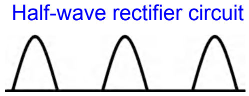
High-side current sensing with discrete difference amplifier circuit



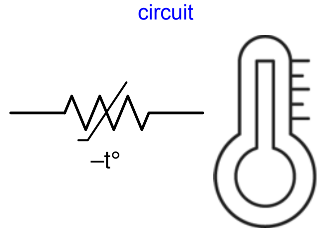
Low-side, bidirectional current-sensing circuit



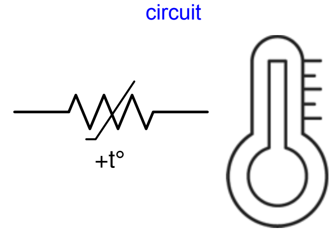
Half-wave rectifier circuit



Temperature sensing with NTC thermistor circuit



Temperature sensing with PTC thermistor circuit



Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 27, 2019 to March 6, 2020 **Page**

Analog Engineer's Circuit

Low-Noise and Long-Range PIR Sensor Conditioner Circuit with MSP430™ Smart Analog Combo

TEXAS INSTRUMENTS

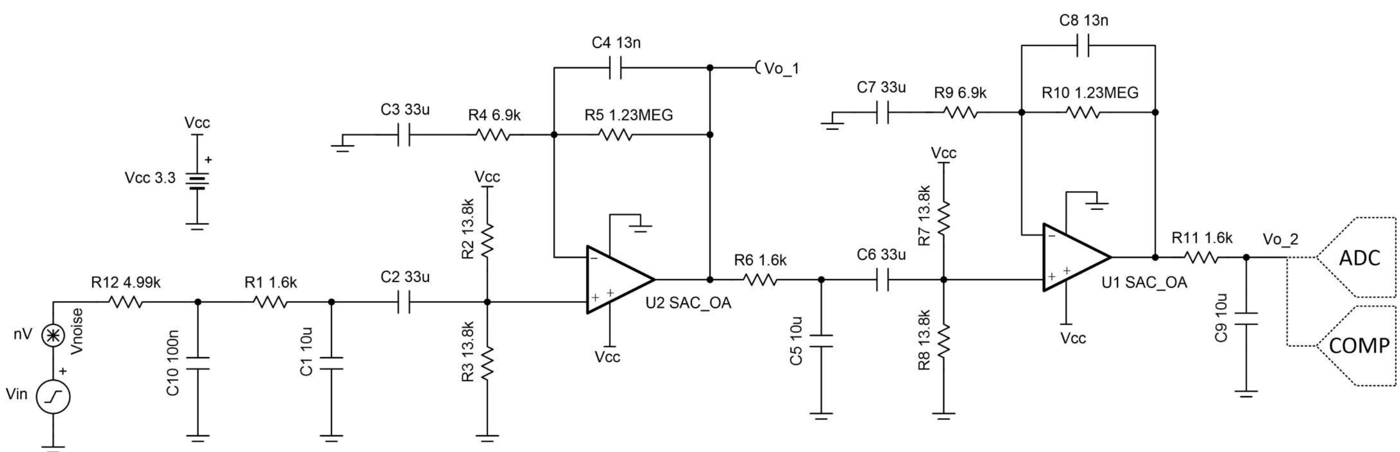
Design Goals

AC Gain	Filter Cut-Off Frequency		Supply	
90 dB	f_L	f_H	V_{cc}	V_{ee}
	0.7 Hz	10 Hz	3.3 V	0 V

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the Smart Analog Combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the Low-Noise Long-Range PIR Sensor Conditioner Circuit Design Files.

This design leverages two of the four integrated op-amp blocks (SACs) in the MSP430FR2355 MCU. Two SAC_L3 peripherals are configured as cascaded op-amps in general-purpose mode to amplify and filter the signal from a passive infrared (PIR) sensor. The circuit includes multiple low-pass and high-pass filters to reduce noise at the output of the circuit to be able to detect motion at long distances and reduce false triggers. The output of the second-stage op-amp in this circuit can be internally or externally connected to other integrated peripherals in the MSP430FR2355 MCU. For example, the analog-to-digital converter (ADC) window comparator can sample this output periodically (with no CPU intervention) and trigger an interrupt when the signal crosses a threshold, indicating motion or an alert.



Design Notes

- The common-mode voltage and output-bias voltage are set using the resistor dividers between R_2 and R_3 (and R_7 and R_8).
- Two or more amplifier stages must be used to allow for sufficient loop gain.
- Additional low-pass and high-pass filters can be added to further reduce noise.
- Capacitors C_4 and C_8 filter noise by decreasing the bandwidth of the circuit and help stabilize the amplifiers.
- RC filters on the output of the amplifiers (for example, R_6 and C_5) are required to reduce the total integrated noise of the amplifier.
- The maximum gain of the circuit can be affected by the cut-off frequencies of the filters. The cut-off frequencies may need to be adjusted to achieve the desired gain.
- For this design, two SAC_L3 peripherals in the MSP430FR2355 MCU are configured as cascaded op-amps in general-purpose mode.
- This design can also be implemented by using the transimpedance amplifier (TIA) and SAC_L1 peripheral in the MSP430FR2311 MCU for the cascaded op-amps, but since the maximum input voltage of the TIA is limited to VCC/2, the common-mode voltage and gain should be limited accordingly.
- The Low-Noise Long-Range PIR Sensor Conditioner Circuit Design Files include a code example demonstrating how to properly configure the SAC_L3 and ADC window comparator peripherals in the MSP430FR2355 MCU.

Design Steps

1. Choose large-valued capacitors C_1, C_5, and C_9 for the low-pass filters. These capacitors should be selected first because large-valued capacitors have limited standard values to select from compared to standard resistor values.

   $$C_1 = C_5 = C_9 = 10\mu F$$

2. Calculate resistor values for R_1, R_6, and R_{11} to form the low-pass filters.

   $$R_1 = R_6 = R_{11} = \frac{1}{2\pi \times f_H \times C_1} = \frac{1}{2\pi \times 10Hz \times 10\mu F} = 1.592k\Omega$$

   $$\text{Choose} \quad R_1 = R_6 = R_{11} = 1.6k\Omega \quad \left(\text{Standard} \quad \text{value}\right)$$

3. Select capacitor values for C_2, C_3, C_6, and C_7 for the high-pass filters.

   $$C_2 = C_3 = C_6 = C_7 = 33\mu F$$

4. Calculate the resistor values for R_4 and R_9 for the high-pass filters.

   $$R_4 = R_9 = \frac{1}{2\pi \times f_L \times C_2} = \frac{1}{2\pi \times 0.7Hz \times 33\mu F} = 6.89k\Omega$$

   $$\text{Choose} \quad R_4 = R_9 = 6.9k\Omega \quad \left(\text{Standard} \quad \text{value}\right)$$

5. Set the common-mode voltage of the amplifier to mid-supply using a voltage divider. The equivalent resistance of the voltage divider should be equal to R_4 to properly set the corner frequency of the high-pass filter.

   $$R_2 = R_3 = R_7 = R_8 = 2 \times R_4 = 2 \times 6.9k\Omega = 13.8k\Omega$$
   $$\text{Choose} \quad R_2 = R_3 = R_7 = R_8 = 13.8k\Omega \quad (\text{Standard} \quad \text{value})$$

6. Calculate the gain required by each gain stage to achieve the total gain requirement. Distribute the total gain target of the circuit evenly between both gain stages.

   $$\text{Gain} = \frac{90dB}{2} = 45dB = 177.828\frac{V}{V}$$

7. Calculate R_5 to set the gain of the first stage.

   $$R_5 = (\text{Gain} - 1) \times R_4 = \left(177.828\frac{V}{V} - 1\right) \times 6.9k\Omega = 1.22M\Omega$$

   $$\text{Choose} \quad R_5 = 1.23M\Omega \quad \left(\text{Standard} \quad \text{value}\right)$$

8. Calculate C_4 to set the low-pass filter cut-off frequency.

   $$C_4 = \frac{1}{2\pi \times f_H \times R_5} = \frac{1}{2\pi \times 10Hz \times 1.23M\Omega} = 12.939nF$$

   $$\text{Choose} \quad C_4 = 13nF \quad \left(\text{Standard} \quad \text{value}\right)$$

9. Since the gain and cut-off frequency of the first gain stage is equal to the second gain stage, set all component values of both stages equal to each other.

   $$R_1 = R_6 = 1.6k\Omega$$
   $$R_7 = R_8 = 13.8k\Omega$$
   $$R_9 = R_4 = 6.9k\Omega$$
   $$R_{10} = R_5 = 1.23M\Omega$$
   $$C_8 = C_4 = 13nF$$

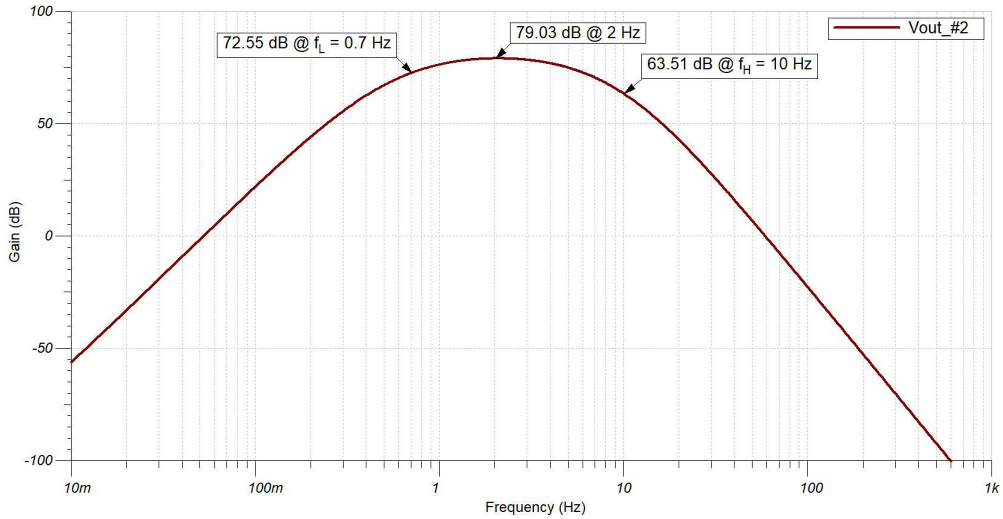
10. Calculate R_{11} to set the cut-off frequency of the low-pass filter at the output of the circuit.

   $$R_{11} = \frac{1}{2\pi \times f_H \times C_9} = \frac{1}{2\pi \times 10Hz \times 10\mu F} = 1.592k\Omega$$

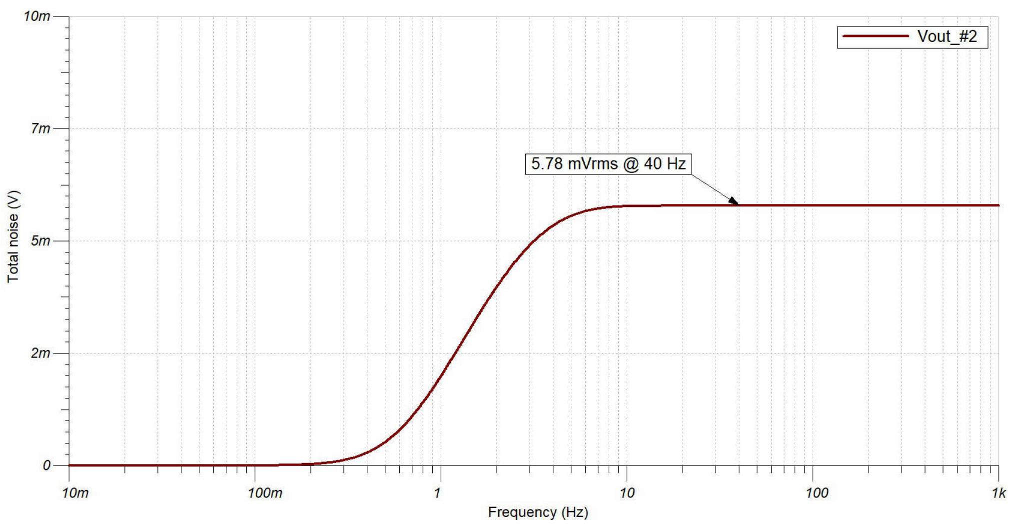
   $$\text{Choose} \quad R_{11} = 1.6k\Omega \quad \left(\text{Standard} \quad \text{value}\right)$$

Design Simulations

AC Simulation Results



Noise Simulation Results



Target Applications

- Motion detector
- Occupancy detection
- Analog security camera
- IP network camera
- Lighting sensor
- Thermostat
- Video doorbell

References

1. Low-Noise Long-Range PIR Sensor Conditioner Circuit Design Files
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. How to Use the Smart Analog Combo in MSP430™ MCUs
5. MSP430 MCUs Smart Analog Combo Training

Design Featured Op Amp

MSP430FRxx Smart Analog Combo		
	MSP430FR2311 SAC_L1	MSP430FR2355 SAC_L3
V_{cc}	2.0 V to 3.6 V	
V_{CM}	-0.1 V to V_{CC} + 0.1 V	
V_{out}	Rail-to-rail	
V_{os}	±5 mV	
A_{OL}	100 dB	
I_q	350 µA (high-speed mode)	
	120 µA (low-power mode)	
I_b	50 pA	
UGBW	4 MHz (high-speed mode)	2.8 MHz (high-speed mode)
	1.4 MHz (low-power mode)	1 MHz (low-power mode)
SR	3 V/µs (high-speed mode)	
	1 V/µs (low-power mode)	
Number of channels	1	4
	MSP430FR2311	MSP430FR2355

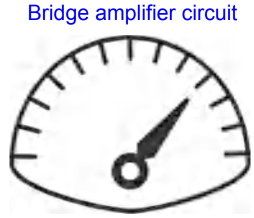
Design Alternate Op Amp

MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
MSP430FR2311	

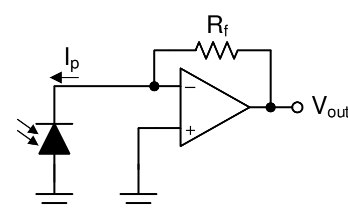
Related MSP430 Circuits

Low-noise and long-range PIR sensor conditioner circuit

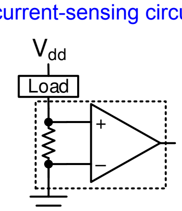
Bridge amplifier circuit



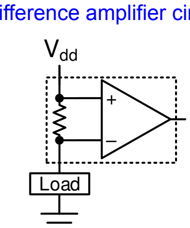
Transimpedance amplifier circuit



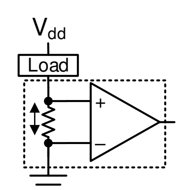
Single-supply, low-side, unidirectional current-sensing circuit



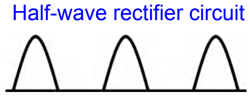
High-side current sensing with discrete difference amplifier circuit



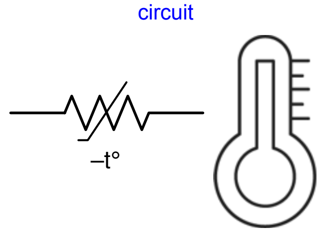
Low-side, bidirectional current-sensing circuit



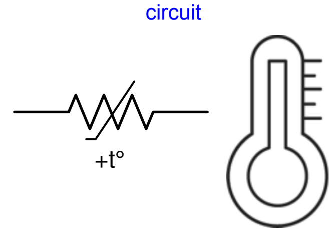
Half-wave rectifier circuit



Temperature sensing with NTC thermistor circuit



Temperature sensing with PTC thermistor circuit



Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 15, 2019 to March 6, 2020	Page
• Added *Related MSP430 Circuits* section	1

Low-Side Bidirectional Current Sensing Circuit with MSP430™ Smart Analog Combo

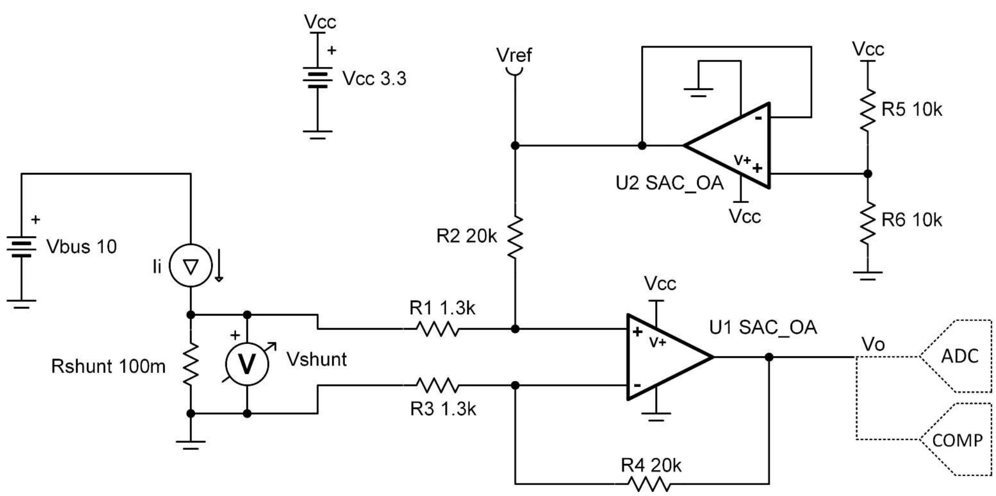
Design Goals

Input		Output		Supply	
I_{iMin}	I_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ref}
–1 A	1 A	100 mV	3.2 V	3.3 V	1.65 V

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the Smart Analog Combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the Low-side Bidirectional Current Sensing Design Files.

This single-supply low-side, bidirectional current sensing solution can accurately detect load currents from –1 A to 1 A. The linear range of the output is from 100 mV to 3.2 V. Low-side current sensing keeps the common-mode voltage near ground, and is thus most useful in applications with large bus voltages. This design leverages two of the four integrated op-amp blocks (SACs) in the MSP430FR2355 MCU. One SAC_L3 peripheral is configured as a general purpose op-amp to amplify the voltage across the shunt resistor, while the other is configured as a buffer to provide the bias voltage (Vref). The latter SAC_L3 block can also be configured in DAC buffer mode to provide Vref, replacing the external voltage divider circuit. The output of the circuit can be internally or externally connected to other integrated peripherals in the MSP430FR2355 MCU. For example, the analog-to-digital converter (ADC) window comparator can sample this output periodically (with no CPU intervention) and trigger an interrupt when the signal crosses a threshold.



Design Notes

- To minimize errors, set $R_3 = R_1$ and $R_4 = R_2$.
- Use precision resistors for higher accuracy.
- Set output range based on linear output swing (see A_{ol} specification).
- Low-side sensing should not be used in applications where the system load cannot withstand small ground disturbances or in applications that need to detect load shorts.
- In the schematic above, the first SAC_L3 peripheral in the MSP430FR2355 MCU (U1) is configured in general purpose mode. The second SAC_L3 peripheral (U2) is also configured in general purpose mode, but with an external voltage divider.
- It is recommended to use the DAC buffer configuration for U2 (as seen in the code examples in the Low-side Bidirectional Current Sensing Design Files) to provide Vref instead of using the external voltage divider circuit.
- This solution can also be implemented using the MSP430FR2311 device by using the internal transimpedance amplifer for U1, and the SAC_L1 op-amp for U2.
- The Low-side Bidirectional Current Sensing Design Files include code examples showing how to properly initialize the SAC peripherals.

Design Steps

1. Determine the transfer equation given $R_4 = R_2$ and $R_1 = R_3$.

$$V_o = \left(I_i \times R_{shunt} \times \frac{R_4}{R_3}\right) + V_{ref}$$

$$V_{ref} = V_{cc} \times \left(\frac{R_6}{R_5 + R_6}\right)$$

2. Determine the maximum shunt resistance.

$$R_{shunt} = \frac{V_{shunt}}{I_{imax}} = \frac{100mV}{1\ \ A} = 100m\Omega$$

3. Set reference voltage.
   a. Because the input current range is symmetric, the reference should be set to mid supply. Therefore, make R_5 and R_6 equal.

$$R_5 = R_6 = 10k\Omega$$

4. Set the difference amplifier gain based on the op amp output swing. The op amp output can swing from 100 mV to 3.2 V, given a 3.3-V supply.

$$\text{Gain} = \frac{V_{oMax} - V_{oMin}}{R_{shunt} \times (I_{iMax} - I_{iMin})} = \frac{3.2\ V - 100mV}{100m\Omega \times (1\ \ A - (-1\ \ A))} = 15.5\ \frac{V}{V}$$

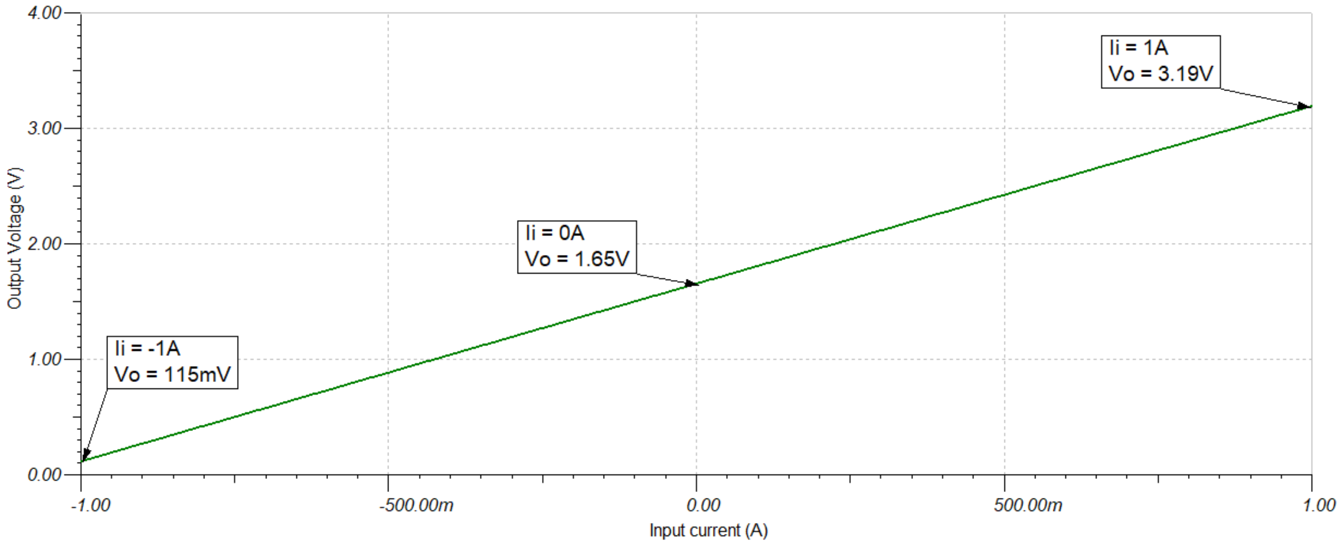
$$\text{Gain} = \frac{R_4}{R_3} = 15.5\ \frac{V}{V}$$

$$\text{Choose } R_1 = R_3 = 1.3k\Omega \text{ (Standard Value)}$$

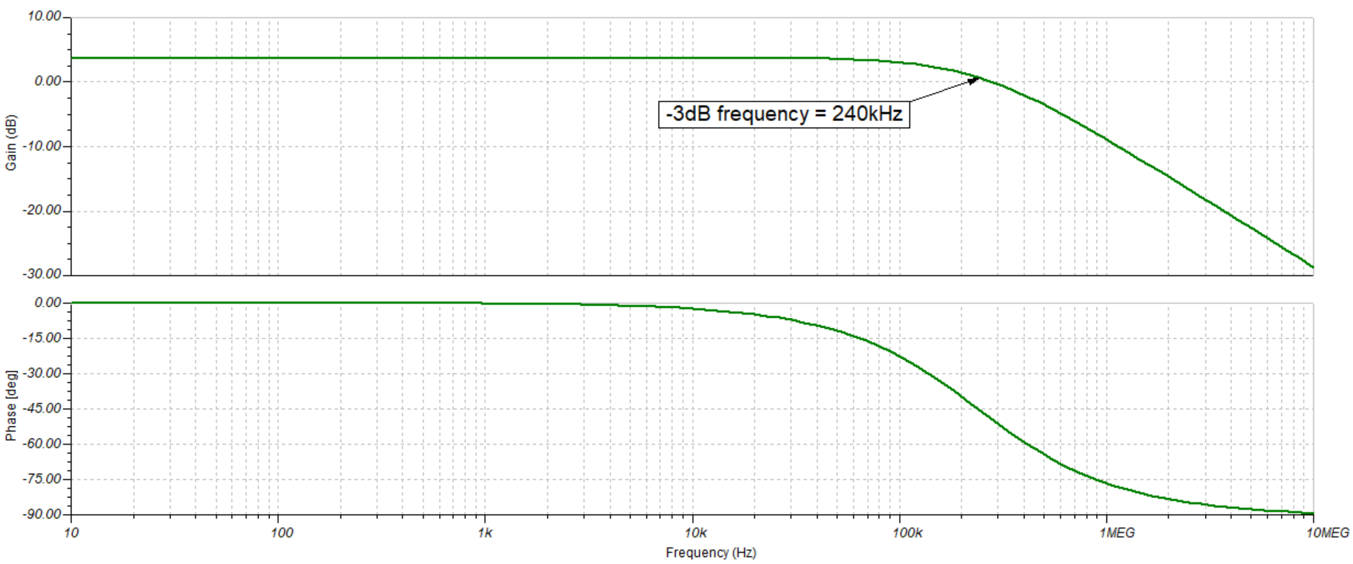
$$R_2 = R_4 = 15.5\frac{V}{V} \times 1.3k\Omega = 20.15\ k\Omega \approx 20k\Omega \text{ (Standard Value)}$$

Design Simulations

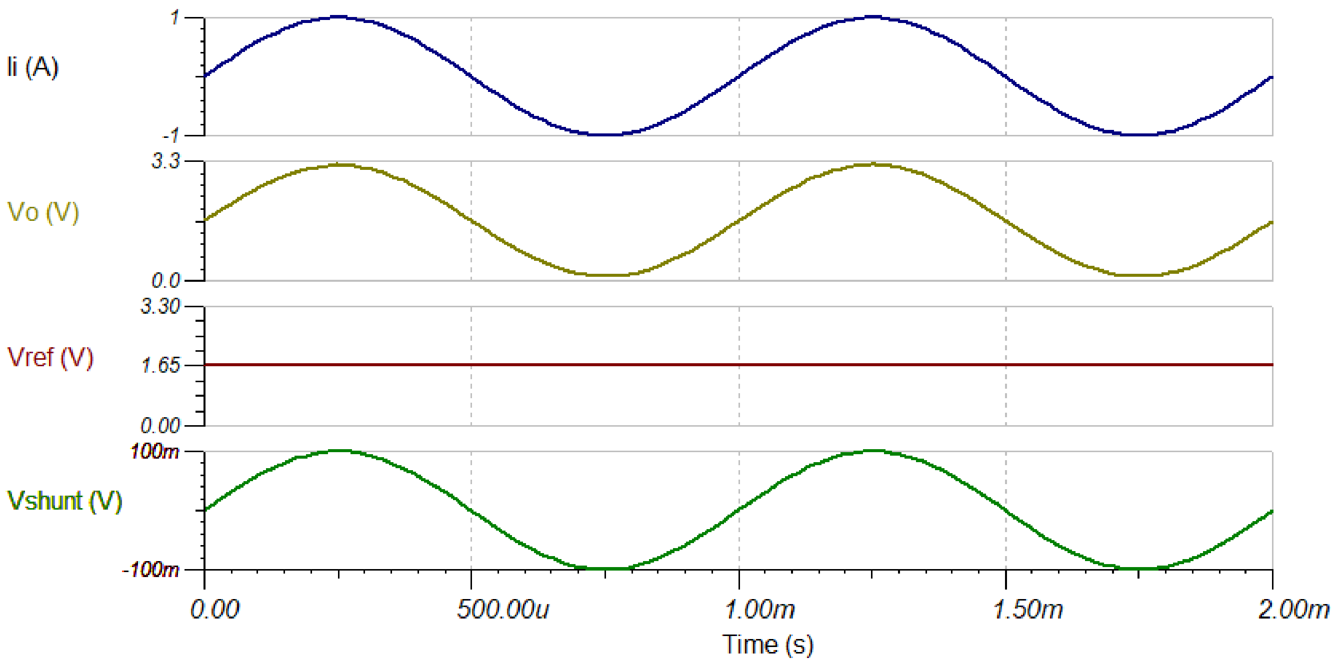
DC Simulation Results



Closed Loop AC Simulation Results



Transient Simulation Results



Target Applications

Motor Drives

Servo Drive Functional Safety Module

Merchant Battery Charger

Battery Pack: Cordless Power Tool

Battery Pack: E-Bike/E-Scooter/Light Electric Vehicle (LEV)

Design References

1. MSP430 Low-side Bidirectional Current Sensing Circuit Code Examples and SPICE Simulation File
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. MSP430 MCUs Smart Analog Combo Training

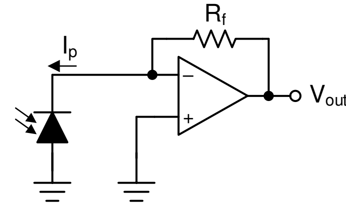
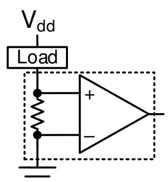
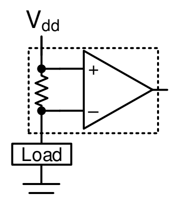
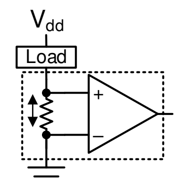
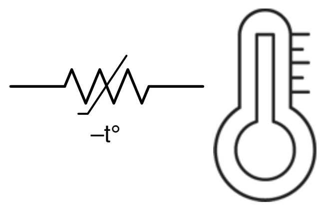
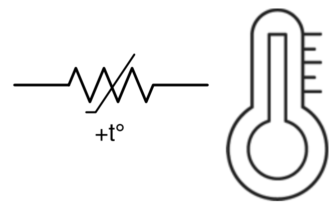
Design Featured Op Amp

MSP430FRxx Smart Analog Combo		
	MSP430FR2311 SAC_L1	MSP430FR2355 SAC_L3
V_{cc}	2.0 V to 3.6 V	
V_{CM}	-0.1 V to V_{CC} + 0.1 V	
V_{out}	Rail-to-rail	
V_{os}	±5 mV	
A_{OL}	100 dB	
I_q	350 µA (high-speed mode)	
	120 µA (low-power mode)	
I_b	50 pA	
UGBW	4 MHz (high-speed mode)	2.8 MHz (high-speed mode)
	1.4 MHz (low-power mode)	1 MHz (low-power mode)
SR	3 V/µs (high-speed mode)	
	1 V/µs (low-power mode)	
Number of channels	1	4
http://www.ti.com/product/MSP430FR2311		
http://www.ti.com/product/MSP430FR2355		

Design Alternate Op Amp

MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
http://www.ti.com/product/MSP430FR2311	

Related MSP430 Circuits

Low-noise and long-range PIR sensor conditioner circuit 	Bridge amplifier circuit 	Transimpedance amplifier circuit 
Single-supply, low-side, unidirectional current-sensing circuit 	High-side current sensing with discrete difference amplifier circuit 	Low-side, bidirectional current-sensing circuit 
Half-wave rectifier circuit 	Temperature sensing with NTC thermistor circuit 	Temperature sensing with PTC thermistor circuit 

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from November 15, 2019 to March 6, 2020	Page
• Added *Related MSP430 Circuits* section	1

Application Note

Half-wave rectifier circuit with MSP430 smart analog combo

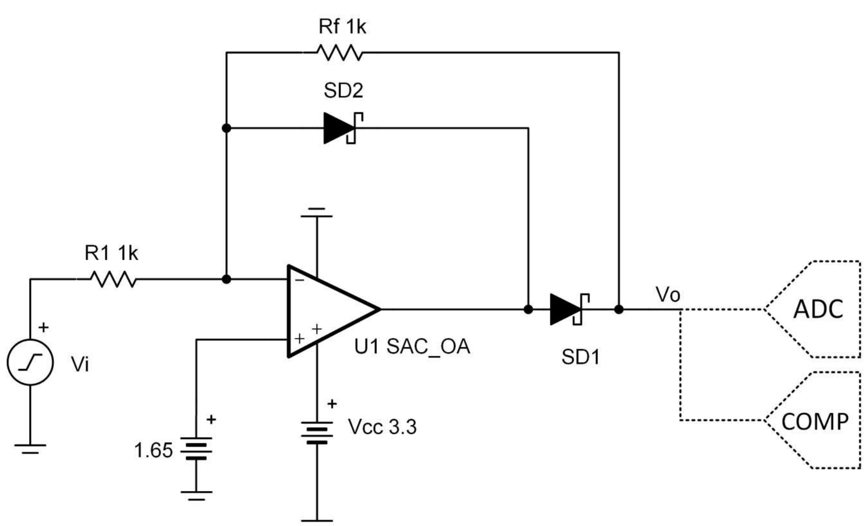
Design Goals

Input		Output		Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	V_{cc}	V_{ee}
0.2 V_{pp}	2 V_{pp}	0.1 V_p	1 V_p	3.3 V	0 V

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the Smart Analog Combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the Half-Wave Rectifier Circuit Design Files.

The precision half-wave rectifier inverts and transfers only the negative-half input of a time varying input signal (preferably sinusoidal) to its output. This circuit uses the MSP430FR2311 SAC_L1 op-amp in an inverting amplifier configuration with the appropriate diodes in place. There is room for further integration by using the integrated DAC in the MSP430FR2355 SAC_L3 block to provide the bias voltage on the non-inverting op-amp terminal. By appropriately selecting the feedback resistor values, different gains can be achieved. Precision half-wave rectifiers are commonly used with other op amp circuits such as a peak-detector or bandwidth limited non-inverting amplifier to produce a DC output voltage. The output of the SAC_L3 op-amp can be cascaded with the other 3 SAC_L3 blocks in the MSP430FR2355 to expand upon the analog signal chain functionality or sampled directly by the onboard ADC or monitored by the onboard comparator for further processing inside the MCU. This configuration has been designed to work for sinusoidal input signals between 0.2 V_{pp} and 2 V_{pp} at frequencies up to 50 kHz.



Design Notes

- Set output range based on linear output swing (see A_{ol} specification).
- Use fast switching diodes. High-frequency input signals will be distorted depending on the speed by which the diodes can transition from blocking to forward conducting mode. Schottky diodes might be a preferable choice, since these have faster transitions than pn-junction diodes at the expense of higher reverse leakage.
- The resistor tolerance sets the circuit gain error.
- Minimize noise errors by selecting low-value resistors.
- If the solution is implemented using the MSP430FR2311, the circuit can be realized by the SAC_L1 op-amp in general purpose mode or the Transimpedance Amplifier (TIA). In both cases the bias voltage can be set using a resistor divider or external DAC.
- If the TIA op-amp is used, the input voltage would need to be kept below VCC/2 to operate within the peripheral's common-mode input specifications.
- If the solution is implemented using the MSP430FR2355, the circuit can be realized using any of the 4 on-board SAC_L3 peripherals in DAC mode in order to generate the bias voltage on the non-inverting op-amp terminal.
- When the input signal changes polarities, the amplifier output must slew two diode voltage drops. The MSP430 SAC and TIA op-amps can be configured in "High-Speed Mode" to achieve a higher slew rate.
- The Half-Wave Rectifier Circuit Design Files include code examples showing how to properly initialize the SAC peripherals.

Design Steps

1. Set the desired gain of the half-wave rectifier to select the feedback resistors.

$$\mathrm{V_o = Gain \times V_i}$$

$$\mathrm{Gain} = -\frac{\mathrm{R_f}}{\mathrm{R_1}} = -1$$

$$\mathrm{R_f = R_1 = 2 \times R_{eq}}$$

   - Where R_{eq} is the parallel combination of R_1 and R_f

2. Select the resistors such that the resistor noise is negligible compared to the voltage broadband noise of the op amp.

$$\mathrm{E_{nr}} = \sqrt{4 \times \mathrm{k_b} \times \mathrm{T} \times \mathrm{R_{eq}}}$$

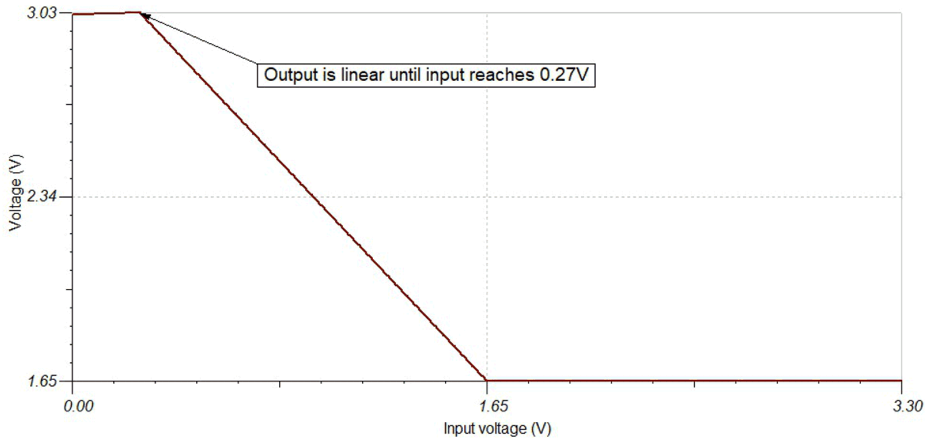
$$\mathrm{R_{eq}} \le \frac{\mathrm{E_{nbb}}^2}{4 \times \mathrm{k_b} \times \mathrm{T} \times 3^2} = (\mathrm{Enbb})$$

$$= 20\frac{\mathrm{nV}}{\sqrt{\mathrm{Hz}}} = \frac{\left(20 \times 10^{-9}\right)^2}{4 \times 1.381 \times 10^{-23} \times 298 \times 3^2} = 2.7k\Omega$$

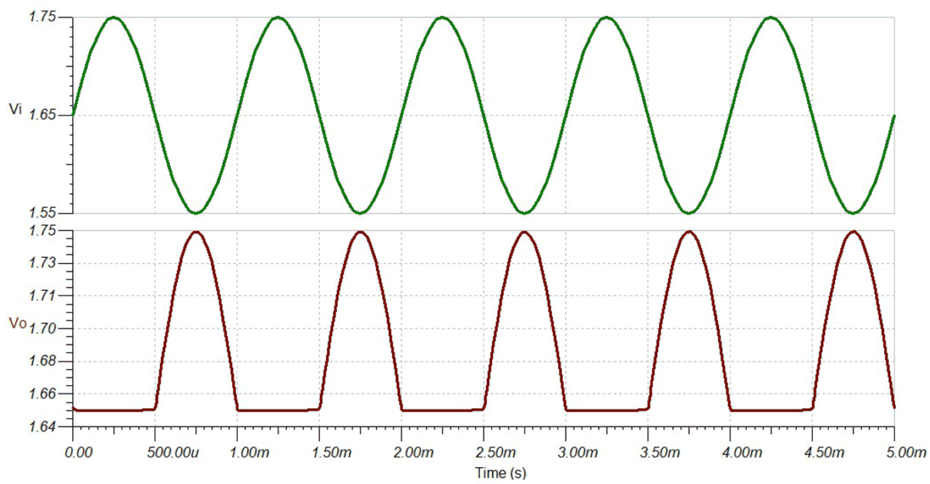
$$\mathrm{R_f = R_1} \le 5.4k\Omega \rightarrow 1k\Omega\ (\mathrm{Standard\ Value})$$

Design Simulations

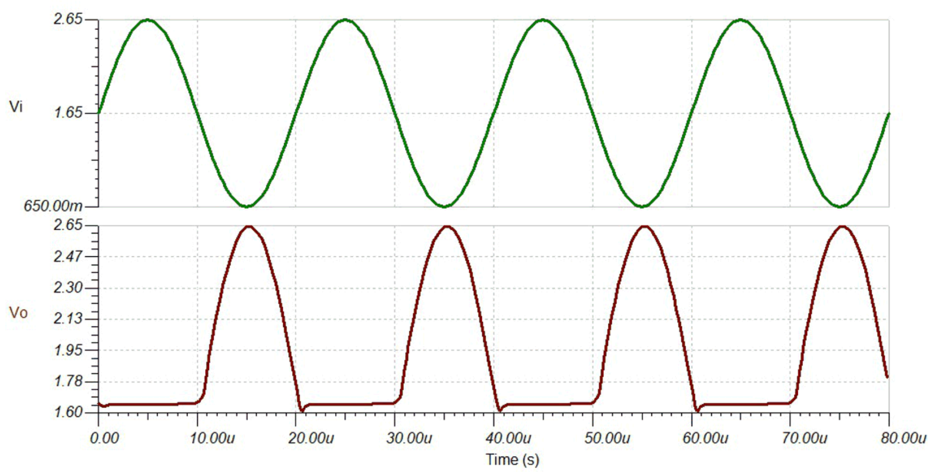
DC Simulation Results



Transient Simulation Results



200 mV_{pp} at 1 kHz



2 V_{pp} at 50 kHz

Target Applications

- Battery charger
- Waveform generator

References

1. MSP430 Half-Wave Rectifier Circuit Code Examples and SPICE Simulation File
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. MSP430 MCUs Smart Analog Combo Training

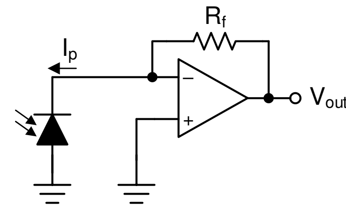
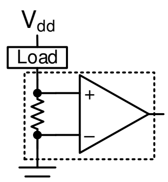
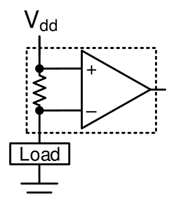
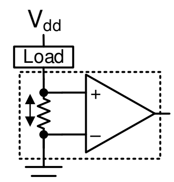
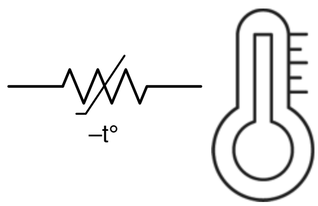
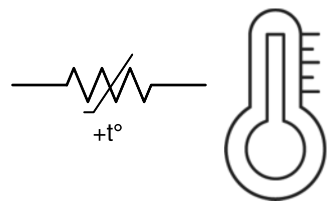
Design Featured Op Amp

MSP430FRxx Smart Analog Combo		
	MSP430FR2311 SAC_L1	MSP430FR2355 SAC_L3
V_{cc}	2.0 V to 3.6 V	
V_{CM}	-0.1 V to V_{CC} + 0.1 V	
V_{out}	Rail-to-rail	
V_{os}	±5 mV	
A_{OL}	100 dB	
I_q	350 µA (high-speed mode)	
	120 µA (low-power mode)	
I_b	50 pA	
UGBW	4 MHz (high-speed mode)	2.8 MHz (high-speed mode)
	1.4 MHz (low-power mode)	1 MHz (low-power mode)
SR	3 V/µs (high-speed mode)	
	1 V/µs (low-power mode)	
Number of channels	1	4
http://www.ti.com/product/MSP430FR2311		
http://www.ti.com/product/MSP430FR2355		

Design Alternate Op Amp

MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
http://www.ti.com/product/MSP430FR2311	

Related MSP430 Circuits

Low-noise and long-range PIR sensor conditioner circuit 	Bridge amplifier circuit 	Transimpedance amplifier circuit 
Single-supply, low-side, unidirectional current-sensing circuit 	High-side current sensing with discrete difference amplifier circuit 	Low-side, bidirectional current-sensing circuit 
Half-wave rectifier circuit 	Temperature sensing with NTC thermistor circuit 	Temperature sensing with PTC thermistor circuit 

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2019) to Revision A (March 2020)	Page
• Added *Related MSP430 Circuits* section	1

Analog Engineer's Circuit

Temperature Sensing PTC Circuit With MSP430™ Smart Analog Combo

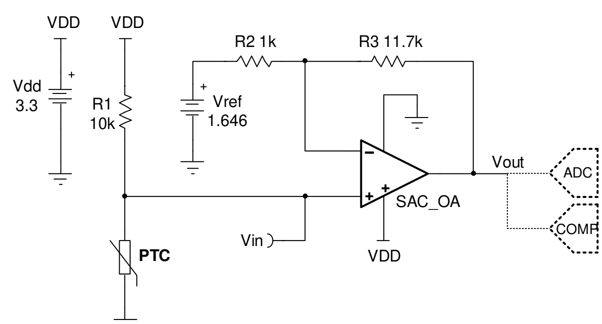
Design Goals

Temperature		Output voltage		Supply		
T_{Min}	T_{Max}	V_{outMin}	V_{outMax}	V_{dd}	V_{ee}	V_{ref}
0°C	50°C	0.15 V	3.15 V	3.3 V	0 V	1.646 V

Design Description

Some MSP430™ microcontrollers (MCUs) contain configurable integrated signal chain elements such as op-amps, DACs, and programmable gain stages. These elements make up a peripheral called the Smart Analog Combo (SAC). For information on the different types of SACs and how to leverage their configurable analog signal chain capabilities, visit MSP430 MCUs Smart Analog Combo Training. To get started with your design, download the Temperature Sensing PTC Circuit Design Files.

This temperature sensing circuit uses a resistor in series with a positive-temperature-coefficient (PTC) thermistor to form a voltage divider, which produces an output voltage that is linear over temperature. The circuit uses the MSP430FR2311 SAC_L1 op-amp in a noninverting amplifier configuration with inverting reference to offset and amplify the signal, which helps to use the full ADC resolution and increase measurement accuracy. (Note: The MSP430FR2355 features four SAC_L3 peripherals which each contain a built-in DAC and PGA, providing a single-chip solution for generating Vref and measuring the thermistor circuit.) The output of the integrated SAC op-amp can be sampled directly by the on-board ADC or monitored by the on-board comparator for further processing inside the MCU.



Design Notes

- The connection, V_{in}, is a positive temperature coefficient output voltage. To measure the output voltage of a negative-temperature-coefficient (NTC) thermistor, switch the position of R_1 and the PTC resistor.
- Vref can be generated by the integrated SAC_L3 DACs in the MSP430FR2355 or a voltage divider. If a voltage divider is used, the equivalent resistance of the voltage divider affects the gain of the circuit.
- Using high-value resistors can degrade the phase margin of the amplifier and introduce additional noise in the circuit. It is recommended to use resistor values around 10 kΩ or less.
- If the solution is implemented using the MSP430FR2311, the SAC_L1 op-amp is configured in general purpose mode to measure the thermistor circuit.
- If the solution is implemented using the MSP430FR2355, one SAC_L3 peripheral is configured in DAC mode to generate the reference voltage and another is configured in general purpose mode to measure the thermistor circuit.

Design Steps

$$V_{out} = V_{dd} \times \frac{R_{PTC}}{R_{PTC} + R_1} \times \frac{R_2 + R_3}{R_2} - \frac{R_3}{R_2} \times V_{ref} \tag{1}$$

1. Calculate the value of R_1 to produce a linear output voltage. Use the minimum and maximum values of the PTC to obtain a range of values for R_1.

$$R_{PTC\_Max} = R_{PTC\ @50°C} = 11.611\ k\Omega \tag{2}$$
$$R_{PTC\_Min} = R_{PTC\ @0°C} = 8.525\ k\Omega$$
$$R_1 = \sqrt{R_{PTC\ @0°C} \times R_{PTC\ @50°C}} = \sqrt{8.525\ k\Omega \times 11.611\ k\Omega} = 9.95\ k\Omega \approx 10\ k\Omega$$

2. Calculate the input voltage range.

$$V_{inMin} = V_{dd} \times \frac{R_{PTC\_Min}}{R_{PTC\_Min} + R_1} = 3.3\ V \times \frac{8.525\ k\Omega}{8.525\ k\Omega + 10\ k\Omega} = 1.519\ V \tag{3}$$
$$V_{inMax} = V_{dd} \times \frac{R_{PTC\_Max}}{R_{PTC\_Max} + R_1} = 3.3\ V \times \frac{11.611\ k\Omega}{11.611\ k\Omega + 10\ k\Omega} = 1.773\ V$$

3. Calculate the gain required to produce the maximum output swing.

$$G_{ideal} = \frac{V_{outMax} - V_{outMin}}{V_{inMax} - V_{inMin}} = \frac{3.15\ V - 0.15\ V}{1.773\ V - 1.519\ V} = 11.811\ \frac{V}{V} \tag{4}$$

4. Select R_2 and calculate R_3 to set the gain calculated in Step 3.

$$Gain = \frac{R_2 + R_3}{R_2} \tag{5}$$
$$R_2 = 1\ k\Omega$$
$$R_3 = R_2 \times \left(G_{ideal} - 1\right) = 1\ k\Omega \times \left(11.811 - 1\right) = 10.811\ k\Omega$$
$$\text{Choose} \quad R_3 = 10.7\ k\Omega \quad \left(\text{Standard value}\right)$$

5. Calculate the actual gain based on standard values of R_2 and R_3.

$$G_{actual} = \frac{R_2 + R_3}{R_2} = \frac{1\ k\Omega + 10.7\ k\Omega}{1\ k\Omega} = 11.7\ \frac{V}{V} \tag{6}$$

6. Calculate the output voltage swing based on the actual gain.

$$V_{out\_swing} = (V_{inMax} - V_{inMin}) \times G_{actual} = (1.773\ V - 1.519\ V) \times 11.7\ \frac{V}{V} = 2.9718 V \tag{7}$$

7. Calculate the maximum output voltage when the output voltage is symmetrical around mid-supply.

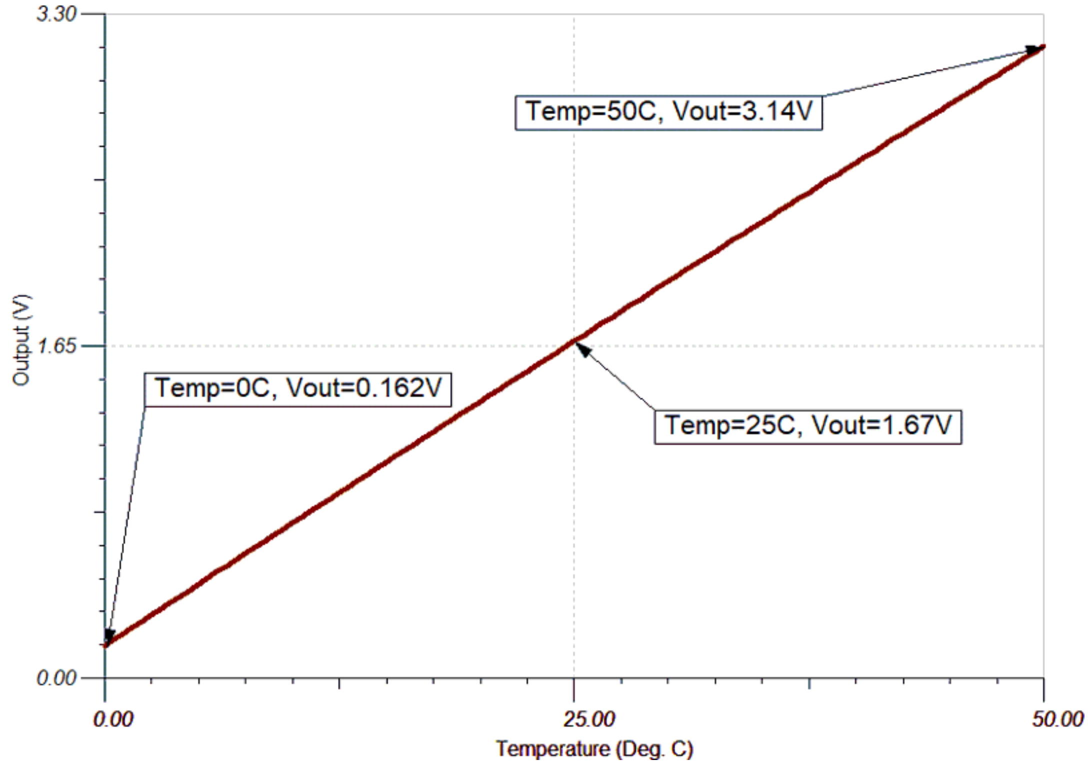
$$V_{outMax} = V_{mid - supply} + \frac{V_{out\_swing}}{2} = \frac{V_{dd} - V_{ee}}{2} + \frac{V_{out\_swing}}{2} = \frac{3.3\ V - 0\ V}{2} + \frac{2.9718\ V}{2} = 3.136\ V \tag{8}$$

8. Calculate the reference voltage.

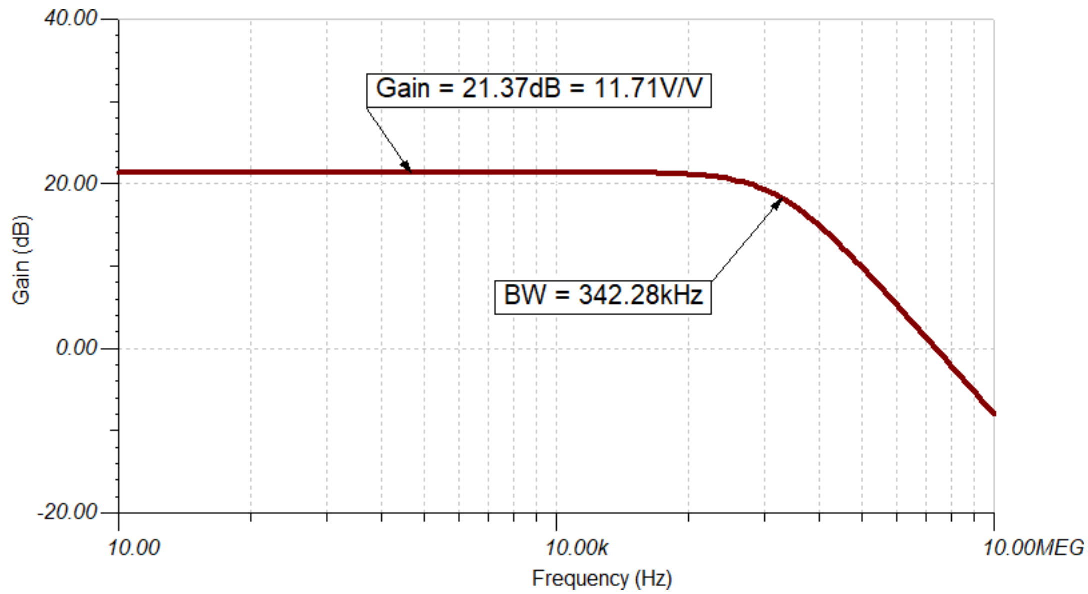
$$V_{outMax} = V_{inMax} \times G_{actual} - \frac{R_3}{R_2} \times V_{ref} \tag{9}$$
$$3.136\ V = 1.773\ V \times 11.7\ \frac{V}{V} - \frac{10.7\ k\Omega}{1\ k\Omega} \times V_{ref}$$
$$V_{ref} = \frac{1.773\ V \times 11.7\ \frac{V}{V} - 3.136\ V}{\frac{10.7\ k\Omega}{1\ k\Omega}} = 1.646\ V$$

Design Simulations

DC Transfer Results



AC Simulation Results



Target Applications

- Field temperature transmitters
- Thermostats
- Thermometers
- Thermistor probes
- System temperature monitor

References

1. MSP430 MCUs Smart Analog Combo Training
2. Analog Engineer's Circuit Cookbooks
3. MSP430FR2311 TINA-TI Spice Model
4. MSP430 Temp Sense PTC Circuit Code Examples and SPICE Simulation File

Design Featured Op Amp

MSP430FRxx Smart Analog Combo		
	MSP430FR2311 SAC_L1	MSP430FR2355 SAC_L3
V_{cc}	2.0 V to 3.6 V	
V_{CM}	-0.1 V to V_{CC} + 0.1 V	
V_{out}	Rail-to-rail	
V_{os}	±5 mV	
A_{OL}	100 dB	
I_q	350 µA (high-speed mode)	
	120 µA (low-power mode)	
I_b	50 pA	
UGBW	4 MHz (high-speed mode)	2.8 MHz (high-speed mode)
	1.4 MHz (low-power mode)	1 MHz (low-power mode)
SR	3 V/µs (high-speed mode)	
	1 V/µs (low-power mode)	
Number of channels	1	4
	MSP430FR2311	MSP430FR2355

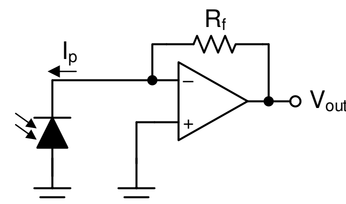
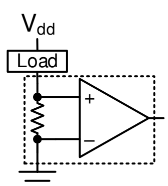
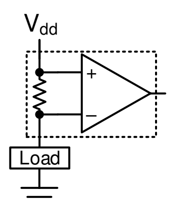
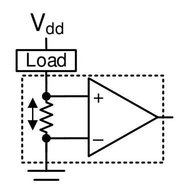
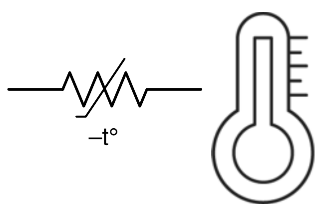
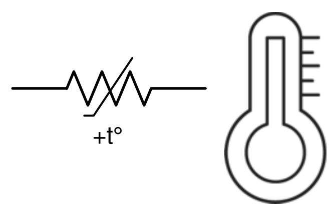
Design Alternate Op Amp

MSP430FR2311 Transimpedance Amplifier	
V_{cc}	2.0 V to 3.6 V
V_{CM}	-0.1 V to V_{CC}/2 V
V_{out}	Rail-to-rail
V_{os}	±5 mV
A_{OL}	100 dB
I_q	350 µA (high-speed mode)
	120 µA (low-power mode)
I_b	5 pA (TSSOP-16 with OA-dedicated pin input)
	50 pA (TSSOP-20 and VQFN-16)
UGBW	5 MHz (high-speed mode)
	1.8 MHz (low-power mode)
SR	4 V/µs (high-speed mode)
	1 V/µs (low-power mode)
Number of channels	1
MSP430FR2311	

Design Featured Thermistor

TMP61	
V_{CC}	Up to 5.5 V
R_{25}	10 kΩ
R_{TOL}	1%
I_{SNS}	400 μA
Operating temperature range	-40°C to 125°C
TMP61	

Related MSP430 Circuits

Low-noise and long-range PIR sensor conditioner circuit 	Bridge amplifier circuit 	Transimpedance amplifier circuit 
Single-supply, low-side, unidirectional current-sensing circuit 	High-side current sensing with discrete difference amplifier circuit 	Low-side, bidirectional current-sensing circuit 
Half-wave rectifier circuit 	Temperature sensing with NTC thermistor circuit 	Temperature sensing with PTC thermistor circuit 

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from October 19, 2019 to March 6, 2020 **Page**

Additional resources to explore

TI Precision Labs
ti.com/precisionlabs
- On-demand courses and tutorials ranging from introductory to advanced concepts that focus on application-specific problem solving
- Hands-on labs and evaluation modules (EVMs) available
  - TIPL Op Amps experimentation platform, ti.com/TIPL-amp-evm
  - TIPL SAR ADC experimentation platform, ti.com/TIPL-adc-evm

Analog Engineer's Pocket Reference
ti.com/analogrefguide
- Printed circuit board (PCB), analog and mixed-signal design formulae; includes conversions, tables and equations

***The Signal*™ e-book**
ti.com/signalbook
- Op amp e-book with short, bite-sized lessons on design topics such as offset voltage, input bias current, stability, noise and more

PSpice® for TI
ti.com/tool/pspice-for-ti
- Supports simultaneous analysis of multiple products
- Pre-installed library with a suite of digital models to enable worst-case timing analysis

TINA-TI™ Simulation Software
ti.com/tool/tina-ti
- Complete SPICE simulator for DC, AC, transient and noise analysis
- Includes schematic entry and post-processor for waveform math

Analog Engineer's Calculator
ti.com/analogcalc
- ADC and amplifier design tools, noise and stability analysis, PCB and sensor tools

TI E2E™ Community
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- Support forums for all TI products

Op Amp Circuit Quick Search and Parametric Search
ti.com/opamp-search
- Search our op amp portfolio by entering key parameters or selecting a circuit function

DIY Amplifier Circuit Evaluation Module (DIYAMP-EVM)
ti.com/DIYAMP-EVM
- Single-channel circuit EVM providing SC-70, small-outline transistor (SOT)-23 and small-outline integrated circuit package options in 12 popular amplifier configurations

Dual-Channel DIY Amplifier Circuit Evaluation Module (DUAL-DIYAMP-EVM)
ti.com/dual-diyamp-evm
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